PCN N	umber:		20160309000					P	CN	Date:	03/30/2016	
Title: TPS62231TDRYRQ1 and TPS622314TDRYRQ1 LLGA to etch and Datasheet update for TPS62231-Q1/TPS622314-Q1												
Custor		PCN Manager				PCN Type:	180 day			Dept:	Quality Services	
Propos	sed 1 st 9	Ship Date:	09/30/2016 Estimated Sam Availability				-					
Chang	e Type:											
As	sembly S	Site			Design				Wafer Bump Site			
As:	sembly I	Process		\boxtimes	Data Sheet				Wafer Bump Material			
⊠ As:	sembly I	Materials			Part number change				Wafer Bump Process			
Me	chanical	Specification		Test Site				Wafer Fab Site				
Pa	cking/Sh	nipping/Labeli	ng		Test Process				Wafer Fab Materials			
									Wa	afer Fab F	Process	
•	PCN Details											

Description of Change:

Texas Instruments Incorporated is announcing the qualification to convert leadframe from LLGA (Lead-frame Land Grid Array) to etch and change Die Attach/Mold Compound as seen in the below table.

Datasheet is also changing per updated thermal model data.

Description	From	To
Mold Compound	SID#CZ0140	SID#CZ0297
LeadFrame	SID#FO0003	SID#FU0148
Die Attach	SID#PZ0039	SID#PZ0037

The product datasheet is being updated as summarized below. The following change history provides further details.



TPS62231-Q1, TPS622314-Q1

SLVSB63A - DECEMBER 2011-REVISED MARCH 2016

www.ti.com

Changes from Original (December 2011) to Revision A

Page

•	Added Pin Configuration and Functions section, ESD Ratings table, Thermal Information table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section	. 1
•	Changed the Applications list	. 1
•	Deleted the Ordering Information table	. 1
•	Deleted references to devices and voltage options that are not available as automotive grade	. 1
•	Added minimum and maximum recommended values for output inductance and output capacitance in the Recommended Operating Conditions table for clarity	. 4
•	Deleted the Dissipation Ratings table and added a more detailed Thermal Information table	. 4
	Deleted the Parameter Measurement Information section	7

The datasheet number will be changing.

Device Family	Change From:	Change To:
TPS62231-Q1/TPS622314-Q1	SLVSB63	SLVSB63A

These changes may be reviewed at the datasheet links provided. The electrical parameter and characteristics will not change.

http://www.ti.com/product/tps62231-q1 http://www.ti.com/product/tps622314-q1

Reason for Change:

- Proactively improved device package delamination performance.
- Update thermal model data in the datasheet to reflect the change in leadframe.

Anticipated impact on Fit, Form, Function, Quality or Reliability (positive / negative):

None.

Changes to product identification resulting from this PCN:

None.

Product Affected:

TPS622314TDRYRQ1, TPS62231TDRYRQ1



TI Confidential NDA Restrictions

Automotive New Product Qualification Summary (As per AEC-Q100 and JEDEC Guidelines)

Approved 15-Dec-2015

Product Attributes

Attributes	Qual Device: TPS62231TDRYRQ1	Qual Device: TPS62237TDRYRQ1	Qual Device: TPS62239TDRYRQ1
Assembly Site	UTAC	UTAC	UTAC
Package Type	USON	USON	USON
Flammability Rating	UL 94 V-0	UL 94 V-0	UL 94 V-0
Wafer Fab Supplier	DMOS5	DMOS5	DMOS5
Wafer Process ID	LBC7	LBC7	LBC7

⁻ QBS: Qual By Similarity

Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

	Туре	#	Test Spec	Min Lot Qty	SS/Lo t	Test Name / Condition	Duration	Qual Device: TPS62231TDRYRQ 1	Qual Device: TPS62237TDRYRQ 1	Qual Device: TPS62239TDRYRQ 1
T	est Grou	ıр A –	- Accelerate	d Envi	ronment	Stress Tests				
	PC	A1	JEDEC J-STD- 020 JESD22- A113	3	77	Automotive Preconditionin g Level 2	260C peak	3/all/0	•	-
	HAS T	A2	JEDEC JESD22- A110	3	77	Biased HAST, 130C/85%RH	96 hrs	1/77/0	-	-
	AC	А3	JEDEC JESD22- A102	3	77	Autoclave 121C	96 hrs	1/77/0	-	-
	TC	A4	JEDEC JESD22- A104 and Appendi	3	77	Temperature Cycle, - 65/150C	500 cycles	1/77/0	-	-

⁻ Qual Device TPS62231TDRYRQ1 is qualified at LEVEL2-260C

Туре	#	Test Spec x 3	Min Lot Qty	SS/Lo t	Test Name / Condition	Duration	Qual Device: TPS62231TDRYRQ 1	Qual Device: TPS62237TDRYRQ 1	Qual Device: TPS62239TDRYRQ 1
			1	5	Wire Pull	Post TC	1/5/0	-	-
PTC	A5	JEDEC JESD22- A105	1	45	Power Temperature Cycle	1000 Cycles	N/A	N/A	N/A
HTSL	A6	JEDEC JESD22- A103	1	45	High Temp Storage Bake 150C	1000 cycles	1/77/0	-	-
Test Grou	ıр В –		d Lifet	ime Simu	lation Tests				
HTO L	B1	JEDEC JESD22- A108	3	77	Life Test, 125C	408 hrs	-	-	1/77/0
ELFR	B2	AEC Q100- 008	3	800	Early Life Failure Rate, 125C	48 Hrs	-	-	-
EDR	В3	AEC Q100- 005	3	77	NVM Endurance, Data Retention, and Operational Life	-	N/A	N/A	N/A
Test Grou	ıр С –	Package A	ssemb	oly Integri	ty Tests				
WBS	C 1	AEC Q100- 001	1	30	Wire Bond Shear	Cpk>1.67	1/30/0		
WBP	C 2	MIL- STD883 Method 2011	1	30	Wire Bond Pull	Cpk>1.67	1/30/0	-	-
SD	C 3	JEDEC JESD22- B102	1	15	Surface Mount Solderability	>95% Lead Coverage	1/15/0	-	-
PD	C 4	JEDEC JESD22- B100 and B108	3	10	Auto Physical Dimensions	Cpk>1.67	1/10/0	-	-
SBS	C 5	AEC Q100- 010	3	50	Solder Ball Shear (Cpk>1.67)	Post HTSL/Bum p	NA	NA	NA
SBS	C 5	AEC Q100- 010	3	50	Solder Ball Shear (Cpk>1.67)	Solder Balls	NA	NA	NA
LI	C 6	JEDEC JESD22- B105	1	50	Lead Integrity	-	NA	NA	NA
Test Grou	ıр E –	Electrical \	/erifica	ition Test	S				
НВМ	E2	AEC Q100- 002	1	3	ESD - HBM - Q100	2000 V	1/3/0	-	-
CDM	E3	AEC Q100-	1	3	ESD - CDM - Q100	500 V (all pins)	1/3/0	-	-

Туре	#	Test Spec	Min Lot Qty	SS/Lo t	Test Name / Condition	Duration	Qual Device: TPS62231TDRYRQ 1	Qual Device: TPS62237TDRYRQ 1	Qual Device: TPS62239TDRYRQ 1
		011				750 V (corner			
						pins)			
						1000 V (all pins) For information only	1/3/0	-	-
LU	E4	AEC Q100- 004	1	6	Latch-up	105 C	1/6/0	-	-
ED	E5	AEC Q100- 009	3	30	Auto Electrical Distributions	Cpk>1.67 Room, hot, and cold test	1/30/0	1/30/0	1/30/0

A1 (PC): Preconditioning:

Performed for THB, Biased HAST, AC, uHAST &TC samples, as applicable.

Junction Operating Temperature by Automotive Grade Level:

Grade 0 (or E): -40°C to +150°C Grade 1 (or Q): -40°C to +125°C Grade 2 (or T): -40°C to +105°C Grade 3 (or I): -40°C to +85°C

E1 (TEST): Electrical test temperatures of Qual samples (High temperature according to Grade level):

Room/Hot/Cold: HTOL, ED

Room/Hot: THB / HAST, TC / PTC, HTSL, ELFR, ESD & LU

Room: AC/uHAST

Green/Pb-free Status:

Qualified Pb-Free(SMT) and Green

TI Qualification ID: 20150721-114721

Quality and Reliability Data Disclaimer

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customer should provide adequate design and operating safeguards. Quality and reliability data provided by Texas Instruments is intended to be an estimate of product performance based upon history only. It does not imply that any performance levels reflected in such data can be met if the product is operated outside the conditions expressly stated in the latest published data sheet or agreed-to customer specification for a device.

Reliability data shows characteristic failure mechanisms of the specific environmental stress as documented in the industry standards for each stress condition.

For questions regarding this notice, e-mails can be sent to the regional contacts shown below or your local Field Sales Representative

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