PCN Num	ber:	20230210	001	.1	I	PCN Date:	February 13, 2023			
Title: Qualification of TI Malaysia as an additional Assembly site for select devices										
Custome	r Contact:	PCN Manage	<u>er</u>	Dept:	Dept: Quality Services					
Proposed	1 st Ship Date	e: May 13	13, 2023Sample requests accepted until:							
*Sample	*Sample requests received after Mar 13, 2023 will not be supported.									
Change T	Change Type:									
🛛 Asse	mbly Site	•		Design			Wafer Bump Site			
Asse	mbly Process			Data Sheet			Wafer Bump Material			
Assembly Materials				Part number change			Wafer Bump Process			
Mech Mech	nanical Specific	ation		Test Site			Wafer Fab Site			
Packing/Shipping/Labeling				Test Process			Wafer Fab Materials			
							Wafer Fab I	Process		
	PCN Details									

Description of Change:

Texas Instruments is pleased to announce the qualification of TI Malaysia as additional Assembly Site for Select Devices listed in the "Product Affected" Section. No material differences between sites.

Assembly Site	Assembly Site Origin	Assembly Country Code	Assembly City		
TI Taiwan	TAI	TWN	Chung Ho, New Taipei City		
TI Malaysia	MLA	MYS	Kuala Lumpur		

Package Marking Differences:

	TAI	MLA				
TI Bug	Include	Replace with "TI" text				
**ECAT	Include Value	Remove				
Example	\T/ YMLLLLS UCC21530 G4 O \TTI/ = TI LOGO YM = YEAR MONTH DATE (S = ASSY SITE CODE LLLL = LOT TRACE CODE G4 = ECAT VALUE O = PIN 1 INDICATOR	ODE	TI YMLLLLS UCC21530 O TI = TI LETTER YM = YEAR MONTH DATE O S = ASSY SITE CODE LLLL = LOT TRACE CODE O = PIN 1 INDICATOR	CODE		

** - Not all devices have ECAT information included in the symbolization, but for the ones that do, this information will be removed.

Reason for Change:

Continuity of supply.

Anticipated impact on Form, Fit, Function, Quality or Reliability (positive / negative): None

Impact on Environmental Ratings

RoHS	REACH	Green Status	IEC 62474
No Change	🛛 No Change	🛛 No Change	🛛 No Change
iges to product	t identification resulting	from this PCN:	
sembly Site			
Taiwan	Assembly Site Origin	(22L) ASO: TAI	
Malaysia	Assembly Site Origin	()	
DE IN: Malaysia C: 20: L'2 /260C/1 YEAR S L 1 /235C/UNLIM 0 T:		(1P) SN74LS07NSR (Q) 2000 (D) 0336 (31T) LOT: 3959047MLA (4W) TKY (1T) 752348353 (P) (2P) REV: (V) 0033317 (20L) CS0: SHE (21L) CC0:USA	
1 /235C/UNLIM 0	<u>3/29/04</u>	(P) (2P) REV: (V) 0033317	

Qualification Report

Automotive New Product Qualification Summary (As per AEC-Q100 and JEDEC Guidelines)

Approve Date 31-Jan-2023

Product Attributes

Attributes	Qual Device:	QBS Reference:	QBS Reference:	QBS Reference:	QBS Reference:	QBS Reference:	QBS Reference:	
Attributes	UCC21320QDWKRQ1	ISOW7841EQDWEQ1	UCC21520QDWRQ1	ISO7741FEDWRQ1	IS06741QDWQ1	UCC21520AQDWRQ1	TMP451AQDQERQ1	
Automotive Grade Level	Grade 1	Grade 1	Grade 1	Grade 0	Grade 1	Grade 1	Grade 1	
Operating Temp Range (C)	-40 to 125	-40 to 125	-40 to 125	-40 to 150	-40 to 125	-40 to 125	-40 to 125	
Product Function	Power Management	Interface	Power Management	Interface	Interface	Power Management	Power Management	
Wafer Fab Supplier	DP1DM5, DP1DM5, DP1DM5	DP1DM5, DP1DM5	DP1DM5, DP1DM5	MH8, MH8	MH8, MH8	MH8, MH8, MH8	DP1DM5	
Assembly Site	MLA	TAI	TAI	TAI	MLA	MLA	UTL1	
Package Group	SOIC	SOIC	SOIC	SOIC	SOIC	SOIC	QFN	
Package Designator	DWK	DWE	DW	DW	DW	DW	DQF	
Pin Count	14	16	16	16	16	16	8	

QBS: Qual By Similarity Qual Device UCC21320QDWKRQ1 is qualified at MSL2 260C

Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

Туре	=	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: UCC21320QDWKRQ1	QBS Reference: ISOW7841FQDWEQ1	QBS Reference: UCC21520QDWRQ1	QBS Reference: ISO7741FEDWRQ1	QBS Reference: ISO6741QDWQ1	QBS Reference: UCC21520AQDWRQ1	QBS Reference: TMP451AQDQFRQ1
Test Group	A - Acce	lerated Enviror	nment St	ress Tes	:ts		•							
PC	A1	JEDEC J- STD-020 JESD22- A113	3	77	Preconditioning	MSL2 260C	1 Step	No Fails	-	-	-	No Fails	-	-
PC	A1	JEDEC J- STD-020 JESD22- A113	3	77	Preconditioning	MSL3 260C	1 Step		-	-		-	No Fails	-
HAST	A2	JEDEC JESD22- A110	3	77	Biased HAST	130C/85%RH	96 Hours	-	-	-		3/231/0	3/231/0	
AC/UHAST	A3	JEDEC JESD22- A102/JEDEC JESD22- A118	3	77	Autoclave	121C/15psig	96 Hours	3/231/0	-	-		3/231/0	3/231/0	-
тс	A4	JEDEC JESD22- A104 and Appendix 3	3	77	Temperature Cycle	-65C/150C	500 Cycles	3/231/0	-	-	-	3/231/0	3/231/0	-
HTSL	A6	JEDEC JESD22- A103	1	45	High Temperature Storage Life	150C	1000 Hours	-	-	-	-	3/135/0	-	-
HTSL	A6	JEDEC JESD22- A103	1	45	High Temperature Storage Life	175C	500 Hours	-	-	-	-	-	3/135/0	
Test Group	B - Acce	lerated Lifetime	e Simula	tion Tes	ts									
HTOL	B1	JEDEC JESD22- A108	1	77	Life Test	125C	1000 Hours	-	3/231/0	3/231/0	-	3/231/0	1/77/0	-
HTOL	B1	JEDEC JESD22- A108	1	77	Life Test	150C	1000 Hours	-	-	-	3/231/0	-	-	-
HTOL	B1	JEDEC JESD22- A108	1	77	Life Test	150C	408 Hours	-	-	-		-	-	3/231/0
ELFR	B2	AEC Q100- 008	1	77	Early Life Failure Rate	125C	48 Hours	-	3/840/3 ¹	-	-	-	-	-
ELFR	B2	AEC Q100- 008	1	77	Early Life Failure Rate	150C	24 Hours		-		-	-	-	3/2400/0
ELFR	B2	AEC Q100- 008	1	77	Early Life Failure Rate	150C	48 Hours		-	-	3/2400/0	-	•	-

Test Group	C - Pack	age Assembly	Integrity	Tests	,		,							
WBS	C1	AEC Q100- 001	1	30	Wire Bond Shear	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	3/90/0	3/90/0	3/90/0	3/90/0	3/90/0	3/90/0	3/90/0
WBP	C2	MIL-STD883 Method 2011	1	30	Wire Bond Pull	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	3/90/0	3/90/0	3/90/0	3/90/0	3/90/0	3/90/0	3/90/0
SD	C3	JEDEC J- STD-002	1	15	PB Solderability	>95% Lead Coverage	-	-	1/15/0	1/15/0	1/15/0	1/15/0	1/15/0	
SD	C3	JEDEC J- STD-002	1	15	PB-Free Solderability	>95% Lead Coverage	-	-	1/15/0	1/15/0	1/15/0	1/15/0	1/15/0	-
PD	C4	JEDEC JESD22- B100 and B108	1	10	Physical Dimensions	Cpk>1.67	-	3/30/0	2/20/0	3/30/0	3/30/0	3/30/0	3/30/0	3/30/0
Test Group	D - Die F	abrication Relia	ability Te	sts										
ЕМ	D1	JESD61			Electromigration			Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
TDDB	D2	JESD35	-		Time Dependent Dielectric Breakdown		-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
нсі	D3	JESD60 & 28			Hot Carrier Injection		-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
NBTI	D4	-	-		Negative Bias Temperature Instability			Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
SM	D5	-	-	-	Stress Migration	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements
Test Group	E - Elect	rical Verification	n Tests											
ESD	E2	AEC Q100- 002	1	3	ESD HBM	-	2000 Volts		1/3/0	1/3/0	1/3/0	1/3/0	-	1/3/0
ESD	E3	AEC Q100- 011	1	3	ESD CDM		500 Volts	1/3/0	1/3/0	1/3/0	1/3/0	1/3/0	1/3/0	1/3/0
LU	E4	AEC Q100- 004	1	6	Latch-Up	Per AEC Q100-004	-		1/6/0	1/6/0	1/6/0	1/6/0		1/6/0
ED	E5	AEC Q100- 009	3	30	Electrical Distributions	Cpk>1.67 Room, hot, and cold	-	1/30/0	3/90/0	3/90/0	3/90/0	3/90/0	3/90/0	3/90/0

Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable

The following are equivalent HTOL options based on an activation energy of 0.7eV : 125C/1k Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours

The following are equivalent HTSL options based on an activation energy of 0.7eV:150C/1k Hours, and 170C/420 Hours

The following are equivalent Temp Cycle options per JESD47 : -55C/125C/700 Cycles and -65C/150C/500 Cycles **Ambient Operating Temperature by Automotive Grade Level:** Grade 0 (or E): -40C to +150C Grade 1 (or Q): -40C to +125C Grade 2 (or T): -40C to +105C Grade 3 (or I) : -40C to +85C **E1 (TEST): Electrical test temperatures of Qual samples (High temperature according to Grade level):** Room/Hot/Cold : HTOL, ED Room/Hot : THB / HAST, TC / PTC, HTSL, ELFR, ESD & LU Room : AC/uHAST Quality and Environmental data is available at TI's external Web site: <u>http://www.ti.com</u>

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