DATA SHEET
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Operational Amplifier, Rail-to-Rail, Low Input Bias Current, 1.8 V to 5 V Single-Supply

LMV301

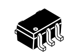
The LMV301 CMOS operational amplifier can operate over a power supply range from 1.8 V to 5 V and has a quiescent current of less than 200 μA, maximum, making it ideal for portable battery−operated applications such as notebook computers, PDA's and medical equipment. Low input bias current and high input impedance make it highly tolerant of high source−impedance signal−sources such as photodiodes and pH probes. In addition, the LMV301's excellent rail−to−rail performance will enhance the signal−to−noise performance of any application together with an output stage capable of easily driving a 600 Ω resistive load and up to 1000 pF capacitive load.

Features

- Single Supply Operation (or $\pm V_S/2$)
- V_S from 1.8 V to 5 V
- Low Quiescent Current: 185 μA, Max with V_S = 1.8 V
- Rail−to−Rail Output Swing
- Low Bias Current: 35 pA, max
- No Output Phase−Reversal when the Inputs are Overdriven
- These are Pb−Free Devices

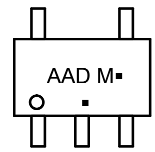
Typical Applications

- Portable Battery−Powered Instruments
- Notebook Computers and PDAs
- Cell Phones and Mobile Communication
- Digital Cameras
- Photodiode Amplifiers
- Transducer Amplifiers
- Medical Instrumentation
- Consumer Products



SC70−5
SQ SUFFIX
CASE 419A
STYLES 3

MARKING DIAGRAM

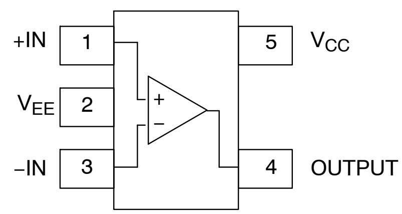


LMV301 = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

PIN CONNECTION



STYLE 3 PINOUT

ORDERING INFORMATION

See detailed ordering and shipping information in the dimensions section on page 11 of this data sheet.

MAXIMUM RATINGS

Symbol	Rating	Value	Unit
V_S	Power Supply (Operating Voltage Range V_S = 1.8 V to 5.0 V)	5.5	V
V_{IDR}	Input Differential Voltage	±Supply Voltage	V
V_{ICR}	Input Common Mode Voltage Range	−0.5 to (V+) + 0.5	V
	Maximum Input Current	10	mA
t_{So}	Output Short Circuit (Note 1)	Continuous	
T_J	Maximum Junction Temperature (Operating Range −40°C to 85°C)	150	°C
J_A	Thermal Resistance (5−Pin SC70−5)	280	°C/W
T_{stg}	Storage Temperature	−65 to 150	°C
	Mounting Temperature (Infrared or Convection (30 sec))	260	
V_{ESD}	ESD Tolerance Machine Model Human Body Model	 100 1500	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Continuous short−circuit to ground operation at elevated ambient temperature can result in exceeding the maximum allowed junction temperature of 150°C. Output currents in excess of 45 mA over long term may adversely affect reliability. Also, shorting output to V+ will adversely affect reliability; likewise shorting output to V− will adversely affect reliability.

1.8 V DC ELECTRICAL CHARACTERISTICS (Unless otherwise specified, all limits are guaranteed for T_A = 25°C, V_{CC} = 1.8 V, R_L = 1 MΩ, V_{EE} = 0 V, V_O = $V_{CC}/2$)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Offset Voltage	V_{IO}	T_A = −40°C to +85°C		1.7	9	mV
Input Offset Voltage Average Drift	T_CV_{IO}	T_A = −40°C to +85°C		5		μV/°C
Input Bias Current (Note 2)	I_B			3	35	pA
		T_A = −40°C to +85°C			50	
Common Mode Rejection Ratio	CMRR	0 V ≤ V_{CM} ≤ 0.9 V	50	63		dB
Power Supply Rejection Ratio	PSRR	1.8 V ≤ V_{CC} ≤ 5 V, V_O = 1 V, V_{CM} = 1 V	62	100		dB
Input Common−Mode Voltage Range	V_{CM}	For CMRR ≥ 50 dB	0 to 0.9	−0.2 to 0.9		V
Large Signal Voltage Gain (Note 2)	A_V	R_L = 600Ω	83	100		dB
		T_A = −40°C to +85°C	80			
		R_L = 2 kΩ	83	100		
		T_A = −40°C to +85°C	80			
Output Swing	V_{OH}	R_L = 600 Ω to 0.9 V T_A = −40°C to +85°C	1.65 1.63			V
	V_{OL}	R_L = 600 Ω to 0.9 V T_A = −40°C to +85°C		75	100 120	mV
	V_{OH}	R_L = 2 kΩ to 0.9 V T_A = −40°C to +85°C	1.5 1.4	1.76		V
	V_{OL}	R_L = 2 kΩ to 0.9 V T_A = −40°C to +85°C		25	35 40	mV
Output Short Circuit Current (Note 2)	I_O	Sourcing = V_O = 0 V Sinking = V_O = 1.8 V	10 20	60 160		mA
Supply Current	I_{CC}	T_A = −40°C to +85°C			185	μA

1.8 V AC ELECTRICAL CHARACTERISTICS (Unless otherwise specified, all limits are guaranteed for T_A = 25°C, V_{CC} = 1.8 V, R_L = 1 MΩ, V_{EE} = 0 V, V_O = $V_{CC}/2$)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Slew Rate	S_R			1		V/μs
Gain Bandwidth Product	GBWP	C_L = 200 pF		1		MHz
Phase Margin	Θ_m			60		°
Gain Margin	G_m			10		dB
Input−Referred Voltage Noise	e_n	f = 50 kHz		50		$nV/\sqrt{Hz}$
Total Harmonic Distortion	THD	A_V = +1, V − 1 V_{PP}, R_L = 10 kW, f = 1 kHz		0.01		%

2. Guaranteed by design and/or characterization.

2.7 V DC ELECTRICAL CHARACTERISTICS (Unless otherwise specified, all limits are guaranteed for T_A = 25°C, V_{CC} = 2.7 V, R_L = 1 MΩ, V_{EE} = 0 V, V_O = V_{CC}/2)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Offset Voltage	V_{IO}	T_A = −40°C to +85°C		1.7	9	mV
Input Offset Voltage Average Drift	T_CV_{IO}	T_A = −40°C to +85°C		5		μV/°C
Input Bias Current (Note 2)	I_B			3	35	pA
		T_A = −40°C to +85°C			50	
Common Mode Rejection Ratio	CMRR	0 V ≤ V_{CM} ≤ 1.35 V	50	63		dB
Power Supply Rejection Ratio	PSRR	1.8 V ≤ V_{CC} ≤ 5 V, V_O = 1 V, V_{CM} = 1 V	62	100		dB
Input Common−Mode Voltage Range	V_{CM}	For CMRR ≥ 50 dB	0 to 1.35	−0.2 to1.35		V
Large Signal Voltage Gain (Note 2)	A_V	R_L = 600 Ω	83	100		dB
		T_A = −40°C to +85°C	80			
		R_L = 2 kΩ	83	100		
		T_A = −40°C to +85°C	80			
Output Swing	V_{OH}	R_L = 600 Ω to 1.35 V T_A = −40°C to +85°C	2.55 2.53	2.62		V
	V_{OL}	R_L = 600 Ω to 1.35 V T_A = −40°C to +85°C		78	100 280	mV
	V_{OH}	R_L = 2 kΩ to 1.35 V T_A = −40°C to +85°C	2.65 2.64	2.675		V
	V_{OL}	R_L = 2 kΩ to 1.35 V T_A = −40°C to +85°C		75	100 110	mV
Output Short Circuit Current (Note 2)	I_O	Sourcing = V_O = 0 V Sinking = V_O = 2.7 V	10 20	60 160		mA
Supply Current	I_{CC}	T_A = −40°C to +85°C			185	μA

2.7 V AC ELECTRICAL CHARACTERISTICS (Unless otherwise specified, all limits are guaranteed for T_A = 25°C, V_{CC} = 2.7 V, R_L = 1 MΩ, V_{EE} = 0 V, V_O = V_{CC}/2)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Slew Rate	S_R			1		V/μs
Gain Bandwidth Product	GBWP	C_L = 200 pF		1		MHz
Phase Margin	Θ_m			60		°
Gain Margin	G_m			10		dB
Input−Referred Voltage Noise	e_n	f = 50 kHz		50		nV/√Hz
Total Harmonic Distortion	THD	A_V = +1, V − 1 V_{PP}, R_L = 10 kW, f = 1 kHz		0.01		%

2. Guaranteed by design and/or characterization.

5.0 V DC ELECTRICAL CHARACTERISTICS (Unless otherwise specified, all limits are guaranteed for T_A = 25°C, V_{CC} = 5.0 V, R_L = 1 MΩ, V_{EE} = 0 V, V_O = V_{CC}/2)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Offset Voltage	V_{IO}	T_A = −40°C to +85°C		1.7	9	mV
Input Offset Voltage Average Drift	T_CV_{IO}	T_A = −40°C to +85°C		5		μV/°C
Input Bias Current (Note 2)	I_B			3	35	pA
		T_A = −40°C to +85°C			50	
Common Mode Rejection Ratio	CMRR	0 V ≤ V_{CM} ≤ 4 V	50	63		dB
Power Supply Rejection Ratio	PSRR	1.8 V ≤ V_{CC} ≤ 5 V, V_O = 1 V, V_{CM} = 1 V	62	100		dB
Input Common−Mode Voltage Range	V_{CM}	For CMRR ≥ 50 dB	0 to 4	−0.2 to 4.2		V
Large Signal Voltage Gain (Note 2)	A_V	R_L = 600 Ω	83	100		dB
		T_A = −40°C to +85°C	80			
		R_L = 2 kΩ	83	100		
		T_A = −40°C to +85°C	80			
Output Swing	V_{OH}	R_L = 600 Ω to 2.5 V T_A = −40°C to +85°C	4.850 4.840			V
	V_{OL}	R_L = 600 Ω to 2.5 V T_A = −40°C to +85°C			150 160	mV
	V_{OH}	R_L = 2 kΩ to 2.5 V T_A = −40°C to +85°C	4.935 4.900			V
	V_{OL}	R_L = 2 kΩ to 2.5 V T_A = −40°C to +85°C			65 75	mV
Output Short Circuit Current (Note 2)	I_O	Sourcing = V_O = 0 V Sinking = V_O = 5 V	10 10	60 160		mA
Supply Current	I_{CC}	T_A = −40°C to +85°C			200	μA

5.0 V AC ELECTRICAL CHARACTERISTICS (Unless otherwise specified, all limits are guaranteed for T_A = 25°C, V_{CC} = 5.0 V, R_L = 1 MΩ, V_{EE} = 0 V, V_O = V_{CC}/2)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Slew Rate	S_R			1		V/μs
Gain Bandwidth Product	GBWP	C_L = 200 pF		1		MHz
Phase Margin	Θ_m			60		°
Gain Margin	G_m			10		dB
Input−Referred Voltage Noise	e_n	f = 50 kHz		50		nV/√Hz
Total Harmonic Distortion	THD	A_V = +1, V − 1 V_{PP}, R_L = 10 kW, f = 1 kHz		0.01		%

2. Guaranteed by design and/or characterization.

TYPICAL CHARACTERISTICS

(T_A = 25°C and V_S = 5 V unless otherwise specified)

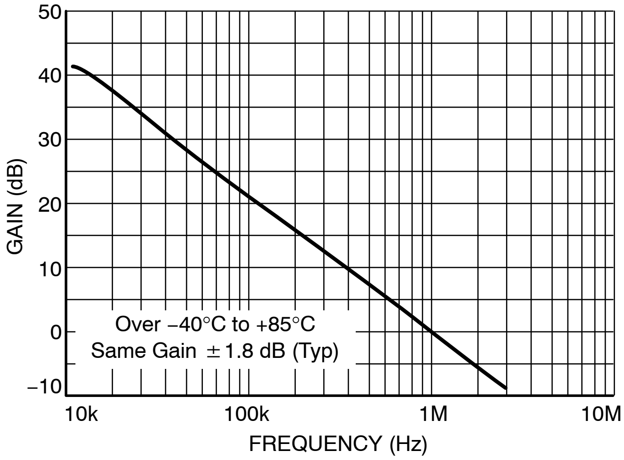


Figure 1. Open Loop Frequency Response (R_L = 2 kΩ, T_A = 25°C, V_S = 5 V)

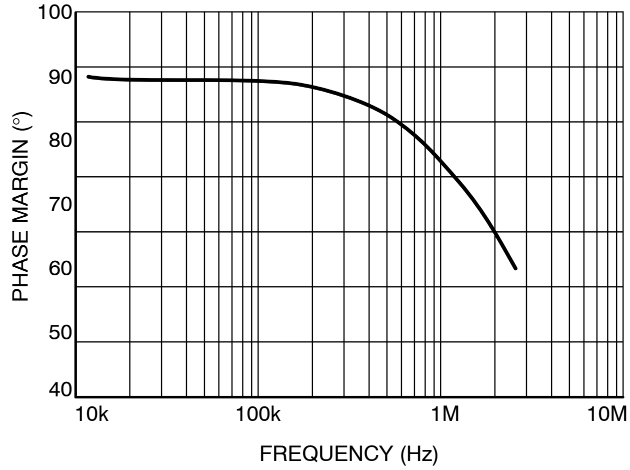


Figure 2. Open Loop Phase Margin (R_L = 2 kΩ, T_A = 25°C)

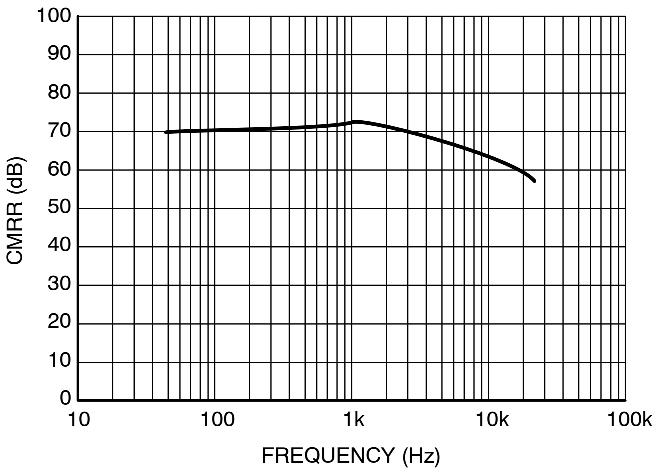


Figure 3. CMRR vs. Frequency (R_L = 5 kΩ, V_S = 5 V)

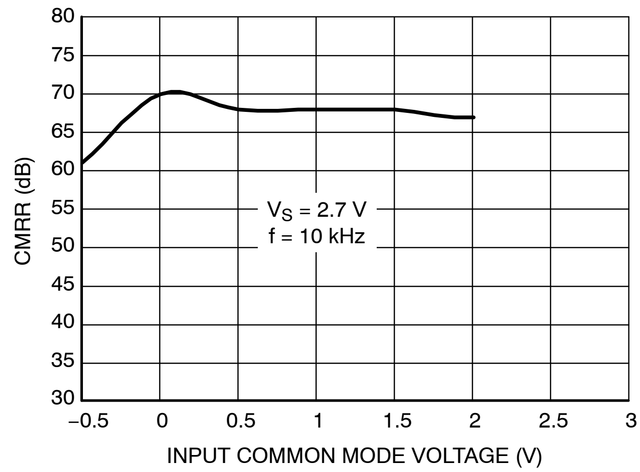


Figure 4. CMRR vs. Input Common Mode Voltage

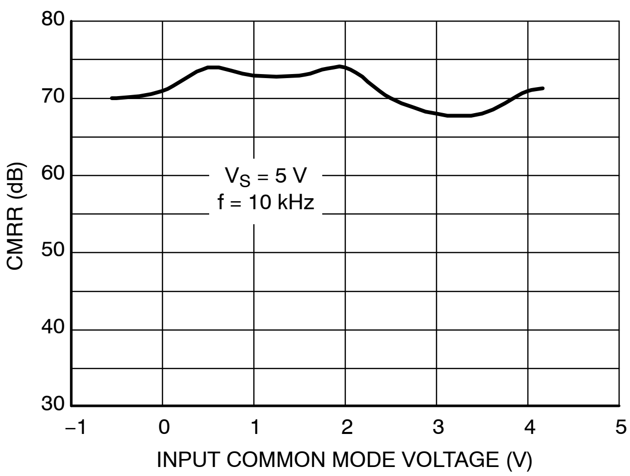


Figure 5. CMRR vs. Input Common Mode Voltage

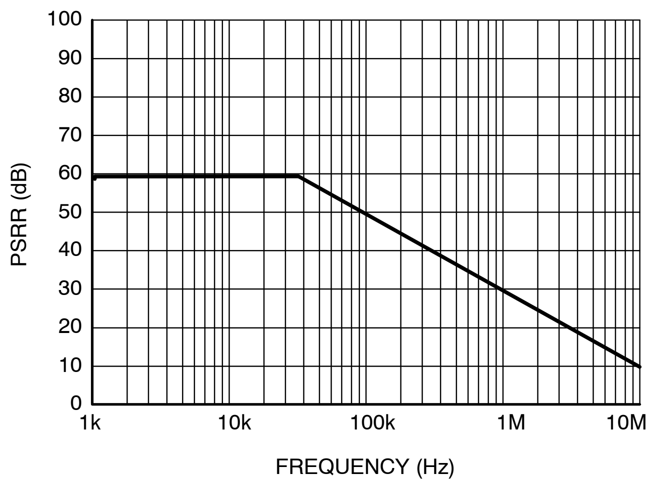


Figure 6. PSRR vs. Frequency (R_L = 5 kΩ, V_S = 2.7 V, +PSRR)

TYPICAL CHARACTERISTICS

(T_A = 25°C and V_S = 5 V unless otherwise specified)

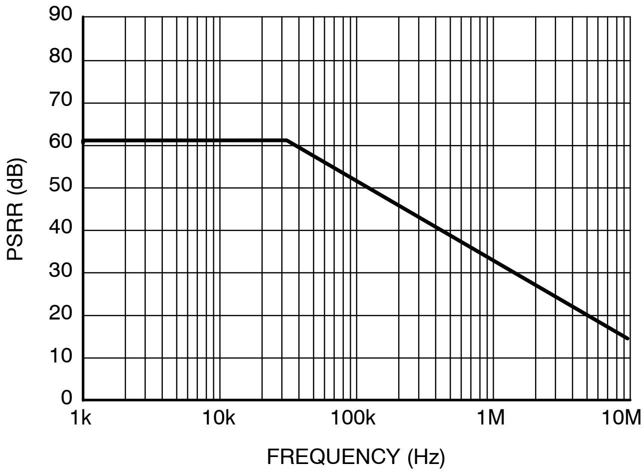


Figure 7. PSRR vs. Frequency (R_L = 5 kΩ, V_S = 2.7 V, −PSRR)

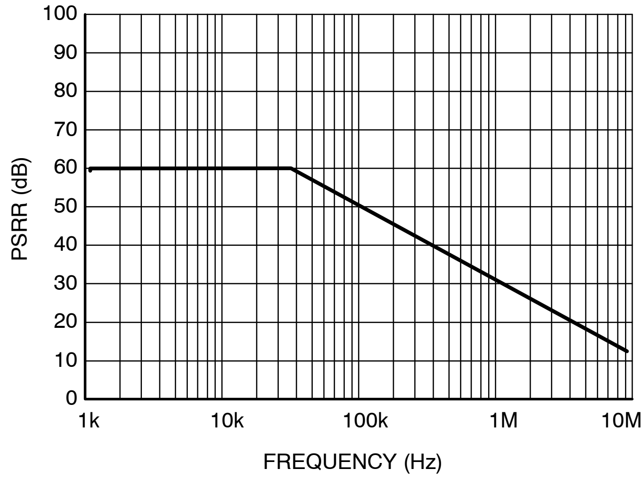


Figure 8. PSRR vs. Frequency (R_L = 5 kΩ, V_S = 5 V, +PSRR)

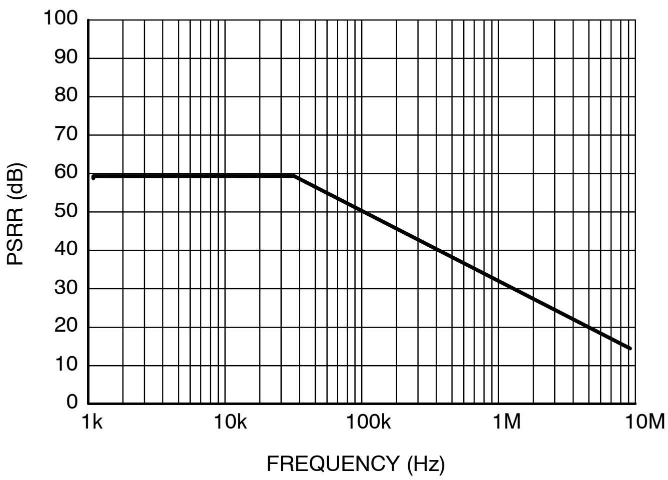


Figure 9. PSRR vs. Frequency (R_L = 5 kΩ, V_S = 5 V, −PSRR)

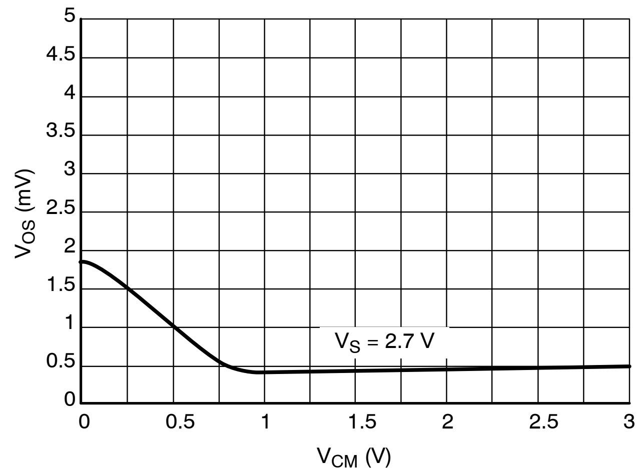


Figure 10. V_{OS} vs CMR

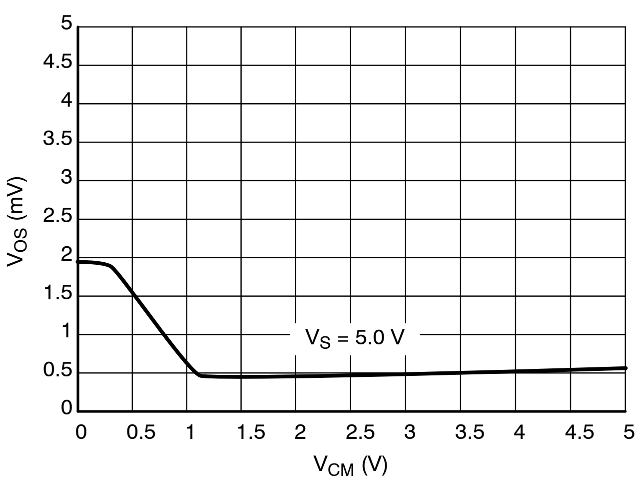


Figure 11. V_{OS} vs CMR

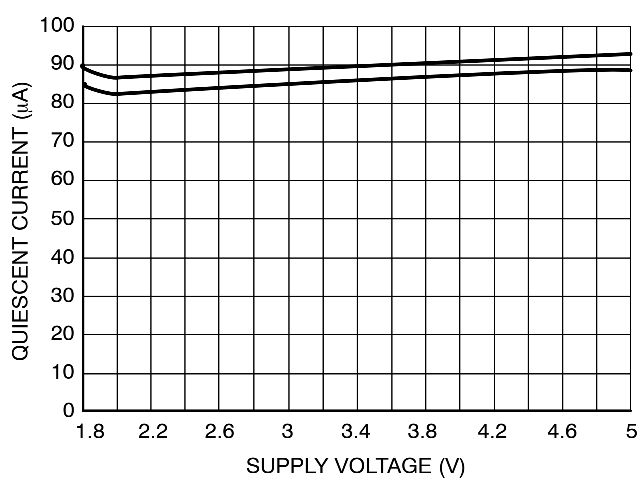


Figure 12. Supply Current vs. Supply Voltage

TYPICAL CHARACTERISTICS

(T_A = 25°C and V_S = 5 V unless otherwise specified)

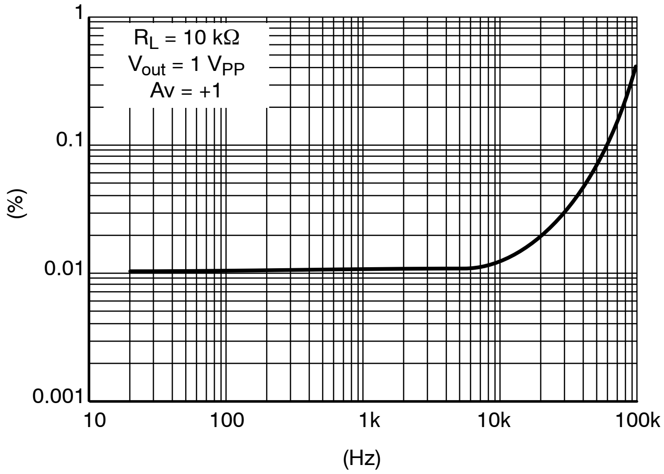


Figure 13. THD+N vs Frequency

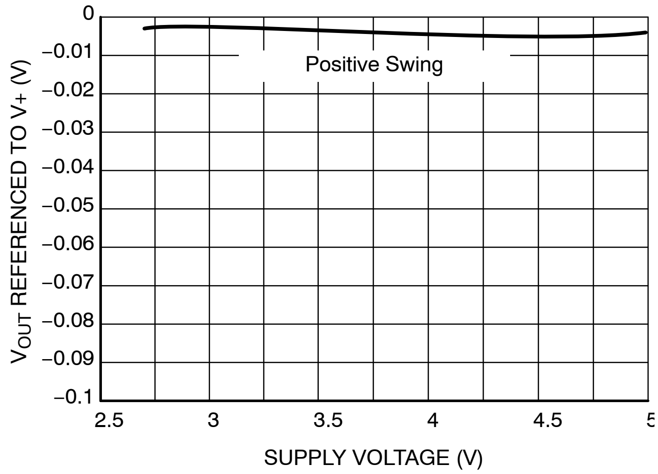


Figure 14. Output Voltage Swing vs Supply Voltage (R_L = 10k)

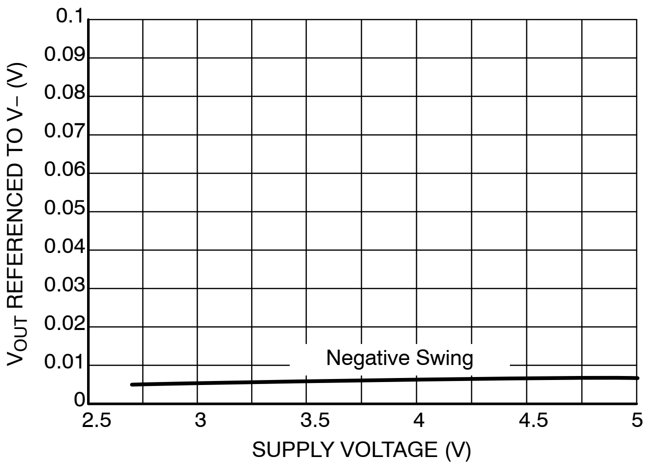


Figure 15. Output Voltage Swing vs Supply Voltage (R_L = 10k)

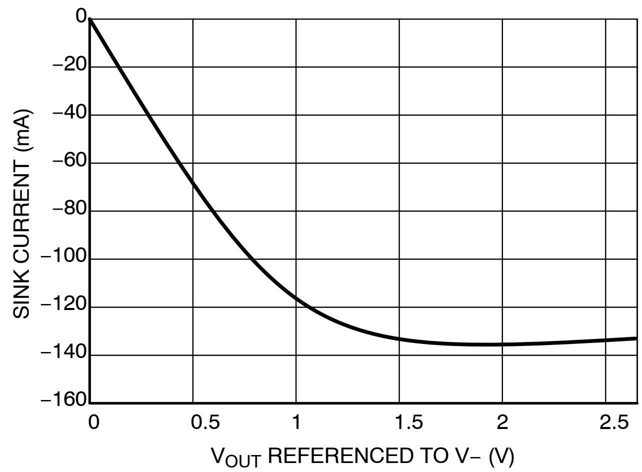


Figure 16. Sink Current vs. Output Voltage V_S = 2.7 V

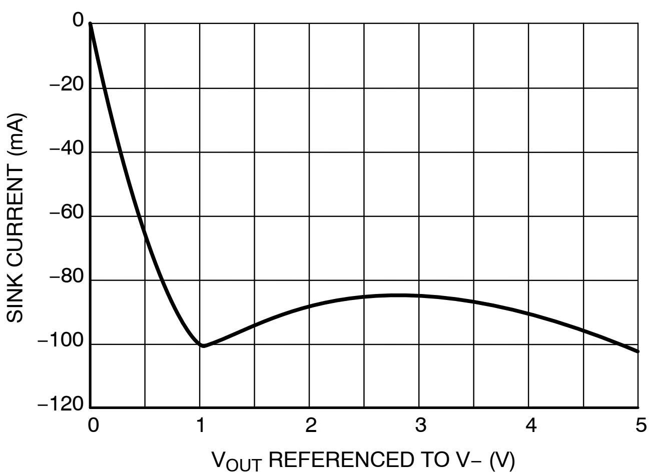


Figure 17. Sink Current vs. Output Voltage V_S = 5.0 V

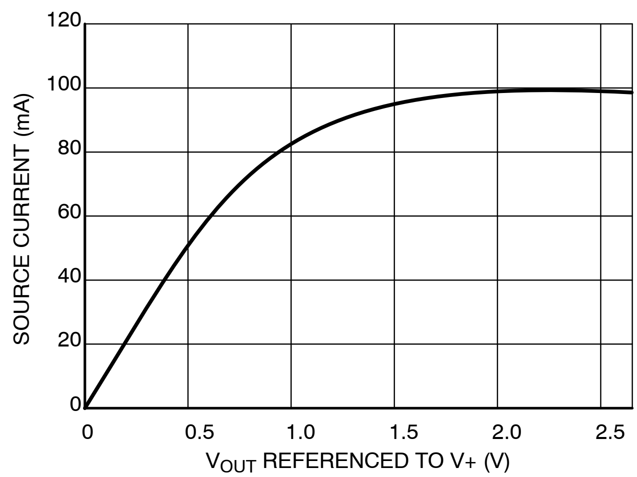


Figure 18. Source Current vs. Output Voltage V_S = 2.7 V

TYPICAL CHARACTERISTICS

(T_A = 25°C and V_S = 5 V unless otherwise specified)

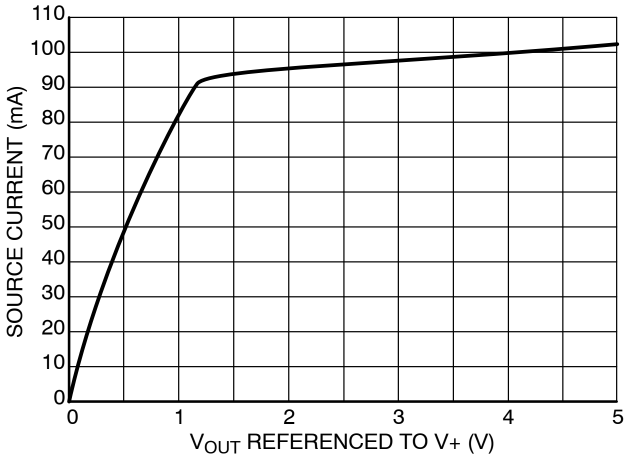


Figure 19. Source Current vs. Output Voltage V_S = 5.0 V

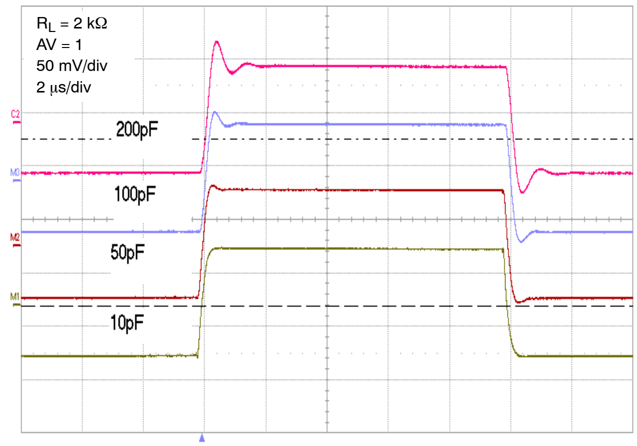


Figure 20. Settling Time vs. Capacitive Load

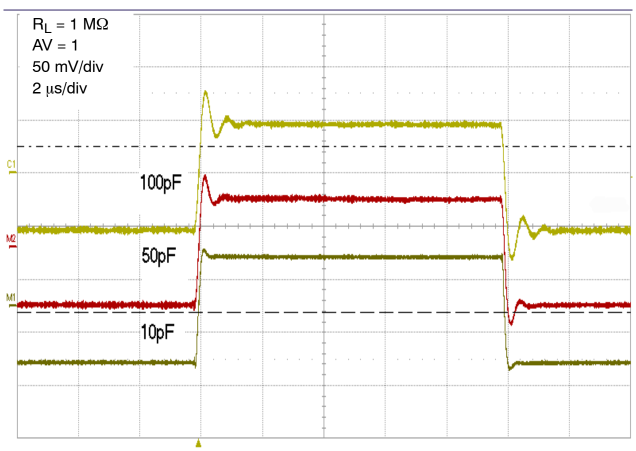


Figure 21. Settling Time vs. Capacitive Load

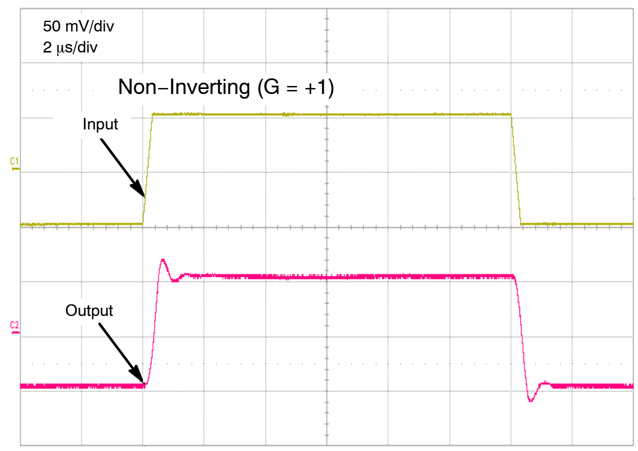


Figure 22. Step Response − Small Signal

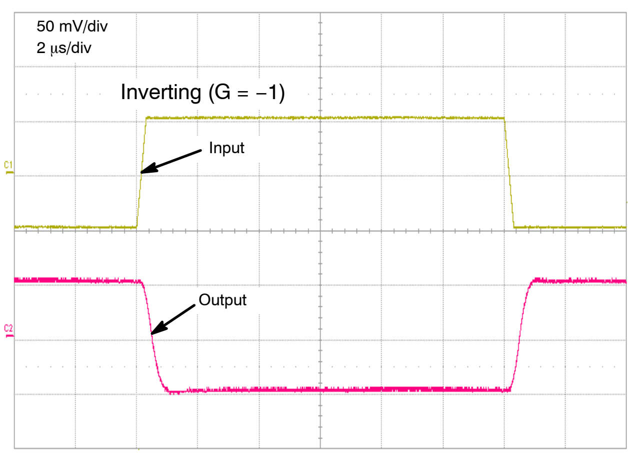


Figure 23. Step Response − Small Signal

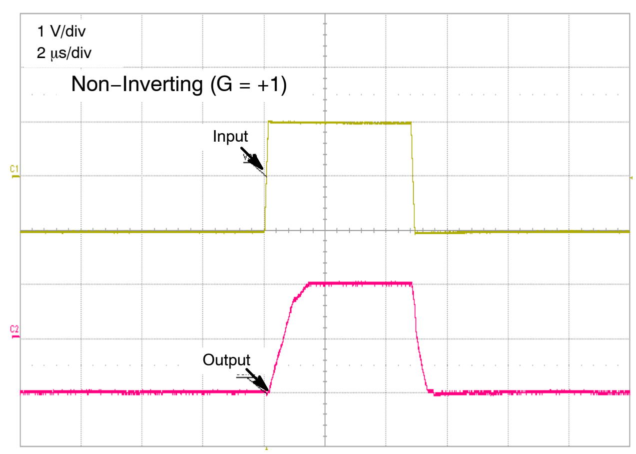


Figure 24. Step Response − Large Signal

TYPICAL CHARACTERISTICS

(T_A = 25°C and V_S = 5 V unless otherwise specified)

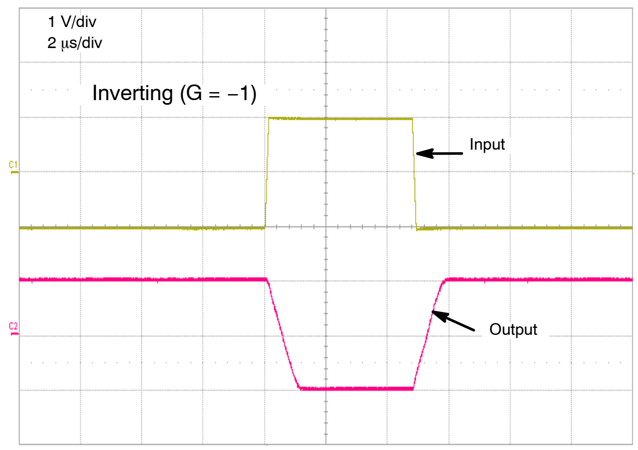
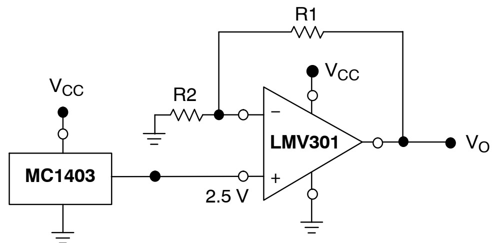


Figure 25. Step Response − Large Signal

APPLICATIONS



$$V_O = 2.5\ V(1 + \frac{R1}{R2})$$

Figure 26. Voltage Reference

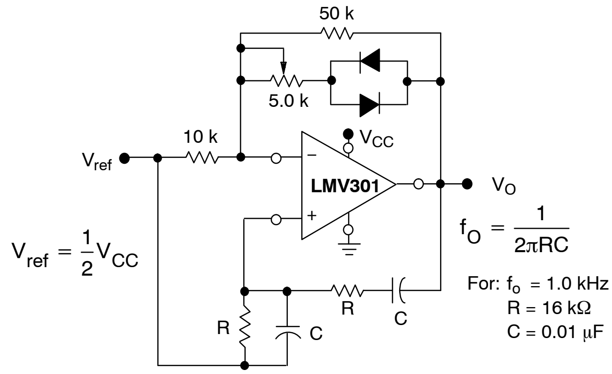
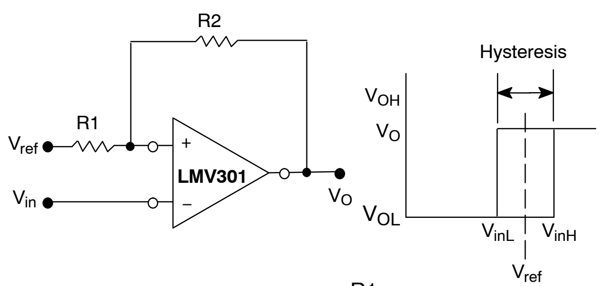


Figure 27. Wien Bridge Oscillator

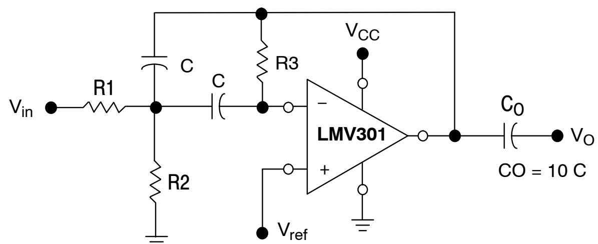


$$V_{in}L = \frac{R1}{R1 + R2}(V_{OL} - V_{ref}) + V_{ref}$$

$$V_{in}H = \frac{R1}{R1 + R2}(V_{OH} - V_{ref}) + V_{ref}$$

$$H = \frac{R1}{R1 + R2}(V_{OH} - V_{OL})$$

Figure 28. Comparator with Hysteresis



Given: f_o = center frequency
$A(f_o)$ = gain at center frequency

Choose value f_o, C

Then : $R3 = \frac{Q}{\pi f_O C}$

$$R1 = \frac{R3}{2\ A(f_O)}$$

$$R2 = \frac{R1\ R3}{4Q^2\ R1 - R3}$$

For less than 10% error from operational amplifier, $((Q_O\ f_O)/BW) < 0.1$ where f_o and BW are expressed in Hz. If source impedance varies, filter may be preceded with voltage follower buffer to stabilize filter parameters.

Figure 29. Multiple Feedback Bandpass Filter

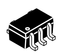
ORDERING INFORMATION

Device	Pinout Style	Marking	Package	Shipping†
LMV301SQ3T2G	Style 3	AAD	SC70−5 (Pb−Free)	3000 / Tape & Reel

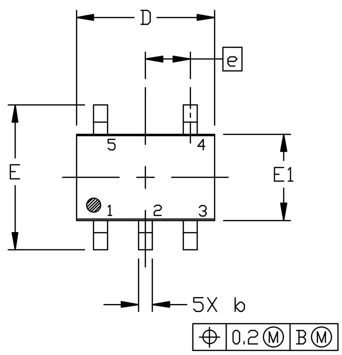
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

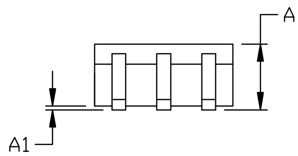
SC−88A (SC−70−5/SOT−353)
CASE 419A−02
ISSUE M

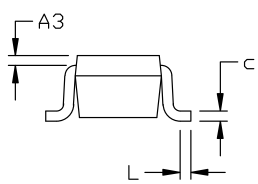
DATE 11 APR 2023



SCALE 2:1

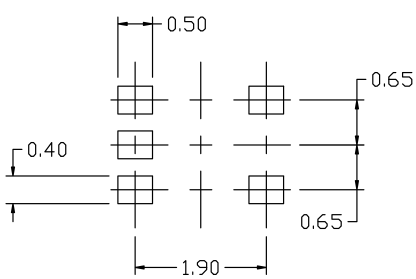






NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. 419A-01 OBSOLETE. NEW STANDARD 419A-02
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.1016MM PER SIDE.

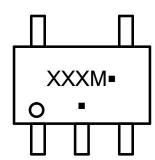
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.95	1.10
A1	---	---	0.10
A3	0.20 REF		
b	0.10	0.20	0.30
c	0.10	---	0.25
D	1.80	2.00	2.20
E	2.00	2.10	2.20
E1	1.15	1.25	1.35
e	0.65 BSC		
L	0.10	0.15	0.30



RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

STYLE 1:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. EMITTER
3. BASE
4. COLLECTOR
5. CATHODE

STYLE 3:
PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. CATHODE 1

STYLE 4:
PIN 1. SOURCE 1
2. DRAIN 1/2
3. SOURCE 1
4. GATE 1
5. GATE 2

STYLE 5:
PIN 1. CATHODE
2. COMMON ANODE
3. CATHODE 2
4. CATHODE 3
5. CATHODE 4

STYLE 6:
PIN 1. EMITTER 2
2. BASE 2
3. EMITTER 1
4. COLLECTOR
5. COLLECTOR 2/BASE 1

STYLE 7:
PIN 1. BASE
2. EMITTER
3. BASE
4. COLLECTOR
5. COLLECTOR

STYLE 8:
PIN 1. CATHODE
2. COLLECTOR
3. N/C
4. BASE
5. EMITTER

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. ANODE
5. ANODE

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

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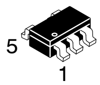
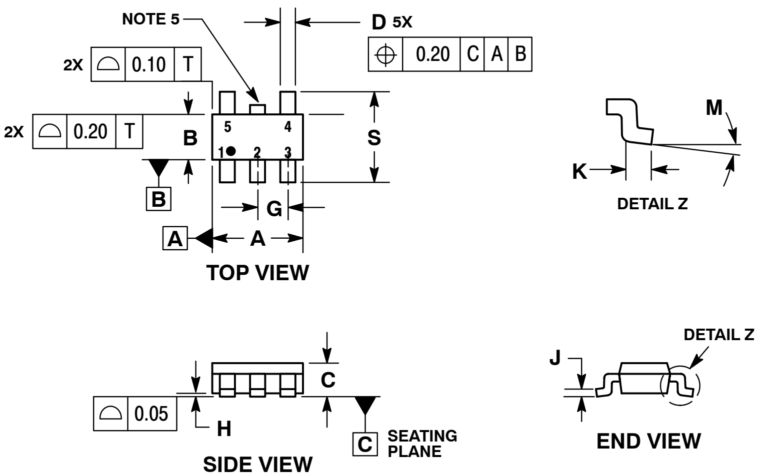
TSOP−5
CASE 483
ISSUE N



SCALE 2:1

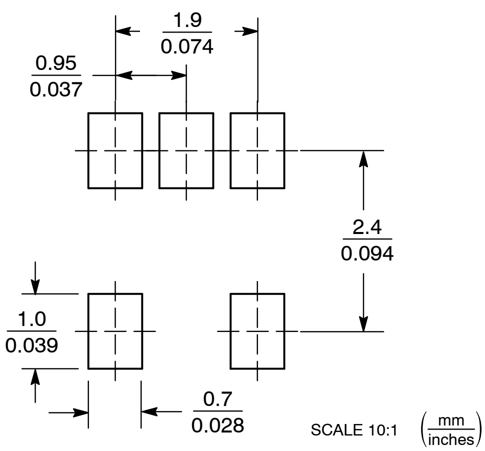
DATE 12 AUG 2020



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION A.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

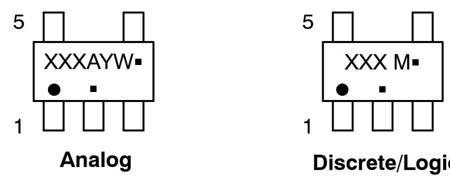
	MILLIMETERS	
DIM	MIN	MAX
A	2.85	3.15
B	1.35	1.65
C	0.90	1.10
D	0.25	0.50
G	0.95 BSC	
H	0.01	0.10
J	0.10	0.26
K	0.20	0.60
M	0 °	10 °
S	2.50	3.00

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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DESCRIPTION:	TSOP−5	PAGE 1 OF 1

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