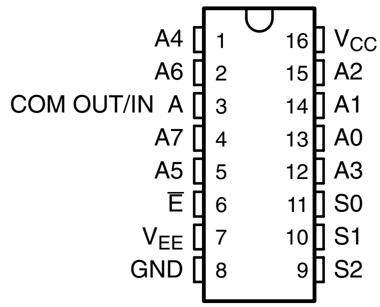
- **Qualified for Automotive Applications**
- **Wide Analog Input Voltage Range: ±5 V Max**
- **Low ON Resistance**
  - **70 Ω Typical (V_{CC} – V_{EE} = 4.5 V)**
  - **40 Ω Typical (V_{CC} – V_{EE} = 9 V)**
- **Low Crosstalk Between Switches**
- **Fast Switching and Propagation Speeds**
- **Break-Before-Make Switching**
- **Wide Operating Temperature Range: –40°C to 125°C**
- **Operation Control Voltage: 4.5 V to 5.5 V**
- **Switch Voltage: 0 V to 10 V**
- **Direct LSTTL Input Logic Compatibility: V_{IL} = 0.8 V Max, V_{IH} = 2 V Min**
- **CMOS Input Compatibility: $I_I \leq 1\ \mu A$ at V_{OL}, V_{OH}**

M PACKAGE
(TOP VIEW)



description/ordering information

This device is a digitally controlled analog switch that utilizes silicon-gate CMOS technology to achieve operating speeds similar to LSTTL, with the low power consumption of standard CMOS integrated circuits.

This analog multiplexer/demultiplexer controls analog voltages that may vary across the voltage supply range (i.e., V_{CC} to V_{EE}). It is a bidirectional switch that allows any analog input to be used as an output and vice-versa. The switch has low ON resistance and low OFF leakages. In addition, this device has an enable control that, when high, disables all switches to their OFF state.

ORDERING INFORMATION†

T_A	PACKAGE‡		ORDERABLE PART NUMBER§	TOP-SIDE MARKING
–40°C to 125°C	SOIC – M	Reel of 2500	CD74HCT4051QM96Q1	HCT4051Q

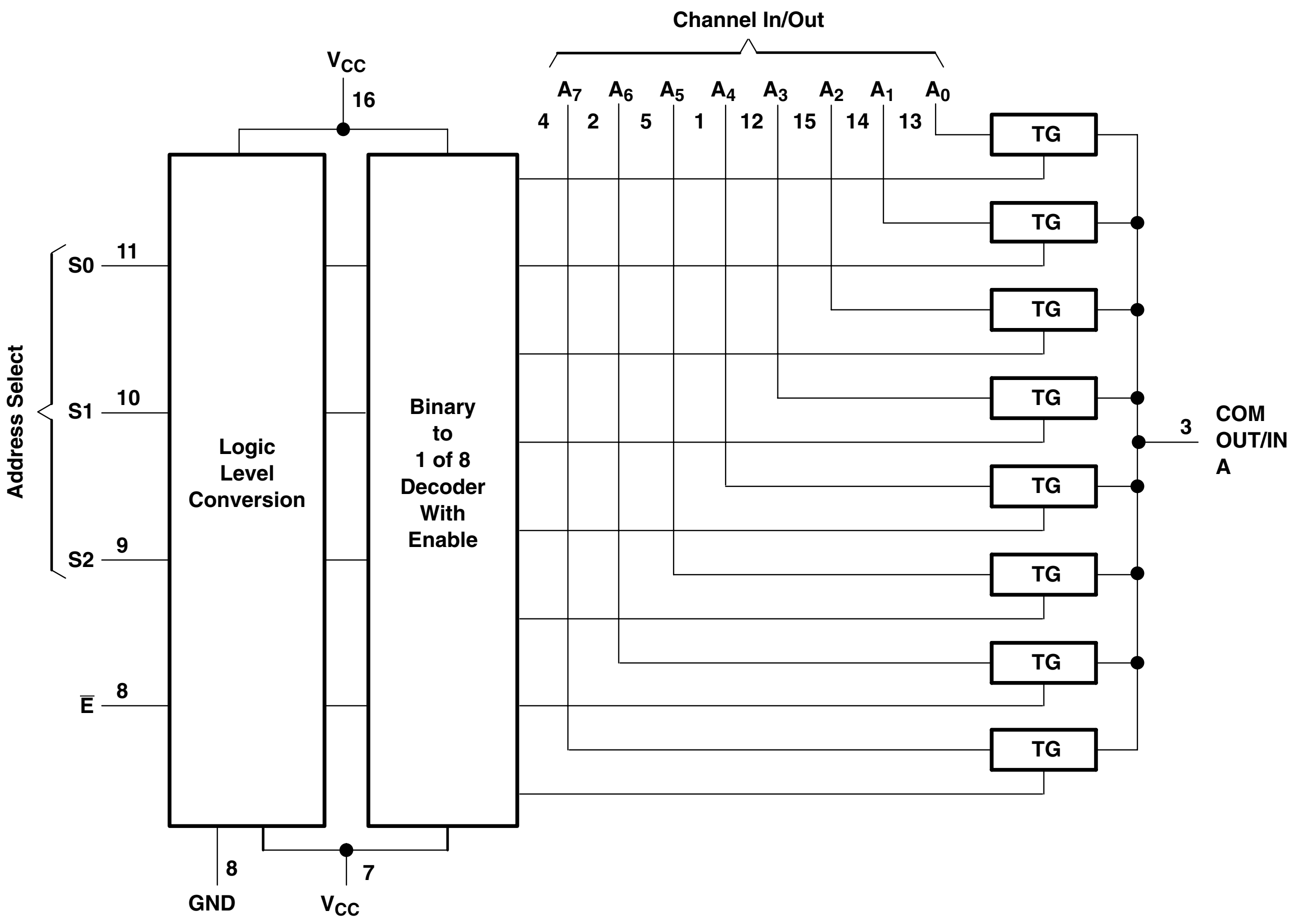
† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at http://www.ti.com.
‡ Package drawings, thermal data, and symbolization are available at http://www.ti.com/packaging.
§ The suffix 96 denotes tape and reel.

FUNCTION TABLE

INPUTS				ON CHANNELS
ENABLE	S2	S1	S0	
L	L	L	L	A0
L	L	L	H	A1
L	L	H	L	A2
L	L	H	H	A3
L	H	L	L	A4
L	H	L	H	A5
L	H	H	L	A6
L	H	H	H	A7
H	X	X	X	None

X = Don't care

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range: $V_{CC} - V_{EE}$ (see Note 1) . . . . –0.5 V to 10.5 V
V_{CC} . . . . –0.5 V to +7 V
V_{EE} . . . . 0.5 V to –7 V
Input clamp current, I_{IK} ($V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) . . . . ±20 mA
Output clamp current, I_{OK} ($V_O < V_{EE} - 0.5$ V or $V_O > V_{CC} + 0.5$ V) . . . . ±20 mA
Switch current ($V_I > V_{EE} - 0.5$ V or $V_I < V_{CC} + 0.5$ V) . . . . ±25 mA
Continuous current through V_{CC} or GND . . . . ±50 mA
V_{EE} current, I_{EE} . . . . –20 mA
Package thermal impedance, θ_{JA} (see Note 2) . . . . 73°C/W
Maximum junction temperature, T_J . . . . 150°C
Lead temperature (during soldering):
At distance 1/16 ± 1/32 inch (1,59 ± 0,79 mm) from case for 10 s max . . . . 300°C
Storage temperature range, T_{stg} . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages referenced to GND unless otherwise specified.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		4.5	5.5	V
	Supply voltage, $V_{CC} - V_{EE}$ (see Figure 1)		2	10	V
V_{EE}	Supply voltage (see Note 4 and Figure 2)		0	–6	V
V_{IH}	High-level input voltage		2		V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input control voltage		0	V_{CC}	V
V_{IS}	Analog switch I/O voltage		V_{EE}	V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 4.5 V	0	500	ns
T_A	Operating free-air temperature		–40	125	°C

NOTES: 3. All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
4. In certain applications, the external load resistor current may include both V_{CC} and signal-line components. To avoid drawing V_{CC} current when switch current flows into the transmission gate inputs, the voltage drop across the bidirectional switch must not exceed 0.6 V (calculated from r_{on} values shown in electrical characteristics table). No V_{CC} current flows through R_L if the switch current flows into the COM OUT/IN A terminal.

recommended operating area as a function of supply voltages

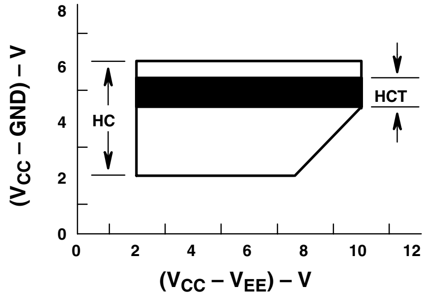


Figure 1

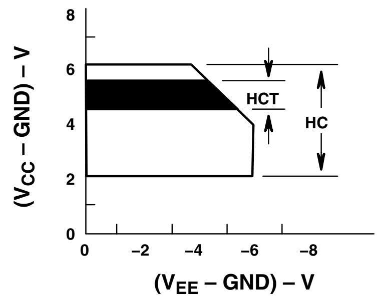


Figure 2

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{EE}	V_{CC}	T_A = 25°C			T_A = –40°C TO 125°C		UNIT
					MIN	TYP	MAX	MIN	MAX	
r_{on}	I_O = 1 mA, $V_I = V_{IH}$ or V_{IL}, See Figure 9	$V_{IS} = V_{CC}$ or V_{EE}	0 V	4.5 V		70	160		240	Ω
			–4.5 V	4.5 V		40	120		180	
		$V_{IS} = V_{CC}$ to V_{EE}	0 V	4.5 V		90	180		270	
			–4.5 V	4.5 V		45	130		195	
Δr_{on}	Between any two channels		0 V	4.5 V		10				Ω
			–4.5 V	4.5 V		5				
I_{IZ}	For switch OFF: When $V_{IS} = V_{CC}$, $V_{OS} = V_{EE}$; When $V_{IS} = V_{EE}$, $V_{OS} = V_{CC}$ For switch ON: All applicable combinations of V_{IS} and V_{OS} voltage levels, $V_I = V_{IH}$ or V_{IL}		0 V	6 V			±0.2		±2	μA
			–5 V	5 V			±0.4		±4	
I_{IL}	$V_I = V_{CC}$ or GND	Control input		5.5 V			±0.1		±1	μA
I_{CC}	I_O = 0, $V_I = V_{CC}$ or GND	When $V_{IS} = V_{EE}$, $V_{OS} = V_{CC}$	0 V	5.5 V			8		160	μA
		When $V_{IS} = V_{CC}$, $V_{OS} = V_{EE}$	–4.5 V	5.5 V			16		320	
ΔI_{CC}	Per input pin: 1 unit load, See Note 5, $V_{IN} = V_{CC}$ – 2.1 V			4.5 V to 5.5 V		100	360		490	μA

NOTE 5: For dual-supply systems, theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT input loading

TYPE	INPUT	UNIT LOADS†
4051	All	0.5

† Unit load is ΔI_{CC} limit specified in the electrical characteristics table, e.g., 360 μA max at 25°C.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 8)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V_{EE}	V_{CC}	$T_A = 25°C$			$T_A = –40°C$ TO 125°C		UNIT
						MIN	TYP	MAX	MIN	MAX	
t_{pd}	IN	OUT	C_L = 15 pF		5 V		4				ns
			C_L = 50 pF	0 V	4.5 V			12		18	
			C_L = 50 pF	–4.5 V	4.5 V			8		12	
t_{en}	S or $\overline{E}$	OUT	C_L = 15 pF		5 V		23				ns
			C_L = 50 pF	0 V	4.5 V			55		83	
			C_L = 50 pF	–4.5 V	4.5 V			39		59	
t_{dis}	S or $\overline{E}$	OUT	C_L = 15 pF		5 V		19				ns
			C_L = 50 pF	0 V	4.5 V			45		68	
			C_L = 50 pF	–4.5 V	4.5 V			32		48	
C_I	Control							10		10	pF

operating characteristics, V_{CC} = 5 V, T_A = 25°C, input t_r, t_f = 6 ns

PARAMETER		TYP	UNIT
C_{pd}	Power dissipation capacitance (see Note 6)	52	pF

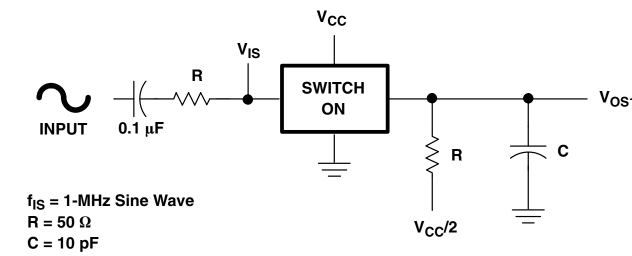
NOTE 6: C_{pd} is used to determine the dynamic power consumption (P_D), per package.
$P_D = (C_{pd} \times V_{CC}^2 \times f_I) + \Sigma (C_L + C_S) V_{CC}^2 \times f_O$
f_O = output frequency
f_I = input frequency
C_L = output load capacitance
C_S = switch capacitance
V_{CC} = supply voltage

analog channel characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{EE}	V_{CC}	TYP	UNIT
C_I	Switch input capacitance				5	pF
C_{COM}	Common output capacitance				25	pF
f_{max}	Minimum switch frequency response at –3 dB	See Figure 3 and Figure 10 and Notes 7 and 8	–2.25 V	2.25 V	145	MHz
			–4.5 V	4.5 V	180	
	Sine-wave distortion	See Figure 5	–2.25 V	2.25 V	0.035	%
			–4.5 V	4.5 V	0.018	
	$\overline{E}$ or address select (S0, S1, S2) to switch feedthrough noise	See Figure 6 and Notes 8 and 9	–2.25 V	2.25 V	TBE	mV
			–4.5 V	4.5 V	TBE	
	Switch OFF signal feedthrough	See Figure 7 and Figure 11 and Notes 8 and 9	–2.25 V	2.25 V	–73	dB
			–4.5 V	4.5 V	–75	

NOTES: 7. Adjust input voltage to obtain 0 dBm at V_{OS} for f_{IN} = 1 MHz.
8. V_{IS} is centered at $(V_{CC} – V_{EE})/2$.
9. Adjust input for 0 dBm.

PARAMETER MEASUREMENT INFORMATION



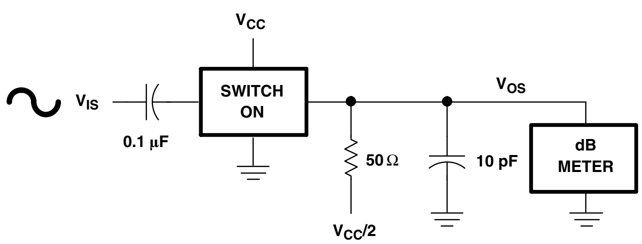


Figure 3. Frequency-Response Test Circuit

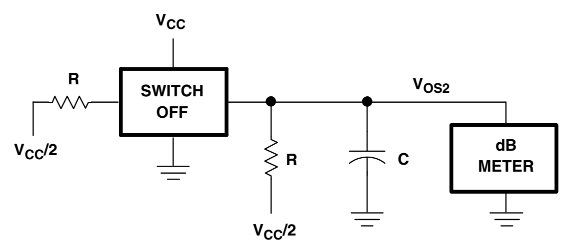


Figure 4. Crosstalk Between Two Switches Test Circuit

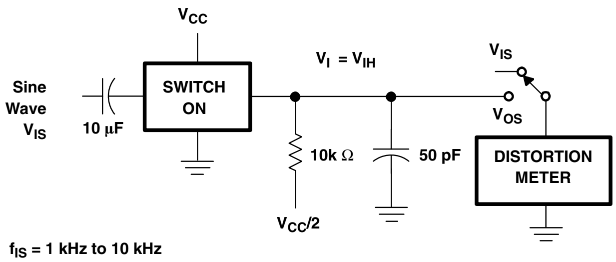


Figure 5. Sine-Wave Distortion Test Circuit

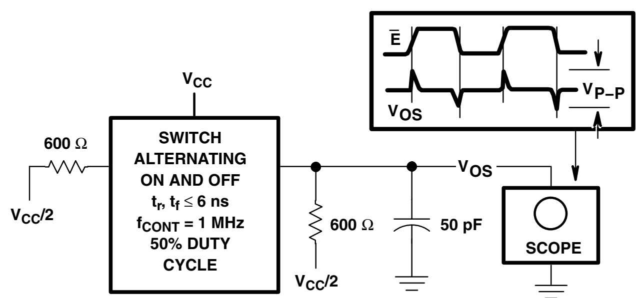


Figure 6. Control-to-Switch Feedthrough Noise Test Circuit

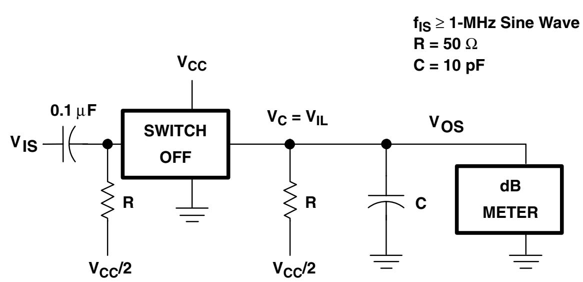
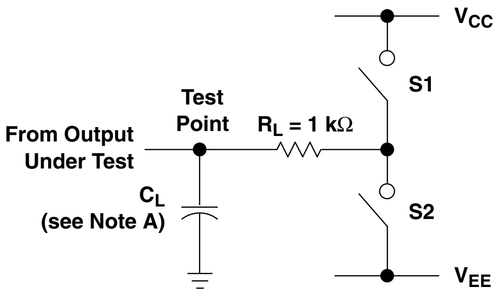


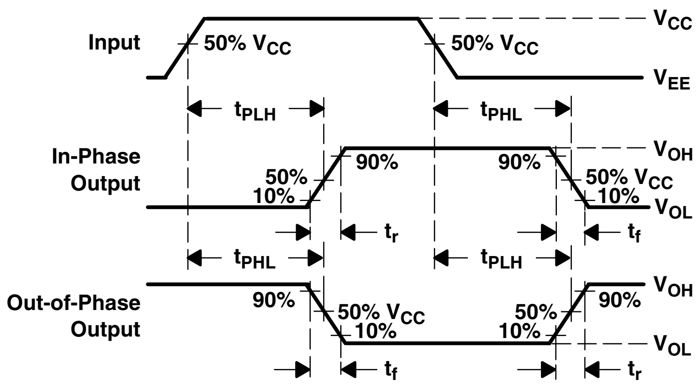
Figure 7. Switch OFF Signal Feedthrough Test Circuit

PARAMETER MEASUREMENT INFORMATION

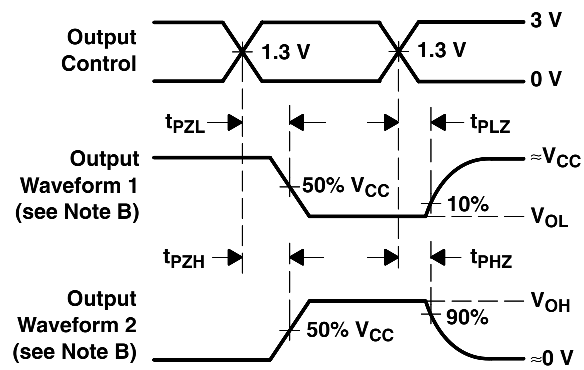


LOAD CIRCUIT

PARAMETER		S1	S2
t_{en}	t_{PZH}	Open	Closed
	t_{PZL}	Closed	Open
t_{dis}	t_{PHZ}	Open	Closed
	t_{PLZ}	Closed	Open
t_{pd}		Open	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORMS
OUTPUT ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. For clock inputs, f_{max} is measured with the input duty cycle at 50%.
E. The outputs are measured one at a time, with one input transition per measurement.
F. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
G. t_{PZL} and t_{PZH} are the same as t_{en}.
H. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 8. Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

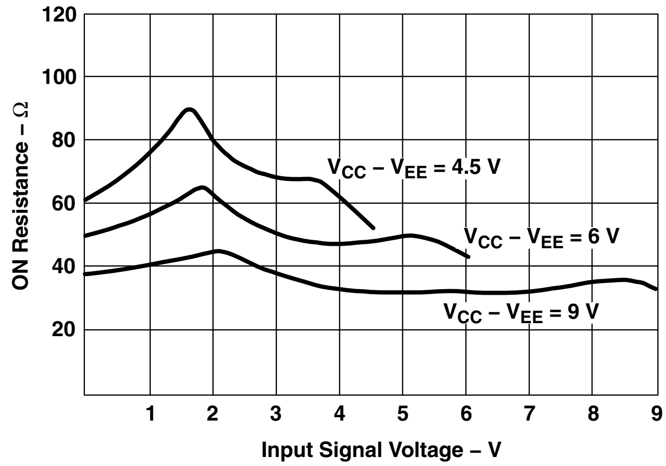


Figure 9. Typical ON Resistance vs Input Signal Voltage

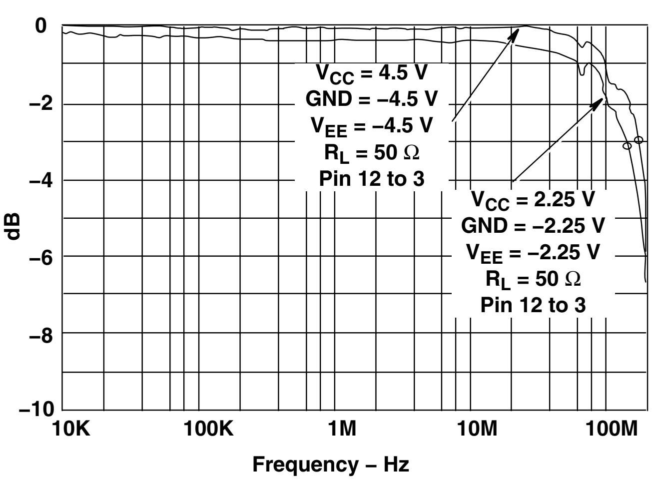


Figure 10. Channel ON Bandwidth

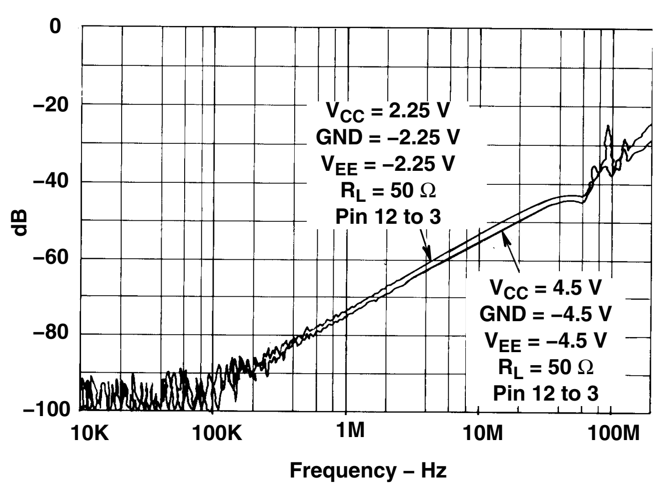


Figure 11. Channel OFF Feedthrough

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD74HCT4051QM96Q1	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCT4051Q	Samples
D24051QM96G4Q1	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCT4051Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

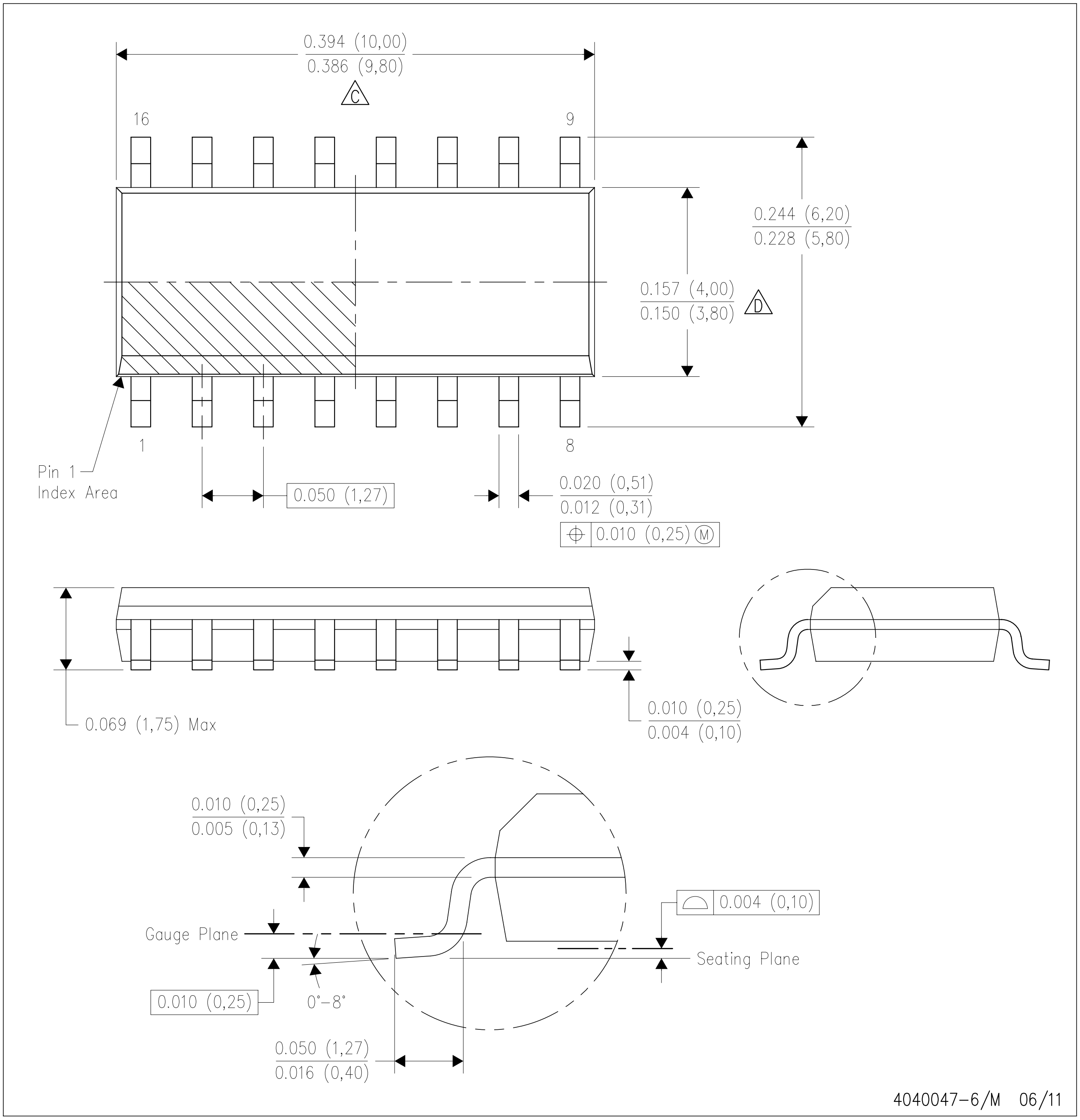
OTHER QUALIFIED VERSIONS OF CD74HCT4051-Q1 :

- Catalog: CD74HCT4051
- Military: CD54HCT4051

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AC.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265