







PCN Number:	20220125001.2		PCN Date:	Mar. 9, 2022																																				
Title:	Qualification of Carsem Suzhou as an additional Assy/Test Site for DAC7551x devices																																							
Customer Contact:	PCN Manager		Dept:	Quality Services																																				
Proposed 1st Ship Date:	Sept. 9, 2022	Estimated Sample Availability:	Date provided at sample request																																					
Change Type:	<table border="1"> <tr> <td><input checked="" type="checkbox"/></td> <td>Assembly Site</td> <td><input type="checkbox"/></td> <td>Design</td> <td><input type="checkbox"/></td> <td>Wafer Bump Site</td> </tr> <tr> <td><input type="checkbox"/></td> <td>Assembly Process</td> <td><input type="checkbox"/></td> <td>Data Sheet</td> <td><input type="checkbox"/></td> <td>Wafer Bump Material</td> </tr> <tr> <td><input checked="" type="checkbox"/></td> <td>Assembly Materials</td> <td><input type="checkbox"/></td> <td>Part number change</td> <td><input type="checkbox"/></td> <td>Wafer Bump Process</td> </tr> <tr> <td><input type="checkbox"/></td> <td>Mechanical Specification</td> <td><input checked="" type="checkbox"/></td> <td>Test Site</td> <td><input type="checkbox"/></td> <td>Wafer Fab Site</td> </tr> <tr> <td><input type="checkbox"/></td> <td>Packing/Shipping/Labeling</td> <td><input type="checkbox"/></td> <td>Test Process</td> <td><input type="checkbox"/></td> <td>Wafer Fab Materials</td> </tr> <tr> <td></td> <td></td> <td></td> <td></td> <td><input type="checkbox"/></td> <td>Wafer Fab Process</td> </tr> </table>				<input checked="" type="checkbox"/>	Assembly Site	<input type="checkbox"/>	Design	<input type="checkbox"/>	Wafer Bump Site	<input type="checkbox"/>	Assembly Process	<input type="checkbox"/>	Data Sheet	<input type="checkbox"/>	Wafer Bump Material	<input checked="" type="checkbox"/>	Assembly Materials	<input type="checkbox"/>	Part number change	<input type="checkbox"/>	Wafer Bump Process	<input type="checkbox"/>	Mechanical Specification	<input checked="" type="checkbox"/>	Test Site	<input type="checkbox"/>	Wafer Fab Site	<input type="checkbox"/>	Packing/Shipping/Labeling	<input type="checkbox"/>	Test Process	<input type="checkbox"/>	Wafer Fab Materials					<input type="checkbox"/>	Wafer Fab Process
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Product Affected:
DAC7551TDRNRQ1 DAC7551ZTDRNRQ1

**Automotive New Product Qualification Summary
(As per AEC-Q100 and JEDEC Guidelines)**

Approved 22-Jun-2020

Product Attributes

Attributes	Qual Device: <u>DAC7551ZTDRNRQ1</u>	QBS Process Reference: <u>DAC7551TDRNRQ1</u>	QBS Process Reference: <u>REF5025AODRO1/</u> <u>REF5020AODRO1</u>	QBS Process Reference: <u>REF5030AODRO1/</u> <u>REF5050AODRO1</u>
Automotive Grade Level	Grade 2	Grade 2	Grade 1	Grade 1
Operating Temp Range	-40 to +105 C	-40 to +105 C	-40 to +125 C	-40 to +125 C
Product Function	Signal Chain	Signal Chain	Power Management	Power Management
Wafer Fab Supplier	DMOS5	DMOS5	DMOS5	DMOS5
Die Revision	B	B	C	C
Assembly Site	CARZ	AP3	MLA	MLA
Package Type	USON	USON	SOIC	SOIC
Package Designator	DRN	DRN	D	D
Ball/Lead Count	12	12	8	8

- QBS: Qual By Similarity

- Qual Device DAC7551ZTDRNRQ1 is qualified at LEVEL2-260C

Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

Type	#	Test Spec	Min Lot Qty	SS/Lot	Test Name / Condition	Duration	Qual Device: <u>DAC7551ZTDRNRQ1</u>	QBS Process Reference: : <u>DAC7551TDRNRQ1</u>	QBS Process Reference: <u>REF5025AODRO1/</u> <u>REF5020AODRO1</u>	QBS Process Reference: <u>REF5030AODRO1/</u> <u>REF5050AODRO1</u>	
Test Group A – Accelerated Environment Stress Tests											
PC	A1	JEDEC J-STD-020 JESD22-A113	3	-	Preconditioning	Level 2-260C	4 Fails (1)	-	-	-	
HAST	A2	JEDEC JESD22-A110	3	77	Biased HAST, 110C/85%RH	264 Hours	3/231/0	-	-	-	
AC	A3	JEDEC JESD22-A102	3	77	Autoclave 121C	96 Hours	3/231/0	-	-	-	

Type	#	Test Spec	Min Lot Qty	SS/Lot	Test Name / Condition	Duration	Qual Device: <u>DAC7551ZT</u> <u>DRNRO1</u>	QBS Process Reference : <u>DAC7551TD</u> <u>RNRQ1</u>	QBS Process Reference: <u>REF5025AQDRO1/</u> <u>REF5020AQDRO1</u>	QBS Process Reference: <u>REF5030AQDRO1/</u> <u>REF5050AQDRO1</u>
TC	A4	JEDEC JESD22-A104 and Appendix 3	3	77	Temperature Cycle, -65/150C	500 Cycles	3/231/0	-	-	-
TC-BP	A4	MIL-STD883 Method 2011	1	50	Post Temp Cycle Bond Pull	Wires	1/50/0	-	-	-
PTC	A5	JEDEC JESD22-A105	1	45	Power Temperature Cycle	1000 Cycles	N/A	-	-	-
HTSL	A6	JEDEC JESD22-A103	1	45	High Temp Storage Bake 150C	1000 Hours	1/77/0	-	-	-
Test Group B – Accelerated Lifetime Simulation Tests										
HTOL	B1	JEDEC JESD22-A108	3	77	Life Test, 125C	408 Hours	3/231/0	-	-	-
HTOL	B1	JEDEC JESD22-A108	3	77	Life Test, 125C	1000 Hours	-	-	1/77/0	-
HTOL	B1	JEDEC JESD22-A108	3	77	Life Test, 150C	300 Hours	-	1/77/0	-	1/77/0
ELFR	B2	AEC Q100-008	3	800	Early Life Failure Rate, 125C	48 Hours	-	1/800/0	2/1600/1 (2)	-
ELFR	B2	AEC Q100-008	3	800	Early Life Failure Rate, 150C	24 Hours	-	-	-	1/800/0
EDR	B3	AEC Q100-005	3	77	NVM Endurance, Data Retention, and Operational Life	-	N/A	-	-	-
Test Group C – Package Assembly Integrity Tests										
WBS	C1	AEC Q100-001	1	30	Wire Bond Shear, Cpk	Wires	1/30/0	-	-	-

Type	#	Test Spec	Min Lot Qty	SS/Lot	Test Name / Condition	Duration	Qual Device: <u>DAC7551ZT</u> <u>DRNR01</u>	QBS Process Reference : <u>DAC7551TD</u> <u>RNR01</u>	QBS Process Reference: <u>REF5025AODRO1/</u> <u>REF5020AODRO1</u>	QBS Process Reference: <u>REF5030AODRO1/</u> <u>REF5050AODRO1</u>
					>1.67					
WBP	C2	MIL-STD883 Method 2011	1	30	Wire Bond Pull, Cpk >1.67	Wires	1/30/0	-	-	-
SD	C3	JEDEC JESD22-B102	1	15	Surface Mount Solderability	Pb Free Solder	1/15/0	-	-	-
SD	C3	JEDEC JESD22-B102	1	15	Surface Mount Solderability	Pb Solder	1/15/0	-	-	-
PD	C4	JEDEC JESD22-B100 and B108	3	10	Physical Dimensions	Cpk >1.67	3/30/0	-	-	-
Test Group D – Die Fabrication Reliability Tests										
EM	D1	JESD61	-	-	Electromigration	-	Completed Per Process Technology Requirements	-	-	-
TDDB	D2	JESD35	-	-	Time Dependent Dielectric Breakdown	-	Completed Per Process Technology Requirements	-	-	-
HCI	D3	JESD60 & 28	-	-	Hot Injection Carrier	-	Completed Per Process Technology Requirements	-	-	-
NBTI	D4	-	-	-	Negative Bias Temperature Instability	-	Completed Per Process Technology Requirements	-	-	-

Type	#	Test Spec	Min Lot Qty	SS/Lot	Test Name / Condition	Duration	Qual Device: <u>DAC7551ZT</u> <u>DRNRO1</u>	QBS Process Reference : <u>DAC7551TD</u> <u>RNRO1</u>	QBS Process Reference: <u>REF5025AQDRO1/</u> <u>REF5020AQDRO1</u>	QBS Process Reference: <u>REF5030AQDRO1/</u> <u>REF5050AQDRO1</u>
SM	D5	-	-	-	Stress Migration	-	Completed Per Process Technology Requirements	-	-	-
Test Group E – Electrical Verification Tests										
HB M	E2	AEC Q100-002	1	3	ESD - HBM	4000 V	1/3/0	-	-	-
CD M	E3	AEC Q100-011	1	3	ESD - CDM	1500 V	1/3/0	-	-	-
LU	E4	AEC Q100-004	1	6	Latch-up	Per AEC-Q100-004	1/6/0	1/6/0	-	-
ED	E5	AEC Q100-009	3	30	Electrical Distributions	Cpk >1.67	3/90/0	-	-	-

A1 (PC): Preconditioning:

Performed for THB, Biased HAST, AC, uHAST, TC & PTC samples, as applicable.

Ambient Operating Temperature by Automotive Grade Level:

Grade 0 (or E): -40°C to +150°C
Grade 1 (or Q): -40°C to +125°C
Grade 2 (or T): -40°C to +105°C
Grade 3 (or I) : -40°C to +85°C

E1 (TEST): Electrical test temperatures of Qual samples (High temperature according to Grade level):

Room/Hot/Cold : HTOL, ED
Room/Hot : THB / HAST, TC / PTC, HTSL, ELFR, ESD & LU
Room : AC/uHAST

Green/Pb-free Status:

Qualified Pb-Free(SMT) and Green

Notes/ Comments:

- (1) Damaged die due to Handling. Discounted. QEM-EVAL-2001-00270
- (2) EOS. QTS 262177-1. Discount

For questions regarding this notice, e-mails can be sent to the contacts shown below or your local Field Sales Representative.

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Europe	PCNEuropeContact@list.ti.com
Asia Pacific	PCNAsiaContact@list.ti.com
WW PCN Team	PCN_ww_admin_team@list.ti.com

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