# SN74ALVCH162260
# 12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCH WITH 3-STATE OUTPUTS

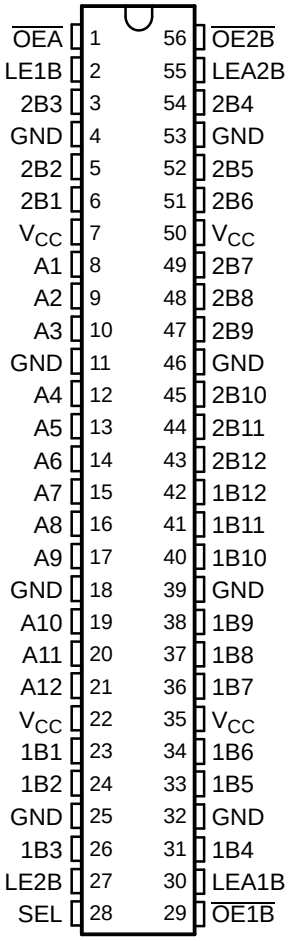
SCAS570I – MARCH 1996 – REVISED AUGUST 2004

## FEATURES

- **Member of the Texas Instruments Widebus™ Family**
- **EPIC™ (Enhanced-Performance Implanted CMOS) Submicron Process**
- **B-Port Outputs Have Equivalent 26-Ω Series Resistors, So No External Resistors Are Required**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Package Options Include Thin-Shrink Small-Outline (DGG) and Plastic Shrink Small-Outline (DL) Packages**

NOTE: For tape-and-reel order entry: The DGGR package is abbreviated to GR.

**DGG OR DL PACKAGE**
**(TOP VIEW)**




## DESCRIPTION

This 12-bit to 24-bit multiplexed D-type latch is designed for 1.65-V to 3.6-V $V_{CC}$ operation.

The SN74ALVCH162260 is used in applications in which two separate data paths must be multiplexed onto, or demultiplexed from, a single data path. Typical applications include multiplexing and/or demultiplexing address and data information in microprocessor or bus-interface applications. This device also is useful in memory-interleaving applications.

Three 12-bit I/O ports (A1-A12, 1B1-1B12, and 2B1-2B12) are available for address and/or data transfer. The output-enable ($\overline{OE1B}$, $\overline{OE2B}$, and $\overline{OEA}$) inputs control the bus transceiver functions. The $\overline{OE1B}$ and $\overline{OE2B}$ control signals also allow bank control in the A-to-B direction.

Address and/or data information can be stored using the internal storage latches. The latch-enable (LE1B, LE2B, LEA1B, and LEA2B) inputs are used to control data storage. When the latch-enable input is high, the latch is transparent. When the latch-enable input goes low, the data present at the inputs is latched and remains latched until the latch-enable input is returned high.

The B outputs, which are designed to sink up to 12 mA, include equivalent 26-Ω resistors to reduce overshoot and undershoot.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

The SN74ALVCH162260 is characterized for operation from -40°C to 85°C.

## FUNCTION TABLES

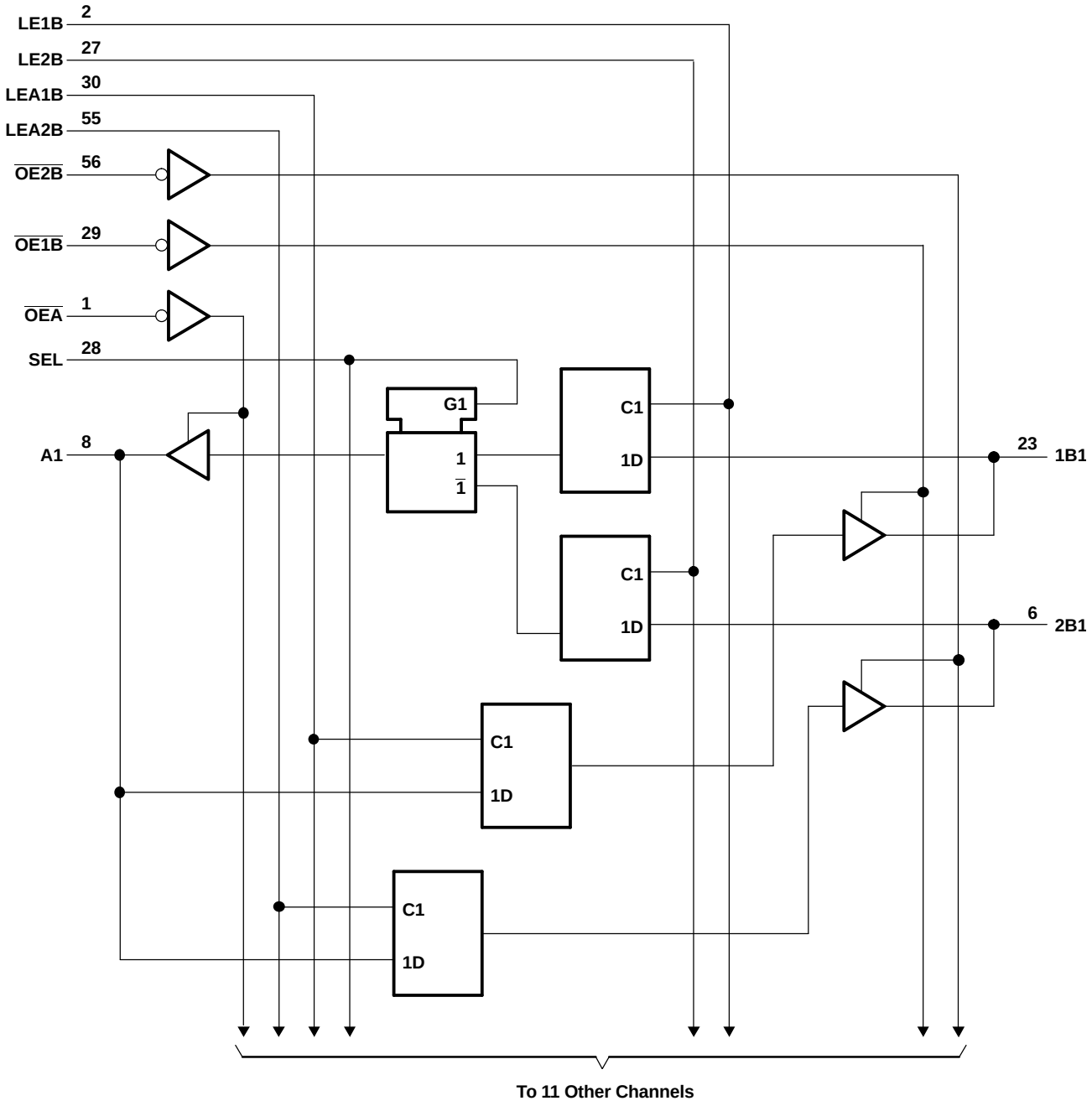
### B TO A ($\overline{OEB}$ = H)

| INPUTS | | | | | | OUTPUT |
|---|---|---|---|---|---|---|
| 1B | 2B | SEL | LE1B | LE2B | $\overline{OEA}$ | A |
| H | X | H | H | X | L | H |
| L | X | H | H | X | L | L |
| X | X | H | L | X | L | $A_0$ |
| X | H | L | X | H | L | H |
| X | L | L | X | H | L | L |
| X | X | L | X | L | L | $A_0$ |
| X | X | X | X | X | H | Z |

### A TO B ($\overline{OEA}$ = H)

| INPUTS | | | | | OUTPUTS | |
|---|---|---|---|---|---|---|
| A | LEA1B | LEA2B | $\overline{OE1B}$ | $\overline{OE2B}$ | 1B | 2B |
| H | H | H | L | L | H | H |
| L | H | H | L | L | L | L |
| H | H | L | L | L | H | $2B_0$ |
| L | H | L | L | L | L | $2B_0$ |
| H | L | H | L | L | $1B_0$ | H |
| L | L | H | L | L | $1B_0$ | L |
| X | L | L | L | L | $1B_0$ | $2B_0$ |
| X | X | X | H | H | Z | Z |
| X | X | X | L | H | Active | Z |
| X | X | X | H | L | Z | Active |
| X | X | X | L | L | Active | Active |

## LOGIC DIAGRAM (POSITIVE LOGIC)



## ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage range | | -0.5 | 4.6 | V |
| $V_I$ | Input voltage range | Except I/O ports(2) | -0.5 | 4.6 | V |
| | | I/O ports(2)(3) | -0.5 | $V_{CC}$ + 0.5 | |
| $V_O$ | Output voltage range(2)(3) | | -0.5 | $V_{CC}$ + 0.5 | V |
| $I_{IK}$ | Input clamp current | $V_I$ < 0 | | -50 | mA |
| $I_{OK}$ | Output clamp current | $V_O$ < 0 | | -50 | mA |
| $I_O$ | Continuous output current | | | ±50 | mA |
| | Continuous current through each $V_{CC}$ or GND | | | ±100 | mA |
| $\theta_{JA}$ | Package thermal impedance(4) | DGG package | | 81 | °C/W |
| | | DGV package | | 86 | |
| | | DL package | | 74 | |
| $T_{stg}$ | Storage temperature | | -65 | 150 | °C |

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) This value is limited to 4.6 V maximum.
(4) The package thermal impedance is calculated in accordance with JESD 51.

## RECOMMENDED OPERATING CONDITIONS[1]

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 1.65 | 3.6 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 1.65 V to 1.95 V | 0.65 × $V_{CC}$ | | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.7 | | |
| | | $V_{CC}$ = 2.7 V to 3.6 V | 2 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 1.65 V to 1.95 V | | 0.35 × $V_{CC}$ | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | 0.7 | |
| | | $V_{CC}$ = 2.7 V to 3.6 V | | 0.8 | |
| $V_I$ | Input voltage | | 0 | $V_{CC}$ | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | v |
| $I_{OH}$ | High-level output current (A port) | $V_{CC}$ = 1.65 V | | -4 | mA |
| | | $V_{CC}$ = 2.3 V | | -12 | |
| | | $V_{CC}$ = 2.7 V | | -12 | |
| | | $V_{CC}$ = 3 V | | -24 | |
| | High-level output current (B port) | $V_{CC}$ = 1.65 V | | -2 | |
| | | $V_{CC}$ = 2.3 V | | -6 | |
| | | $V_{CC}$ = 2.7 V | | -8 | |
| | | $V_{CC}$ = 3 V | | -12 | |
| $I_{OL}$ | Low-level output current (A port) | $V_{CC}$ = 1.65 V | | 4 | mA |
| | | $V_{CC}$ = 2.3 V | | 12 | |
| | | $V_{CC}$ = 2.7 V | | 12 | |
| | | $V_{CC}$ = 3 V | | 24 | |
| | Low-level output current (B port) | $V_{CC}$ = 1.65 V | | 2 | |
| | | $V_{CC}$ = 2.3 V | | 6 | |
| | | $V_{CC}$ = 2.7 V | | 8 | |
| | | $V_{CC}$ = 3 V | | 12 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | | 10 | ns/V |
| $T_A$ | Operating free-air temperature | | -40 | 85 | °C |

(1) All unused control inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | $V_{CC}$ | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | A port | $I_{OH}$ = -100 µA | 1.65 V to 3.6 V | $V_{CC}$ - 0.2 | | | V |
| | | $I_{OH}$ = -4 mA | 1.65 V | 1.2 | | | |
| | | $I_{OH}$ = -6 mA | 2.3 V | 2 | | | |
| | | $I_{OH}$ = -12 mA | 2.3 V | 1.7 | | | |
| | | | 2.7 V | 2.2 | | | |
| | | | 3 V | 2.4 | | | |
| | | $I_{OH}$ = -24 mA | 3 V | 2 | | | |
| | B port | $I_{OH}$ = -100 µA | 1.65 V to 3.6 V | $V_{CC}$ - 0.2 | | | |
| | | $I_{OH}$ = -2 mA | 1.65 V | 1.2 | | | |
| | | $I_{OH}$ = -4 mA | 2.3 V | 1.9 | | | |
| | | $I_{OH}$ = -6 mA | 2.3 V | 1.7 | | | |
| | | | 3 V | 2.4 | | | |
| | | $I_{OH}$ = -8 mA | 2.7 V | 2 | | | |
| | | $I_{OH}$ = -12 mA | 3 V | 2 | | | |
| $V_{OL}$ | A port | $I_{OL}$ = 100 µA | 1.65 V to 3.6 V | | | 0.2 | V |
| | | $I_{OL}$ = 4 mA | 1.65 V | | | 0.45 | |
| | | $I_{OL}$ = 6 mA | 2.3 V | | | 0.4 | |
| | | $I_{OL}$ = 12 mA | 2.3 V | | | 0.7 | |
| | | | 2.7 V | | | 0.4 | |
| | | $I_{OL}$ = 24 mA | 3 V | | | 0.55 | |
| | B port | $I_{OL}$ = 100 µA | 1.65 V to 3.6 V | | | 0.2 | |
| | | $I_{OL}$ = 2 mA | 1.65 V | | | 0.45 | |
| | | $I_{OL}$ = 4 mA | 2.3 V | | | 0.4 | |
| | | $I_{OL}$ = 6 mA | 2.3 V | | | 0.55 | |
| | | | 3 V | | | 0.55 | |
| | | $I_{OL}$ = 8 mA | 2.7 V | | | 0.6 | |
| | | $I_{OL}$ = 12 mA | 3 V | | | 0.8 | |
| $I_I$ | | $V_I = V_{CC}$ or GND | 3.6 V | | | ±5 | µA |
| $I_{I(hold)}$ | | $V_I$ = 0.58 V | 1.65 V | 25 | | | µA |
| | | $V_I$ = 1.07 V | | -25 | | | |
| | | $V_I$ = 0.7 V | 2.3 V | 45 | | | |
| | | $V_I$ = 1.7 V | | -45 | | | |
| | | $V_I$ = 0.8 V | 3 V | 75 | | | |
| | | $V_I$ = 2 V | | -75 | | | |
| | | $V_I$ = 0 to 3.6 V(2) | 3.6 V | | | ±500 | |
| $I_{OZ}$(3) | | $V_O = V_{CC}$ or GND | 3.6 V | | | ±10 | µA |
| $I_{CC}$ | | $V_I = V_{CC}$ or GND, $I_O$ = 0 | 3.6 V | | | 40 | µA |
| $\Delta I_{CC}$ | | One input at $V_{CC}$ - 0.6 V, Other inputs at $V_{CC}$ or GND | 3 V to 3.6 V | | | 750 | µA |
| $C_i$ | Control inputs | $V_I = V_{CC}$ or GND | 3.3 V | | 3.5 | | pF |
| $C_{io}$ | A or B ports | $V_O = V_{CC}$ or GND | 3.3 V | | 4.5 | | pF |

(1) All typical values are at $V_{CC}$ = 3.3 V, $T_A$ = 25°C.
(2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.
(3) For I/O ports, the parameter $I_{OZ}$ includes the input leakage current.

## TIMING REQUIREMENTS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1 through Figure 3)

| | | $V_{CC}$ = 1.8 V | | $V_{CC}$ = 2.5 V ± 0.2 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | | (1) | | 150 | | 150 | | 150 | MHz |
| $t_w$ | Pulse duration, LE1B, LE2B, LEA1B, or LEA2B high | (1) | | 3.3 | | 3.3 | | 3.3 | | ns |
| $t_{su}$ | Setup time, data before LE1B, LE2B, LEA1B, or LEA2B high or low | (1) | | 1.4 | | 1.1 | | 1.1 | | ns |
| $t_h$ | Hold time, data after LE1B, LE2B, LEA1B, or LEA2B high or low | (1) | | 1.6 | | 1.9 | | 1.5 | | ns |

(1) This information was not available at the time of publication.

## SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1 through Figure 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 1.8 V | | $V_{CC}$ = 2.5 V ± 0.2 V | | $V_{CC}$ = 2.7 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MIN | MAX | MIN | MAX | MIN | MAX | |
| $f_{max}$ | | | (1) | | 150 | | 150 | | 150 | | MHz |
| $t_{pd}$ | A | B | | (1) | 1 | 5.9 | | 5.8 | 1.2 | 4.9 | ns |
| | B | A | | (1) | 1 | 5.7 | | 5.1 | 1.2 | 4.3 | |
| | LE | A | | (1) | 1 | 5.6 | | 5.2 | 1 | 4.4 | |
| | | B | | (1) | 1 | 6.1 | | 5.9 | 1 | 5 | |
| | SEL | A | | (1) | 1 | 6.9 | | 6.6 | 1.1 | 5.6 | |
| $t_{en}$ | $\overline{OE}$ | A | | (1) | 1 | 6.7 | | 6.4 | 1 | 5.4 | ns |
| | | B | | (1) | 1 | 7.2 | | 7.1 | 1 | 6 | |
| $t_{dis}$ | $\overline{OE}$ | A | | (1) | 1 | 5.7 | | 5 | 1.3 | 4.6 | ns |
| | | B | | (1) | 1 | 6.2 | | 5.5 | 1.3 | 5.1 | |

(1) This information was not available at the time of publication.

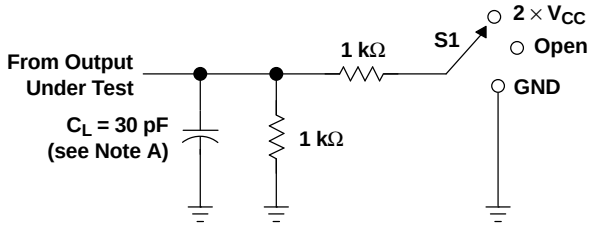
## OPERATING CHARACTERISTICS

$T_A$ = 25°C

| PARAMETER | | | TEST CONDITIONS | $V_{CC}$ = 1.8 V | $V_{CC}$ = 2.5 V | $V_{CC}$ = 3.3 V | UNIT |
|---|---|---|---|---|---|---|---|
| | | | | TYP | TYP | TYP | |
| $C_{pd}$ | Power dissipation capacitance | All outputs enabled | $C_L$ = 50 pF, f = 10 MHz | (1) | 37 | 41 | pF |
| | | All outputs disabled | | (1) | 4 | 7 | |

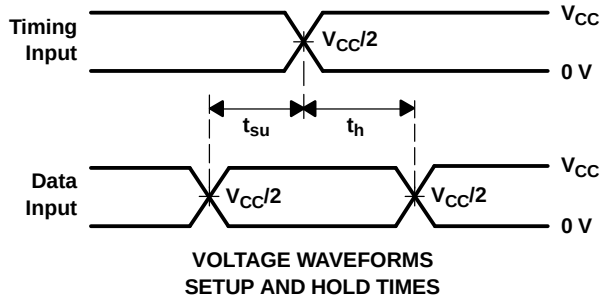
(1) This information was not available at the time of publication.

## PARAMETER MEASUREMENT INFORMATION
## $V_{CC}$ = 1.8 V

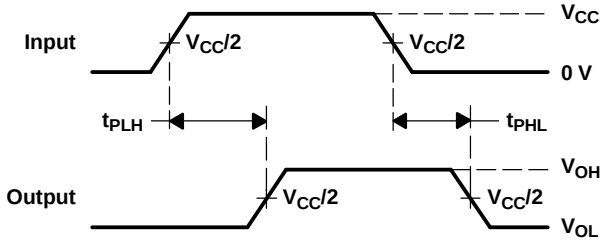



| TEST | S1 |
|---|---|
| $t_{pd}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 2 × $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |

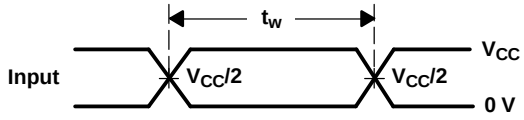
LOAD CIRCUIT



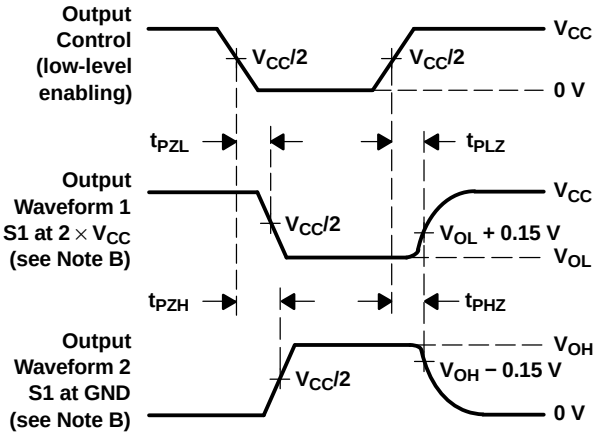

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES




VOLTAGE WAVEFORMS
PULSE DURATION

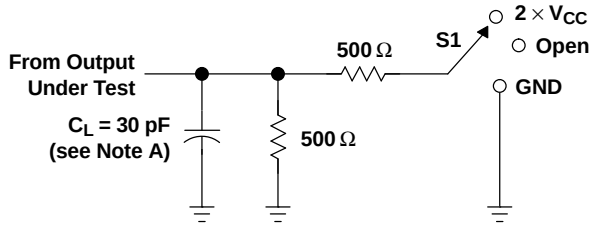



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2 ns, $t_f$ ≤ 2 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.

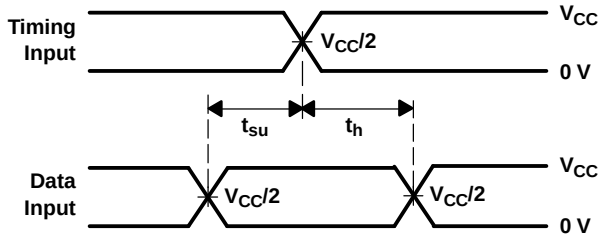
**Figure 1. Load Circuit and Voltage Waveforms**

## PARAMETER MEASUREMENT INFORMATION
## $V_{CC}$ = 2.5 V ± 0.2 V

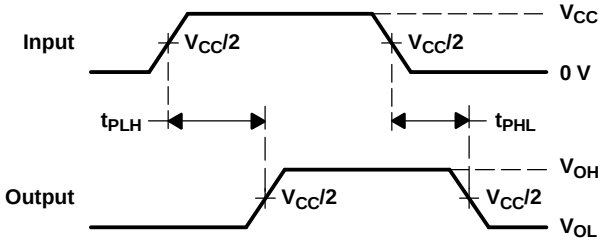



LOAD CIRCUIT

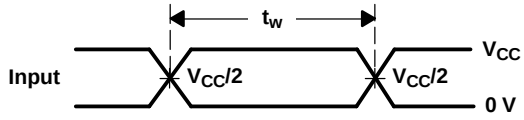
| TEST | S1 |
|---|---|
| $t_{pd}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 2 × $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |



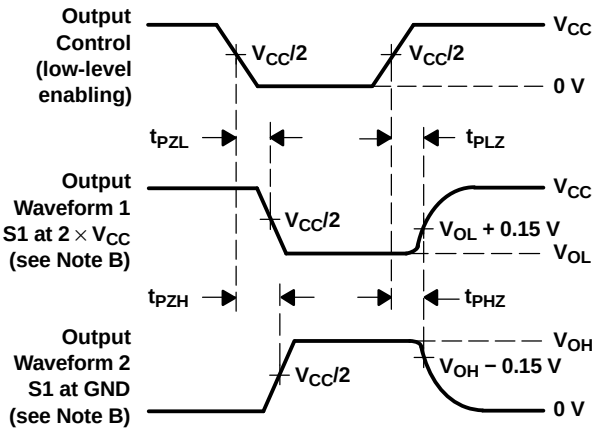

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES




VOLTAGE WAVEFORMS
PULSE DURATION

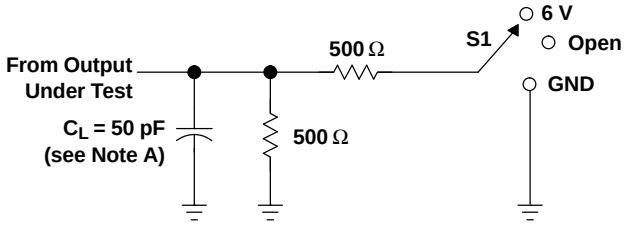



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2 ns, $t_f$ ≤ 2 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.

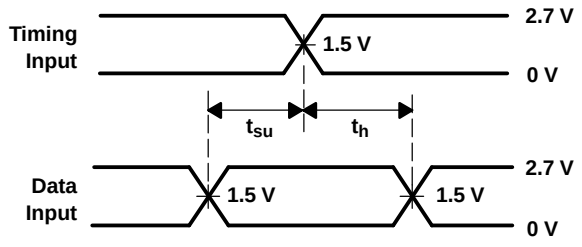
**Figure 2. Load Circuit and Voltage Waveforms**

## PARAMETER MEASUREMENT INFORMATION
## $V_{CC}$ = 2.7 V AND 3.3 V ± 0.3 V

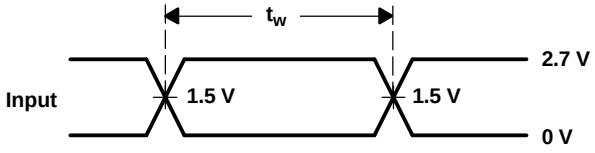



| TEST | S1 |
|---|---|
| $t_{pd}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 6 V |
| $t_{PHZ}/t_{PZH}$ | GND |

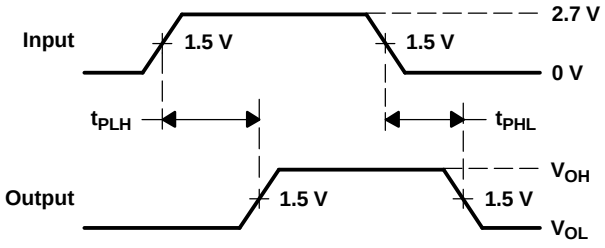
LOAD CIRCUIT



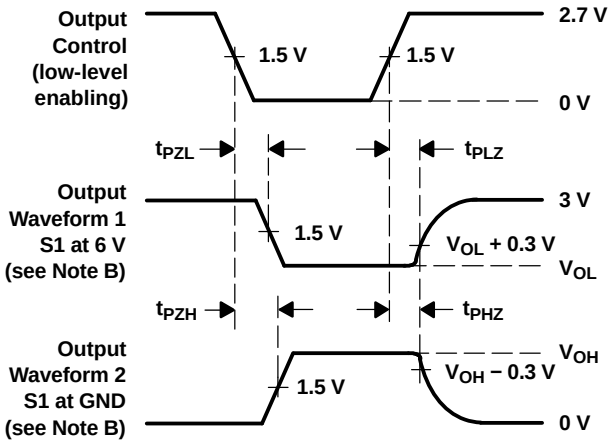

VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.

**Figure 3. Load Circuit and Voltage Waveforms**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 74ALVCH162260DLRG4 | ACTIVE | SSOP | DL | 56 | 1000 | TBD | Call TI | Call TI | -40 to 85 | | Samples |
| SN74ALVCH162260DL | ACTIVE | SSOP | DL | 56 | 20 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ALVCH162260 | Samples |
| SN74ALVCH162260DLR | ACTIVE | SSOP | DL | 56 | 1000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ALVCH162260 | Samples |
| SN74ALVCH162260GR | ACTIVE | TSSOP | DGG | 56 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | ALVCH162260 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

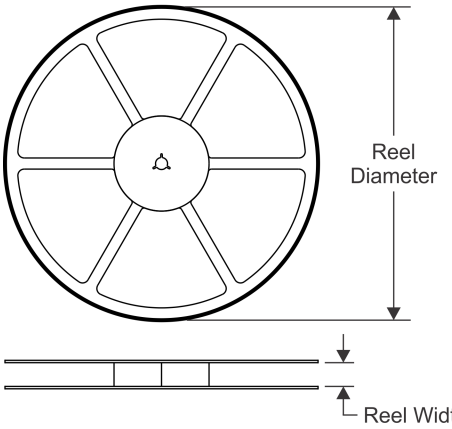
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

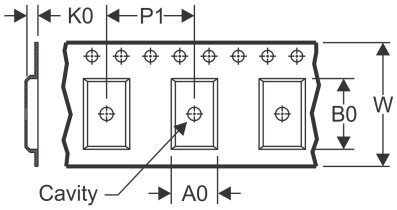
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

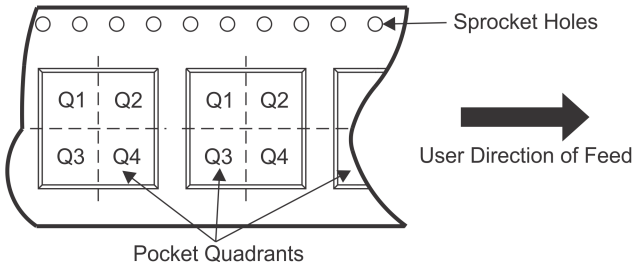



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

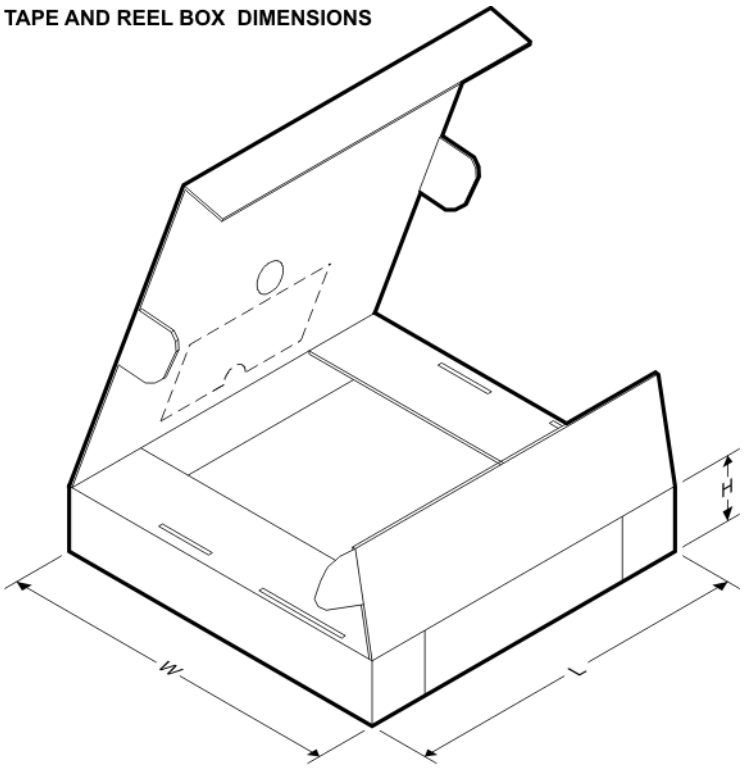
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74ALVCH162260DLR | SSOP | DL | 56 | 1000 | 330.0 | 32.4 | 11.35 | 18.67 | 3.1 | 16.0 | 32.0 | Q1 |
| SN74ALVCH162260GR | TSSOP | DGG | 56 | 2000 | 330.0 | 24.4 | 8.6 | 15.6 | 1.8 | 12.0 | 24.0 | Q1 |

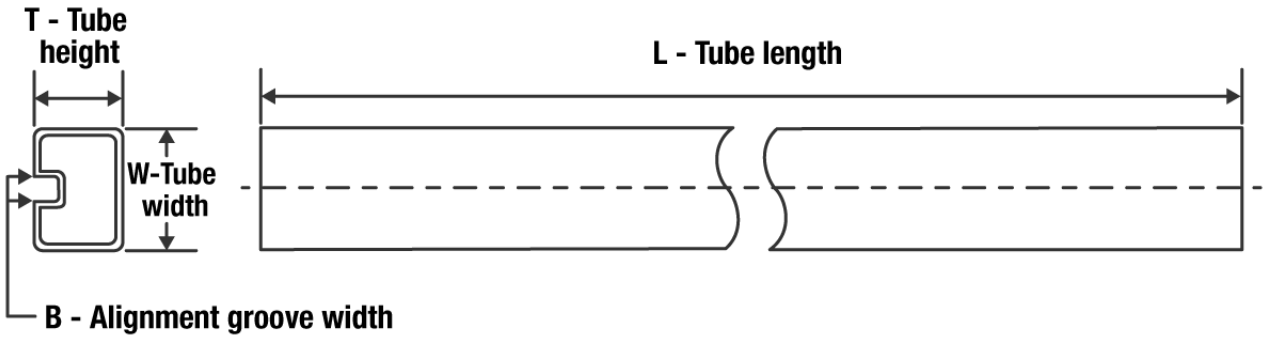
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74ALVCH162260DLR | SSOP | DL | 56 | 1000 | 367.0 | 367.0 | 55.0 |
| SN74ALVCH162260GR | TSSOP | DGG | 56 | 2000 | 367.0 | 367.0 | 45.0 |

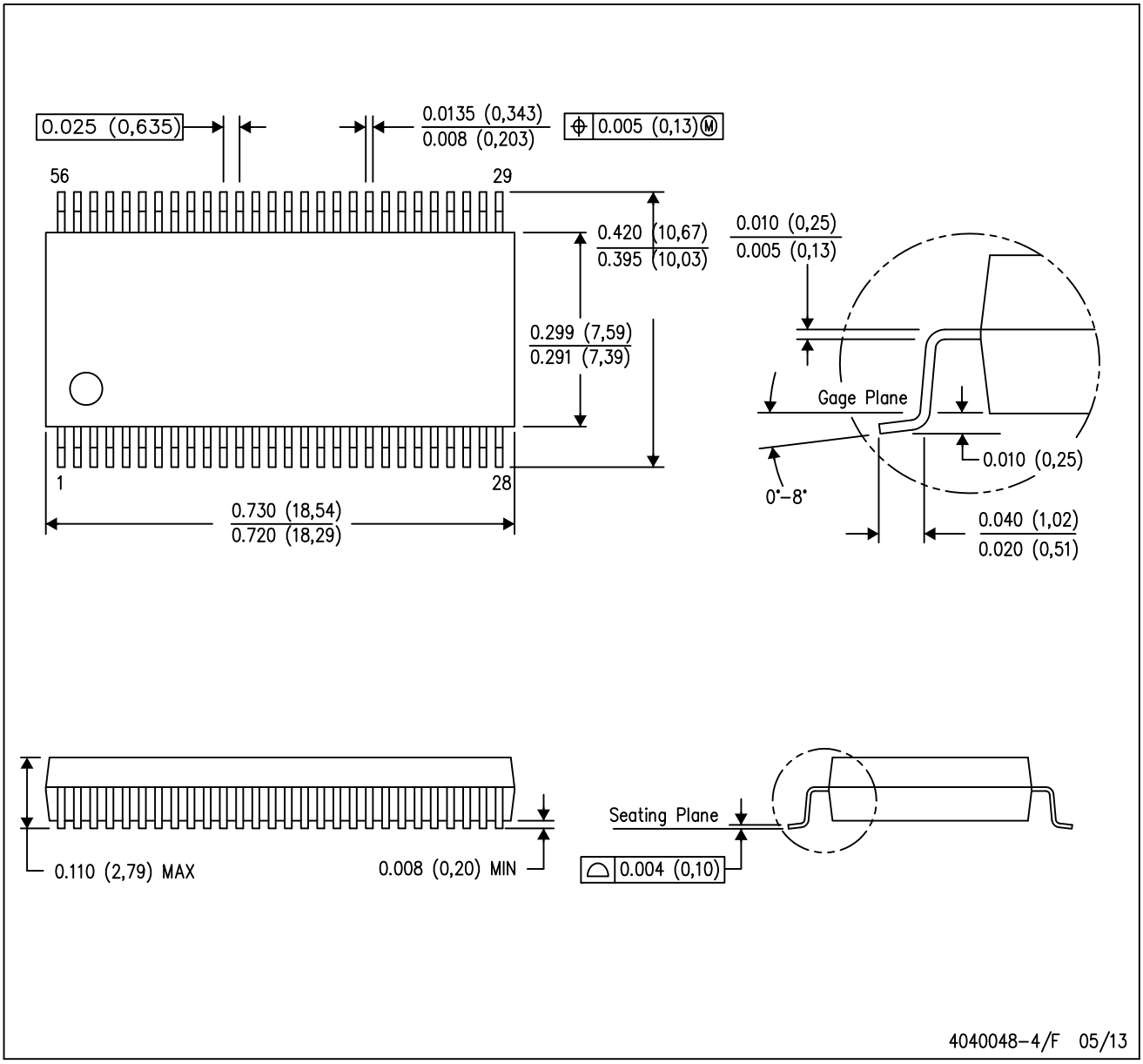
## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| SN74ALVCH162260DL | DL | SSOP | 56 | 20 | 473.7 | 14.24 | 5110 | 7.87 |

DL (R–PDSO–G56) PLASTIC SMALL–OUTLINE PACKAGE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MO–118

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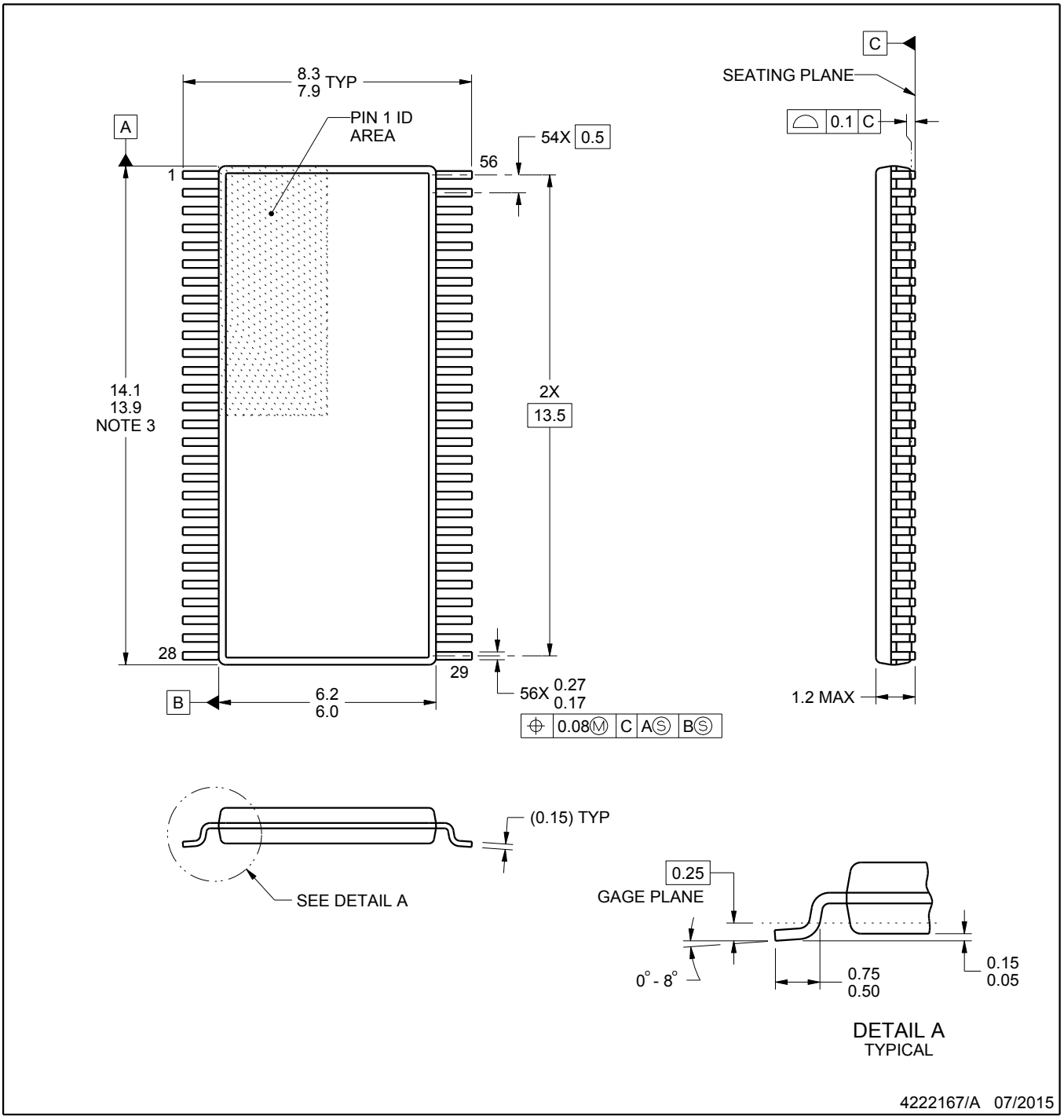
# PACKAGE OUTLINE

## DGG0056A

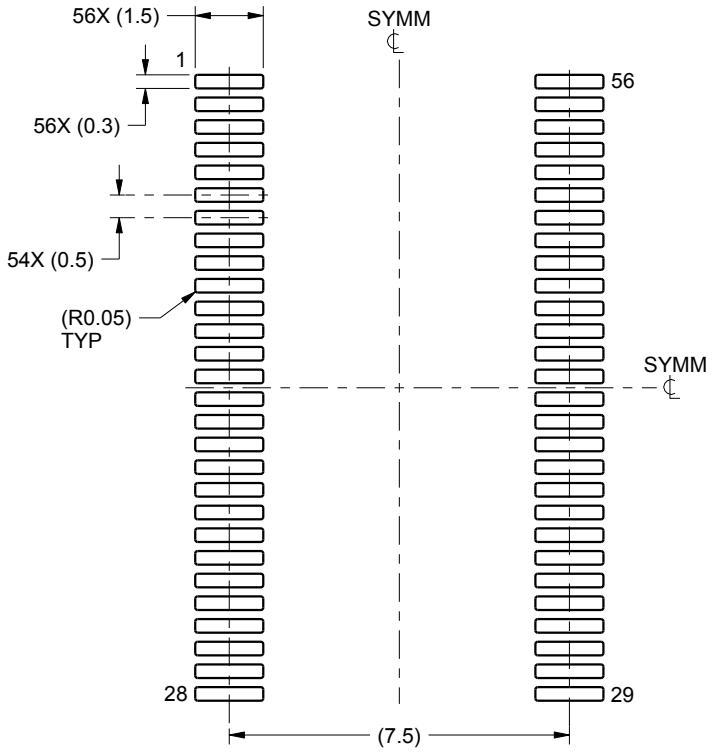
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

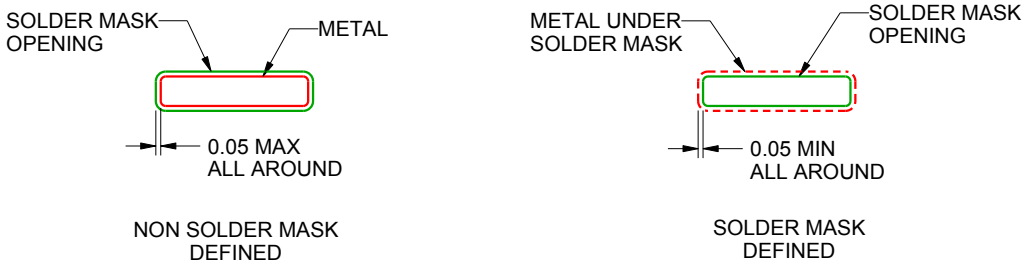



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
SCALE:6X




SOLDER MASK DETAILS

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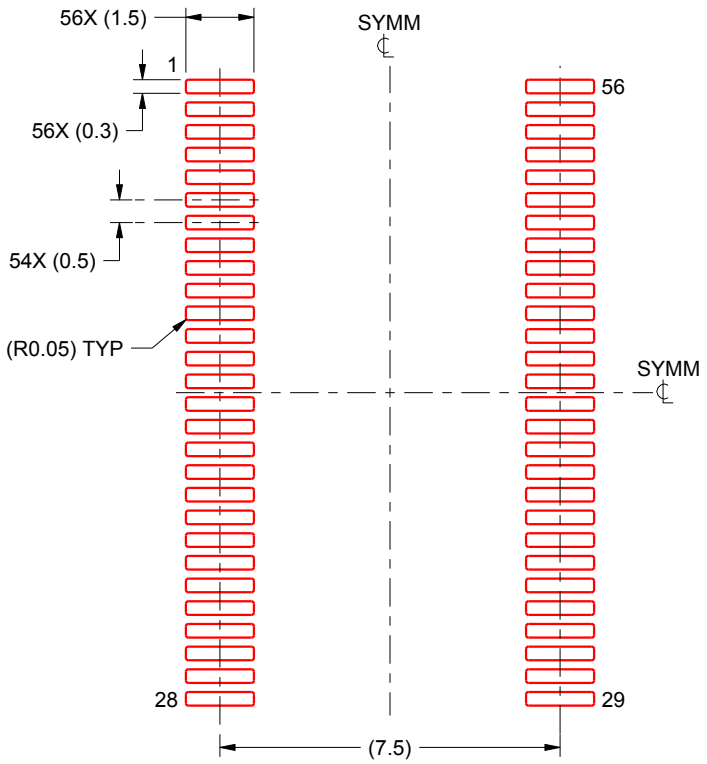
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4222167/A 07/2015

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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