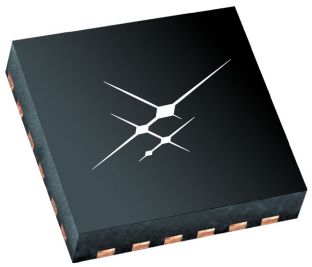
Si52131-A11A

PCI-Express Gen1, Gen2, & Gen3 Two-Output Clock Generator with 25 MHz Reference Clock & Active Low-OE Pins

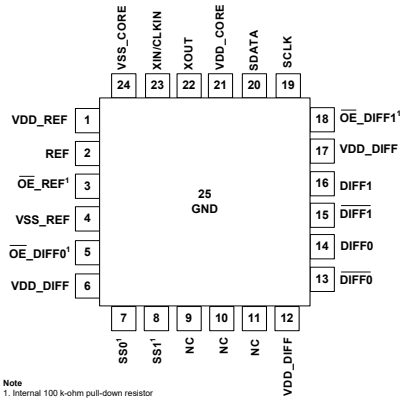
Features

- PCI-Express Gen1, Gen2 & Gen3 Compliant
- Supports Serial ATA (SATA) at 100 MHz
- Low power differential output buffers
- No termination resistors required
- Dedicated active low output enable pins for each output
- Pin selectable spread control
- Selectable frequencies: 100, 125, and 200 MHz
- Up two PCI-Express clocks
- 25 MHz reference clock
- 25 MHz Crystal Input or Clock input
- I^2C support with readback capabilities
- Triangular spread spectrum profile for maximum electromagnetic interference (EMI) reduction
- Extended Temperature –40 to 85°C
- 3.3 V Power supply
- 24-pin QFN package



Ordering Information:
See page 17

Pin Assignments



Patents pending

Applications

- Network Attached Storage
- Multi-function Printer
- Ideal for Thunderbolt applications
- Wireless Access Point
- Routers

Description

Si52131-A11A is a high-performance, PCIe clock generator that can source two PCIe clocks and a buffered 25 MHz reference clock from a 25 MHz crystal or clock input. The PCIe clock outputs are compliant to PCIe Gen 1, Gen 2, and Gen 3 specifications. The device has three active low output enable pins for enabling and disabling each output. The device features two input select pins for frequency selection and spread control. The small footprint and low power consumption makes Si52131-A11A the ideal clock solution for consumer and embedded applications.

Functional Block Diagram

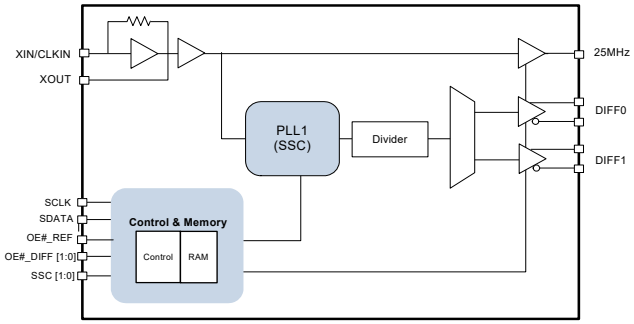


TABLE OF CONTENTS

1. Electrical Specifications

Table 1. DC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
3.3 V Operating Voltage	VDD core	3.3 ±5%	3.135	3.3	3.465	V
3.3 V Input High Voltage	V_{IH}	SS1:0	2.0	—	V_{DD} + 0.3	V
3.3 V Input Low Voltage	V_{IL}	SS1:0	V_{SS} – 0.3	—	0.8	V
Input High Voltage	V_{IHI2C}	SDATA, SCLK	2.2	—	—	V
Input Low Voltage	V_{ILI2C}	SDATA, SCLK	—	—	1.0	V
Input High Leakage Current	I_{IH}	Except internal pull-down resistors, $0 < V_{IN} < V_{DD}$	—	—	5	µA
Input Low Leakage Current	I_{IL}	Except internal pull-up resistors, $0 < V_{IN} < V_{DD}$	–5	—	—	µA
3.3 V Output High Voltage (SE)	V_{OH}	I_{OH} = –1 mA	2.4	—	—	V
3.3 V Output Low Voltage (SE)	V_{OL}	I_{OL} = 1 mA	—	—	0.4	V
High-impedance Output Current	I_{OZ}		–10	—	10	µA
Input Pin Capacitance	C_{IN}		1.5	—	5	pF
Output Pin Capacitance	C_{OUT}		—	—	6	pF
Pin Inductance	L_{IN}		—	—	7	nH
Power Down Current	I_{DD_PD}		—	—	1	mA
Dynamic Supply Current	$I_{DD\_3.3V}$	All outputs enabled. Differential clocks with 5” traces and 2 pF load. 25 MHz clock with 5” traces and 4 pF load	—	—	45	mA

Table 2. AC Electrical Specifications

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal						
Long-term Accuracy	L_{ACC}	Measured at $V_{DD}/2$ differential	—	—	250	ppm
Clock Input						
CLKIN Duty Cycle	T_{DC}	Measured at $V_{DD}/2$	47	—	53	%
CLKIN Rise/Fall Slew Rate	T_R/T_F	Measured between 0.2 V_{DD} and 0.8 V_{DD}	0.5	—	4.0	V/ns
CLKIN Cycle to Cycle Jitter	T_{CCJ}	Measured at VDD/2	—	—	250	ps
CLKIN Long Term Jitter	T_{LTJ}	Measured at VDD/2	—	—	350	ps
Input High Voltage	V_{IH}	XIN/CLKIN pin	2	—	VDD+0.3	V
Input Low Voltage	V_{IL}	XIN/CLKIN pin	—	—	0.8	V
Input High Current	I_{IH}	XIN/CLKIN pin, VIN = VDD	—	—	35	µA
Input Low Current	I_{IL}	XIN/CLKIN pin, 0 < VIN <0.8	–35	—	—	µA
DIFF at 0.7 V						
Duty Cycle	T_{DC}	Measured at 0 V differential	45	—	55	%
Cycle to Cycle Jitter	T_{CCJ}	Measured at 0 V differential	—	35	50	ps
PCIe Gen 1 Pk-Pk Jitter	Pk-Pk	PCIe Gen 1	0	40	86	ps
PCIe Gen 2 Phase Jitter	RMS_{GEN2}	10 kHz < F < 1.5 MHz	0	2	3.0	ps
		1.5 MHz < F < Nyquist	0	2	3.1	ps
PCIe Gen 3 Phase Jitter	RMS_{GEN3}	Includes PLL BW 2–4 MHz, CDR = 10 MHz	0	0.5	1.0	ps
Long Term Accuracy	L_{ACC}	Measured at 0 V differential	—	—	100	ppm
Rise/Fall Slew Rate	T_R/T_F	Measured differentially from ±150 mV	1	—	8	V/ns
Voltage High	V_{HIGH}		—	—	1.15	V
Voltage Low	V_{LOW}		–0.3	—	—	V
Crossing Point Voltage at 0.7 V Swing	V_{OX}		300	—	550	mV
Spread Range	SPR-2	Down spread	—	–0.5	—	%
Modulation Frequency	F_{MOD}		30	31.5	33	kHz
REF at 3.3 V						
Duty Cycle	T_{DC}	Measurement at 1.5 V	45	—	55	%
Rise/Fall Slew Rate	T_R / T_F	Measured between 0.8 and 2.0 V	1.0	—	4.0	V/ns
Cycle to Cycle Jitter	T_{CCJ}	Measurement at 1.5 V	—	—	300	ps
Long Term Accuracy	L_{ACC}	Measured at 1.5 V	—	—	100	ppm
Enable/Disable and Setup						
Clock Stabilization from Power-up	T_{STABLE}		—	—	1.8	ms
Stopclock Setup Time	T_{SS}		10.0	—	—	ns
Note: Visit www.pcisig.com for complete PCIe specifications.						

Table 3. Absolute Maximum Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Main Supply Voltage	$V_{DD\_3.3V}$	Functional	—	—	4.6	V
Input Voltage	V_{IN}	Relative to V_{SS}	–0.5	—	4.6	V_{DC}
Temperature, Storage	T_S	Non-functional	–65	—	150	°C
Temperature, Operating Ambient	T_A	Functional	–40	—	85	°C
Temperature, Junction	T_J	Functional	—	—	150	°C
Dissipation, Junction to Case	$Ø_{JC}$	JEDEC (JESD 51)	—	—	20	°C/W
Dissipation, Junction to Ambient	$Ø_{JA}$	JEDEC (JESD 51)	—	—	60	°C/W
ESD Protection (Human Body Model)	ESD_{HBM}	JEDEC (JESD 22 - A114)	2000	—	—	V
Flammability Rating	UL-94	UL (Class)	V–0			

Note: While using multiple power supplies, the Voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

2. Functional Description

2.1. Crystal Recommendations

The clock device requires a parallel resonance crystal.

Table 4. Crystal Recommendations

Frequency (Fund)	Cut	Loading	Load Cap	Shunt Cap (max)	Motional (max)	Tolerance (max)	Stability (max)	Aging (max)
25 MHz	AT	Parallel	12–15 pF	5 pF	0.016 pF	35 ppm	30 ppm	5 ppm

2.1.1. Crystal Loading

Crystal loading is critical in achieving low ppm performance. To realize low ppm performance, use the total capacitance the crystal sees to calculate the appropriate capacitive loading (C_L).

Figure 1 shows a typical crystal configuration using the two trim capacitors. It is important that the trim capacitors are in series with the crystal.

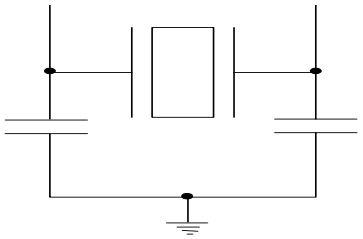


Figure 1. Crystal Capacitive Clarification

2.1.2. Calculating Load Capacitors

In addition to the standard external trim capacitors, consider the trace capacitance and pin capacitance to calculate the crystal loading correctly. Again, the capacitance on each side is in series with the crystal. The total capacitance on both side is twice the specified crystal load capacitance (C_L). Trim capacitors are calculated to provide equal capacitive loading on both sides.

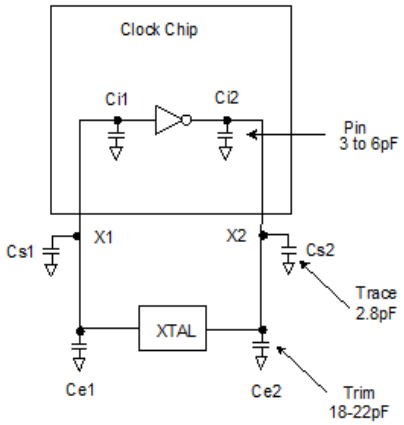


Figure 2. Crystal Loading Example

Use the following formulas to calculate the trim capacitor values for Ce1 and Ce2.

Load Capacitance (each side)

$$Ce = 2 \times CL - (Cs + Ci)$$

Total Capacitance (as seen by the crystal)

$$CLe = \frac{1}{\left(\frac{1}{Ce1 + Cs1 + Ci1} + \frac{1}{Ce2 + Cs2 + Ci2}\right)}$$

- CL: Crystal load capacitance
- CLe: Actual loading seen by crystal using standard value trim capacitors
- Ce: External trim capacitors
- Cs: Stray capacitance (terraced)
- Ci : Internal capacitance (lead frame, bond wires, etc.)

2.2. $\overline{OE}$ Pin Function

The $\overline{OE}$ pin is an active low input used to enable and disable the output clock. To enable the output clock, the $\overline{OE}$ pin needs to be logic low and the I^2C output enable bit needs to be logic high. By default, the $\overline{OE}$ pin is set to a logic low and the I^2C output enable bit is set to a logic high. There are two methods to disable the output clock: the $\overline{OE}$ pin is pulled to a logic high or the I^2C output enable bit is set to a logic low. The $\overline{OE}$ pin is required to be driven at all times even though it has an internal 100 kΩ resistor.

2.3. $\overline{OE}$ Assertion

The $\overline{OE}$ pin is an active low input used for synchronous stopping and starting the respective output clock while the rest of the clock generator continues to function. The assertion of the $\overline{OE}$ function is achieved by pulling the $\overline{OE}$ pin low and the I^2C output enable bit high, which causes the respective stopped output to resume normal operation. No short or stretched clock pulses are produced when the clocks resume. The maximum latency from the assertion to active outputs is no more than two to six output clock cycles.

2.4. $\overline{OE}$ Deassertion

The $\overline{OE}$ function is de-asserted by pulling the pin high, or setting the I^2C output enable bit to a logic low. The corresponding output is stopped and the final output state is driven low.

2.5. SS[1:0] Pins Function

SS1 and SS0 are active inputs used to change the frequency and/or to enable –0.5% down spread on all DIFF outputs. When sampled high or low, the appropriate selection of frequency and spread from Table 5 is applied on all differential outputs. These inputs have an internal pull-down though a 100 kΩ resistor. The default state is SS[1:0] = 00, corresponding to 100 MHz outputs with spread spectrum disabled.

Table 5. SS0 & SS1 Frequency/Spread Selection

SS1	SS0	Differential Frequency	Differential Spread
0	0	100 MHz	Spread Off
0	1	100 MHz	–0.50%
1	0	125 MHz	Spread Off
1	1	200 MHz	Spread Off

3. Test and Measurement Setup

This diagram shows the test load configuration for differential clock signals.

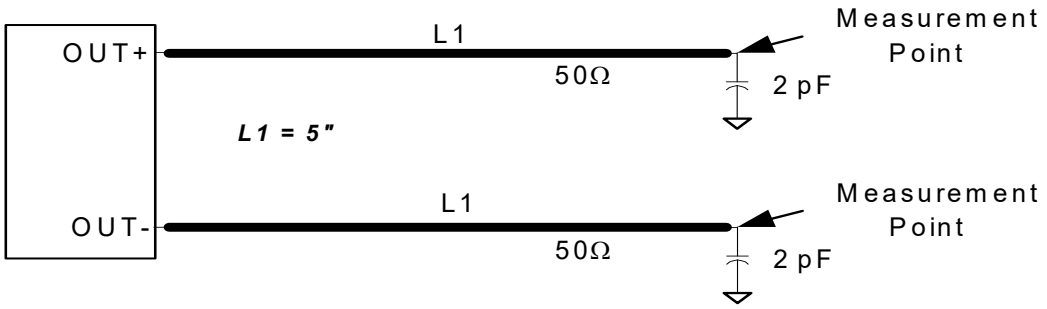


Figure 3. 0.7 V Differential Load Configuration

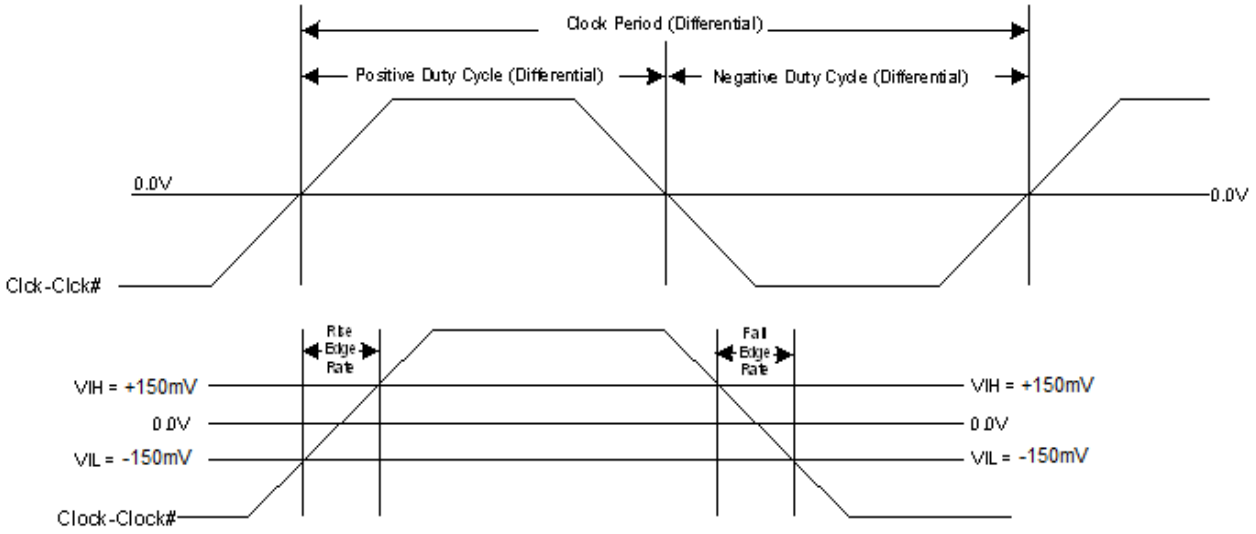


Figure 4. Differential Output Signals (for AC Parameters Measurement)

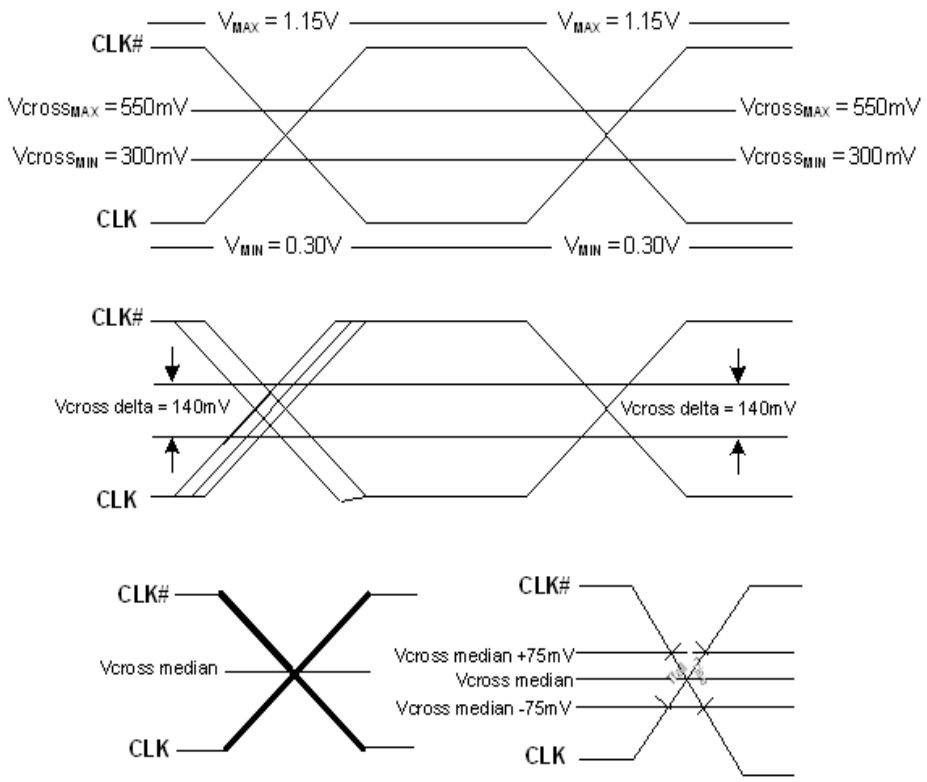


Figure 5. Single-Ended Measurement for Differential Output Signals (for AC Parameter Measurement)

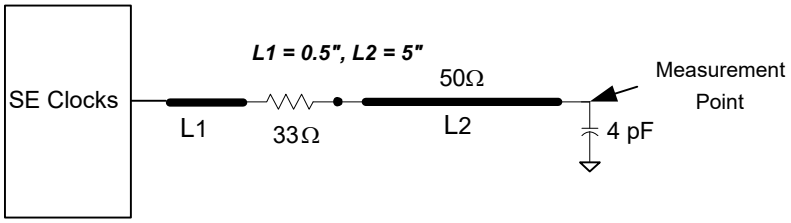


Figure 6. Single-Ended Clocks with Single Load Configuration

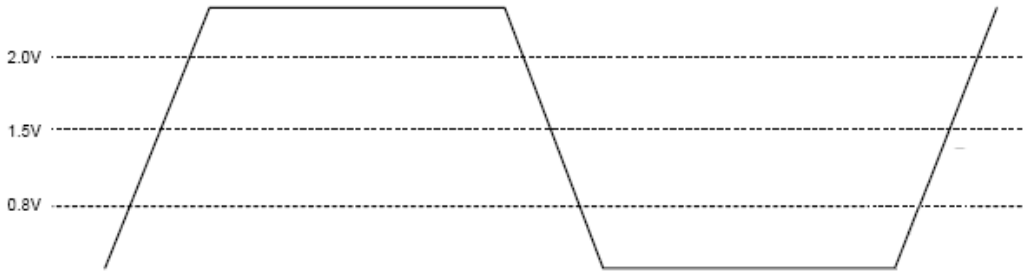


Figure 7. Single-Ended Output Signal (for AC Parameter Measurement)

4. Control Registers

4.1. I²C Interface

To enhance the flexibility and function of the clock synthesizer, an I²C interface is provided. One can control various functions through the I²C interface, such as individual enabling or disabling of the clock output buffers. The registers associated with the I²C interface initialize to their default setting at power-up. The use of this interface is optional. Clock device register changes are normally made at system initialization, if any are required.

4.2. Data Protocol

The I²C protocol accepts byte write, byte read, block write, and block read operations from the controller. For block write/read operation, access the bytes in sequential order from lowest to highest (most significant bit first) with the ability to stop after any complete byte is transferred. For byte write and byte read operations, the system controller can access individually indexed bytes.

The block write and block read protocol is outlined in Table 6 while Table 7 outlines byte write and byte read protocol. The slave receiver address is 11010110 (D6h).

Table 6. Block Read and Block Write Protocol

Block Write Protocol		Block Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
8:2	Slave address–7 bits	8:2	Slave address–7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
18:11	Command Code–8 bits	18:11	Command Code–8 bits
19	Acknowledge from slave	19	Acknowledge from slave
27:20	Byte Count–8 bits	20	Repeat start
28	Acknowledge from slave	27:21	Slave address–7 bits
36:29	Data byte 1–8 bits	28	Read = 1
37	Acknowledge from slave	29	Acknowledge from slave
45:38	Data byte 2–8 bits	37:30	Byte Count from slave–8 bits
46	Acknowledge from slave	38	Acknowledge
....	Data Byte /Slave Acknowledges	46:39	Data byte 1 from slave–8 bits
....	Data Byte N–8 bits	47	Acknowledge
....	Acknowledge from slave	55:48	Data byte 2 from slave–8 bits
....	Stop	56	Acknowledge
		....	Data bytes from slave/Acknowledge
		....	Data Byte N from slave–8 bits
		....	NOT Acknowledge
		....	Stop

Table 7. Byte Read and Byte Write Protocol

Byte Write Protocol		Byte Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
8:2	Slave address–7 bits	8:2	Slave address–7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
18:11	Command Code–8 bits	18:11	Command Code–8 bits
19	Acknowledge from slave	19	Acknowledge from slave
27:20	Data byte–8 bits	20	Repeated start
28	Acknowledge from slave	27:21	Slave address–7 bits
29	Stop	28	Read
		29	Acknowledge from slave
		37:30	Data from slave–8 bits
		38	NOT Acknowledge
		39	Stop

Register 1. Byte 0: Control Register 0

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name						25M_OE		
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 00000100

Bit	Name	Function
7:3	Reserved	
2	25_OE	Output Enable for 25 MHz. 0: Output disabled. 1: Output enabled.
1:0	Reserved	

Register 2. Byte 1: Control Register 1

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name								
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 00000000

Bit	Name	Function
7:0	Reserved	

Register 3. Byte 2: Control Register 2

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	DIFF0_OE	DIFF1_OE						
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 11000000

Bit	Name	Function
7	DIFF0_OE	Output Enable for DIFF0. 0: Output disabled. 1: Output enabled.
6	DIFF1_OE	Output Enable for DIFF1. 0: Output disabled. 1: Output enabled.
5:0	Reserved	

Register 4. Byte 3: Control Register 3

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	Rev Code Bit 3	Rev Code Bit 2	Rev Code Bit 1	Rev Code Bit 0	Vendor ID bit 3	Vendor ID bit 2	Vendor ID bit 1	Vendor ID bit 0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 00001000

Bit	Name	Function
7:4	Rev Code Bit 3:0	Program Revision Code
3:0	Vendor ID bit 3:0	Vendor Identification Code

Register 5. Byte 4: Control Register 4

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	BC7	BC7	BC5	BC4	BC3	BC2	BC1	BC0
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 00000110

Bit	Name	Function
7:0	BC7:0	Byte Count Register.

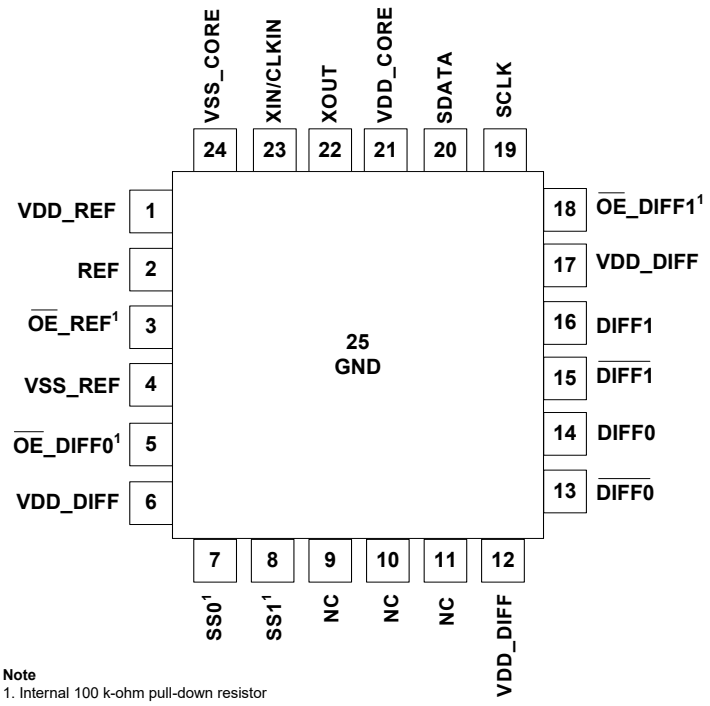
Register 6. Byte 5: Control Register 5

Bit	D7	D6	D5	D4	D3	D2	D1	D0
Name	DIFF_Am_Sel	DIFF_Amp_Cntl[2]	DIFF_Amp_Cntl[1]	DIFF_Amp_Cntl[0]				
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Reset settings = 11011000

Bit	Name	Function
7	DIFF_Amp_Sel	Amplitude control for DIFF Differential outputs. 0: Differential outputs with Default amplitude. 1: Differential outputs amplitude is set by Byte 5[6:4].
6:4	DIF-F_Amp_Cntl[2:0]	DIFF Differential Outputs Amplitude Adjustment. 000: 300 mV 001: 400 mV 010: 500 mV 011: 600 mV 100: 700 mV 101: 800 mV 110: 900 mV 111: 1000 mV
3:0	Reserved	

5. Si52131-A11A Pin Descriptions: 24-Pin QFN



Note
1. Internal 100 k-ohm pull-down resistor

Table 8. Part Number 24-Pin QFN Descriptions

Pin #	Name	Type	Description
1	VDD_REF	PWR	3.3 V power supply.
2	REF	O, SE	3.3 V, 25 MHz Reference clock output.
3	$\overline{OE}$_REF[1]	I,PD	Active low input pin enables REF (internal 100 kΩ pull-down).
4	VSS_REF	GND	Ground.
5	$\overline{OE}$_DIFF0[1]	I,PD	Active low input pin enables DIFF0 (internal 100 kΩ pull-down).
6	VDD_DIFF	PWR	3.3 V power supply.
7	SS0[1]	I, PD	3.3 V tolerant input for enabling frequency/spread selection on DIFF0 and DIFF1 outputs (internal 100 kΩ pull-down).
8	SS1[1]	I, PD	

SS1	SS0	Differential Frequency	Differential Spread
0	0	100 MHz	Spread Off
0	1	100 MHz	–0.50%
1	0	125 MHz	Spread Off
1	1	200 MHz	Spread Off

Table 8. Part Number 24-Pin QFN Descriptions (Continued)

Pin #	Name	Type	Description
9	NC	NC	No connect.
10	NC	NC	No connect.
11	NC	NC	No connect.
12	VDD_DIFF	PWR	3.3 V power supply.
13	$\overline{\text{DIFF0}}$	O, DIF	0.7 V, 100 MHz differential clock output.
14	DIFF0	O, DIF	0.7 V, 100 MHz differential clock output.
15	$\overline{\text{DIFF1}}$	O, DIF	0.7 V, 100 MHz differential clock output.
16	DIFF1	O, DIF	0.7 V, 100 MHz differential clock output.
17	VDD_DIFF	PWR	3.3 V power supply.
18	$\overline{\text{OE}}$_DIFF1[1]	I,PD	Active low input pin enables DIFF1 (internal 100 kΩ pull-down).
19	SCLK	I	I^2C compatible SCLOCK.
20	SDATA	I/O	I^2C compatible SDATA.
21	VDD_CORE	PWR	3.3 V power supply for core.
22	XOUT	O	25.00 MHz Crystal output, *Float XOUT if using CLKIN (Clock input).*
23	XIN/CLKIN	I	25.00 MHz Crystal input or 3.3 V, 25 MHz clock input.
24	VSS_CORE	GND	Ground for core.
25	GND	GND	Ground for bottom pad of the IC.

6. Ordering Guide

Part Number	Package Type	Temperature
Lead-free		
Si52131-A11AGM	24-pin QFN	Extended, –40 to 85 °C
Si52131-A11AGMR	24-pin QFN—Tape and Reel	Extended, –40 to 85 °C

7. Package Outline

Figure 8 illustrates the package details. Table 9 lists the values for the dimensions shown in the illustration.

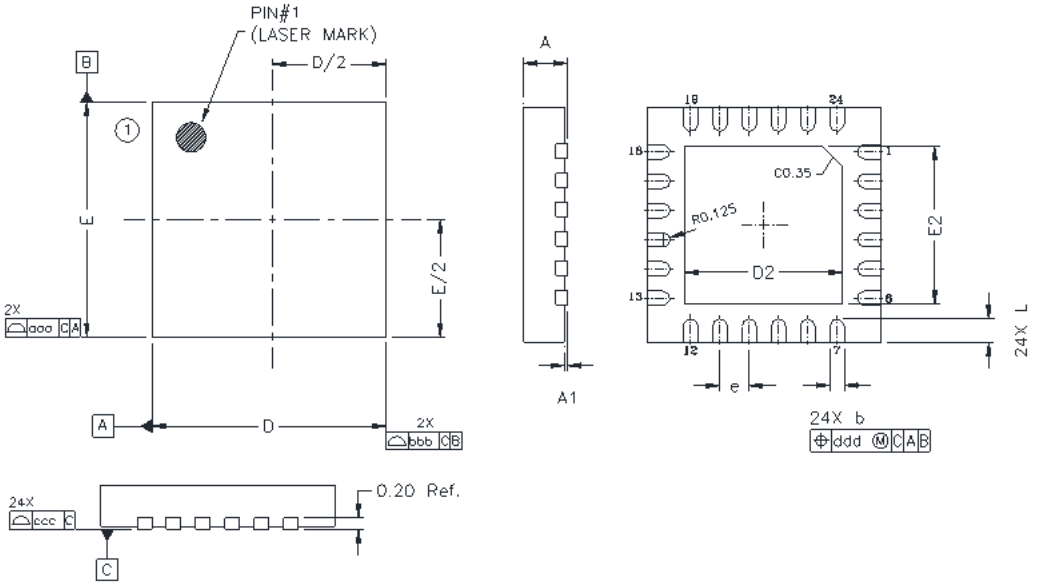


Figure 8. 24-Pin Quad Flat No Lead (QFN) Package

Table 9. Package Diagram Dimensions

Symbol	Millimeters		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	0.00	0.025	0.05
b	0.20	0.25	0.30
D		4.00 BSC.	
D2	2.60	2.70	2.80
e		0.50 BSC.	
E		4.00 BSC.	
E2	2.60	2.70	2.80
L	0.30	0.40	0.50
aaa		0.10	
bbb		0.10	
ccc		0.08	
ddd		0.07	

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerances per ANSI Y14.5M-1994.
3. This drawing conforms to JEDEC outline MO-220, variation VGGD-8
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components

SKYWORKS®

ClockBuilder Pro

Customize Skyworks clock generators, jitter attenuators and network synchronizers with a single tool. With CBPro you can control evaluation boards, access documentation, request a custom part number, export for in-system programming and more!

www.skyworksinc.com/CBPro

Portfolio
www.skyworksinc.com/ia/timing

SW/HW
www.skyworksinc.com/CBPro

Quality
www.skyworksinc.com/quality

Support & Resources
www.skyworksinc.com/support

Skyworks Solutions, Inc. | Nasdaq: SWKS | sales@skyworksinc.com | www.skyworksinc.com
USA: 781-376-3000 | Asia: 886-2-2735 0399 | Europe: 33 (0)1 43548540 |