Ultra-Low Power Stereo Audio Codec

MAX9867

General Description

The MAX9867 is an ultra-low power stereo audio codec designed for portable consumer devices such as mobile phones and portable gaming consoles.

The device features stereo differential microphone inputs that can be connected to either analog or digital microphones. The single-ended line inputs, with configurable preamplifier, can be sent to the ADC for record or routed directly to the headphone amplifier for playback. An auxiliary ADC path can be used to track any DC voltage.

The stereo headphone amplifiers support differential, single-ended, and capacitorless output configurations. Using the capacitorless output configuration, the device can output 10mW into 32Ω headphones. Comprehensive click-and-pop circuitry suppresses audible clicks and pops during volume changes and startup or shutdown.

Utilizing Maxim's proprietary digital circuitry, the device can accept any available 10MHz to 60MHz system clock. This architecture eliminates the need for an external PLL and multiple crystal oscillators. The stereo ADC and DAC paths provide user-configurable voiceband or audioband digital filters. Voiceband filters provide extra attenuation at the GSM packet frequency and greater than 70dB stopband attenuation at $f_S/2$.

The MAX9867 operates from a single 1.8V supply, and supports a 1.65V to 3.6V logic level. An I²C 2-wire serial interface provides control for volume levels, signal mixing, and general operating modes.

The MAX9867 is available in a tiny 2.2mm x 2.7mm, 0.4mm-ball-pitch, WLP package. A 32-pin 5mm x 5mm TQFN package is also available.

Features

- 1.8V Single-Supply Operation
- 6.7mW Playback Power Consumption
- 90dB Stereo DAC, 8kHz ≤ f_S ≤ 48kHz
- 85dB Stereo ADC, 8kHz ≤ f_S ≤ 48kHz
- Battery-Measurement Auxiliary ADC
- Support for Any Master Clock Between 10MHz to 60MHz
- Stereo Digital Microphone Input Support
- Stereo Analog Differential Microphone Inputs
- Stereo Headphone Amplifiers: Differential, Single-Ended, or Capacitorless
- Stereo Line Inputs
- Voiceband Filter with a Stopband Attenuation Greater than 70dB
- 1.65V to 3.6V Digital Interface Supply Voltage
- I²S/TDM-Compatible Digital Audio Bus
- 30-Bump, 2.2mm x 2.7mm 0.4mm-Pitch WLP

Applications

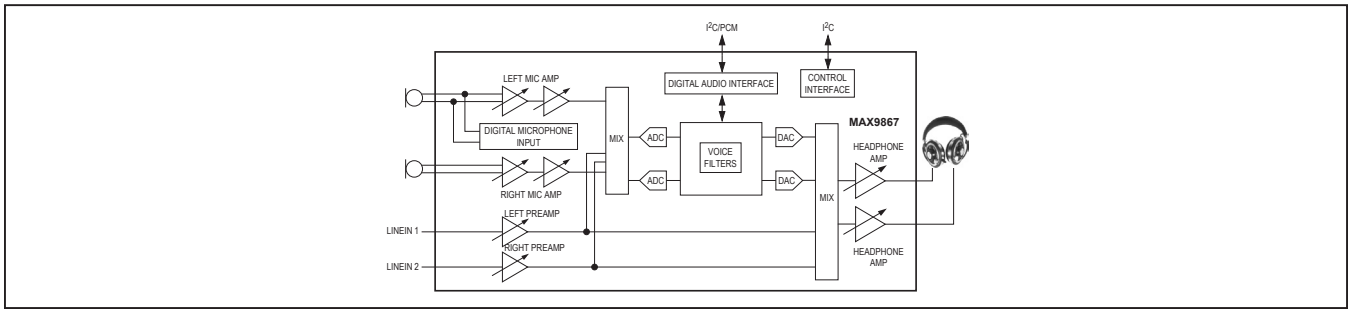
- Cell Phones
- Portable Gaming Devices
- Portable Navigation Devices
- Portable Multimedia Players
- Wireless Headsets

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX9867EWV+	-40°C to +85°C	30 WLP
MAX9867ETJ+	-40°C to +85°C	32 TQFN-EP*

+Denotes lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*

Simplified Block Diagram



19-4573; Rev 4; 12/21

Absolute Maximum Ratings

(Voltages with respect to AGND.)
DVDD, AVDD, and PVDD.....-0.3V to +2V
DVDDIO.....-0.3V to +3.6V
DGND and PGND .....-0.1V to +0.1V
PREG, REF, REG, MICBIAS..... -0.3V to (AVDD + 0.3V)
MCLK, LRCLK, BCLK
SDOUT, SDIN..... -0.3V to (DVDDIO + 0.3V)
SDA, SCL, $\overline{IRQ}$.....-0.3V to +3.6V
LOUTP, LOUTN, ROUTP,
ROUTN..... (PGND - 0.3V) to (PVDD + 0.3V)
LINL, LINR, JACKSNS/AUX, MICLP/DIGMICDATA,
MICLN/DIGMICCLK, MICRP, MICRN...-0.3V to (AVDD + 0.3V)

Continuous Power Dissipation (T_A = +70°C)
30-Bump WLP (derate 12.5mW/°C above +70°C)....1000mW
32-Pin TQFN-EP (derate 34.5mW/°C above +70°C)... 2759mW
Junction-to-Ambient Thermal Resistance (θ_{JA}) (Note 1)
30-Bump WLP .....80°C/W
32-Pin TQFN-EP.....29°C/W
Operating Temp Range ..... -40°C to +85°C
Storage Temp Range ..... -65°C to +150°C
Lead Temperature (TQFN only, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDIO} = +1.8V, R_L = ∞, headphone load (R_L) connected between _OUTP and _OUTN in differential mode, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{PRE} = +20dB, AV_{PGAM} = 0dB, AV_{DAC} = 0dB, AV_{LINE} = +20dB, AV_{VOL} = 0dB, MCLK = 13MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range		PVDD, DVDD, AVDD		1.65	1.8	1.95	V
		DVDDIO		1.65	1.8	3.6	
Total Supply Current	I_{VDD}	Full-duplex 8kHz mono (voice mode) (Note 3)	Analog (AVDD + PVDD)		4.65	7	mA
			Digital (DVDD + DVDDIO)		0.96	1.5	
		DAC playback 48kHz stereo (audio mode) (Note 3)	Analog (AVDD + PVDD)		3.28	5	
			Digital (DVDD + DVDDIO)		1.40	2	
		Full-duplex 48kHz stereo (audio mode) (Note 3)	Analog (AVDD + PVDD)		8.0	12	
			Digital (DVDD + DVDDIO)		2.0	3	
		Stereo line-in only	Analog (AVDD + PVDD)		3.8	6	
			Digital (DVDD + DVDDIO)		0.004	0.05	
Shutdown Supply Current		T_A = +25°C	Analog (AVDD + PVDD)		1	5	µA
			Digital (DVDD + DVDDIO)		1	5	

Electrical Characteristics (continued)

(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDIO} = +1.8V, R_L = ∞, headphone load (R_L) connected between _OUTP and _OUTN in differential mode, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{PRE} = +20dB, AV_{PGAM} = 0dB, AV_{DAC} = 0dB, AV_{LINE} = +20dB, AV_{VOL} = 0dB, MCLK = 13MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Shutdown to Full Operation		Excludes PLL lock time			10		ms
Soft-Start/-Stop Time					10		ms
DAC (Note 4)							
Dynamic Range (Note 5)	DR	f_S = 48kHz, AV_{VOL} = 0dB, T_A = +25°C	Master or slave mode		90		dB
			Slave mode	84			
Full-Scale Output		V_{OLL}/V_{OLR} = 0x09	Differential mode		1		V_{RMS}
			Capacitorless and single-ended modes		0.56		
Gain Error		DC accuracy, measured with respect to full-scale output			1	5	%
Voice Path Phase Delay	P_{DLY}	f = 1kHz, 0dBFS, HP filter disabled, digital input to analog output	f_S = 8kHz		1.2		ms
			f_S = 16kHz		0.59		
Total Harmonic Distortion	THD	MCLK = 12.288MHz, f_S = 48kHz, 0dBFS, measured at headphone outputs			-80		dB
DAC Attenuation Range	AV_{DAC}	DACA = 0xF to 0x0		-15		0	dB
DAC Gain Adjust	AV_{GAIN}	DACG = 00 to 11		0		+18	dB
Power-Supply Rejection Ratio	PSRR	V_{AVDD} = V_{PVDD} = 1.65V to 1.95V		60	78		dB
		f = 217Hz, V_{RIPPLE} = 100mV_{P-P}, AV_{VOL} = 0dB			78		
		f = 1kHz, V_{RIPPLE} = 100mV_{P-P}, AV_{VOL} = 0dB			75		
		f = 10kHz, V_{RIPPLE} = 100mV_{P-P}, AV_{VOL} = 0dB			62		
DAC VOICE MODE DIGITAL IIR LOWPASS FILTER							
Passband Cutoff	f_{PLP}	With respect to f_S within ripple; f_S = 8kHz to 48kHz			0.448 x f_S		Hz
		-3dB cutoff			0.451 x f_S		
Passband Ripple		f < f_{PLP}			±0.1		dB
Stopband Cutoff	f_{SLP}	With respect to f_S; f_S = 8kHz to 48kHz			0.476 x f_S		Hz
Stopband Attenuation		f > f_{SLP}, f = 20Hz to 20kHz		75			dB

Electrical Characteristics (continued)

(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDIO} = +1.8V, R_L = ∞, headphone load (R_L) connected between _OUTP and _OUTN in differential mode, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{PRE} = +20dB, AV_{PGAM} = 0dB, AV_{DAC} = 0dB, AV_{LINE} = +20dB, AV_{VOL} = 0dB, MCLK = 13MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DAC VOICE MODE DIGITAL 5th ORDER IIR HIGHPASS FILTER						
5th Order Passband Cutoff (-3dB from Peak, I²C Register Programmable)	f_{DHPPB}	DVFLT = 0x1 (elliptical tuned for 16kHz GSM + 217Hz notch)		0.0161 x f_S		Hz
		DVFLT = 0x2 (500Hz Butterworth tuned for 16kHz)		0.0312 x f_S		
		DVFLT = 0x3 (elliptical tuned for 8kHz GSM + 217Hz notch)		0.0321 x f_S		
		DVFLT = 0x4 (500Hz Butterworth tuned for 8kHz)		0.0625 x f_S		
		DVFLT = 0x5 (f_S/240 Butterworth)		0.0042 x f_S		
5th Order Stopband Cutoff (-30dB from Peak, I²C Register Programmable)	f_{DHPSB}	DVFLT = 0x1 (elliptical tuned for 16kHz GSM + 217Hz notch)		0.0139 x f_S		Hz
		DVFLT = 0x2 (500Hz Butterworth tuned for 16kHz)		0.0156 x f_S		
		DVFLT = 0x3 (elliptical tuned for 8kHz GSM + 217Hz notch)		0.0279 x f_S		
		DVFLT = 0x4 (500Hz Butterworth tuned for 8kHz)		0.0312 x f_S		
		DVFLT = 0x5 (f_S/240 Butterworth)		0.0021 x f_S		
DC Attenuation	DC_{ATTEN}	DVFLT ≠ 000		90		dB
DAC STEREO AUDIO MODE DIGITAL FIR LOWPASS FILTER						
Passband Cutoff	f_{PLP}	With respect to f_S within ripple; f_S = 8kHz to 48kHz		0.43 x f_S		Hz
		-3dB cutoff		0.47 x f_S		
		-6.02dB cutoff		0.50 x f_S		
Passband Ripple		$f < f_{PLP}$		±0.1		dB
Stopband Cutoff	f_{SLP}	With respect to f_S; f_S = 8kHz to 48kHz		0.58 x f_S		Hz
Stopband Attenuation			60			dB

Electrical Characteristics (continued)

(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDIO} = +1.8V, R_L = ∞, headphone load (R_L) connected between _OUTP and _OUTN in differential mode, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{PRE} = +20dB, AV_{PGAM} = 0dB, AV_{DAC} = 0dB, AV_{LINE} = +20dB, AV_{VOL} = 0dB, MCLK = 13MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DAC STEREO AUDIO MODE DIGITAL DC BLOCKING HIGHPASS FILTER						
Passband Cutoff (-3dB from Peak)	f_{DHPPB}	DVFLT = 0x1		0.000625 x f_S		Hz
DC Attenuation	DC_{ATTEN}	DVFLT = 0x1		90		dB
ADC (Note 6)						
Dynamic Range (Note 5)	DR	f_S = 8kHz, MODE = 0 (IIR voice)	75	84		dB
		f_S = 8kHz to 48kHz, MODE = 1 (FIR audio)		85		
Full-Scale Input		Differential MIC input or stereo-line inputs, AV_{PRE} = 0dB, AV_{PGAM} = 0dB		1		VP-P
Gain Error (Note 7)		DC accuracy, measured with respect to 80% of full-scale output		1	5	%
Voice Path Phase Delay	P_{DLY}	f = 1kHz, 0dBFS, HP filter disabled, analog input to digital output; f_S = 8kHz		1.2		ms
		f = 1kHz, 0dBFS, HP filter disabled, analog input to digital output; f_S = 16kHz		0.61		
Total Harmonic Distortion	THD	f = 1kHz, f_S = 8kHz, T_A = +25°C, 0dBFS		-81	-70	dB
ADC Level Adjust Range	AV_{ADC}	AVL/AVR = 0xF to 0x0	-12		+3	dB
Power-Supply Rejection Ratio	PSRR	V_{AVDD} = 1.65V to 1.95V, input referred	60	85		dB
		f = 217Hz, V_{RIPPLE} = 100mV, AV_{ADC} = 0dB, input referred		85		
		f = 1kHz, V_{RIPPLE} = 100mV, AV_{ADC} = 0dB, input referred		80		
		f = 10kHz, V_{RIPPLE} = 100mV, AV_{ADC} = 0dB, input referred		80		
ADC VOICE MODE DIGITAL IIR LOWPASS FILTER						
Passband Cutoff	f_{PLP}	With respect to f_S within ripple; f_S = 8kHz to 48kHz		0.445 x f_S		Hz
		-3dB cutoff		0.449 x f_S		
Passband Ripple		f < f_{PLP}		±0.1		dB
Stopband Cutoff	f_{SLP}	With respect to f_S; f_S = 8kHz to 48kHz		0.469 x f_S		Hz
Stopband Attenuation		f > f_{SLP}, f = 20Hz to 20kHz	74			dB

Electrical Characteristics (continued)

(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDIO} = +1.8V, R_L = ∞, headphone load (R_L) connected between _OUTP and _OUTN in differential mode, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{PRE} = +20dB, AV_{PGAM} = 0dB, AV_{DAC} = 0dB, AV_{LINE} = +20dB, AV_{VOL} = 0dB, MCLK = 13MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ADC VOICE MODE DIGITAL 5th ORDER IIR HIGHPASS FILTER						
5th Order Passband Cutoff (-3dB from Peak, I²C Register Programmable)	f_{AHPPB}	AVFLT = 0x1 (elliptical tuned for 16kHz GSM + 217Hz notch)		0.0161 x f_S		Hz
		AVFLT = 0x2 (500Hz Butterworth tuned for 16kHz)		0.0312 x f_S		
		AVFLT = 0x3 (elliptical tuned for 8kHz GSM + 217Hz notch)		0.0321 x f_S		
		AVFLT = 0x4 (500Hz Butterworth tuned for 8kHz)		0.0625 x f_S		
		AVFLT = 0x5 (f_S/240 Butterworth)		0.0042 x f_S		
Stopband Cutoff (-30dB from Peak)	f_{AHPSB}	AVFLT = 0x1 (elliptical tuned for 16kHz GSM + 217Hz notch)		0.0139 x f_S		Hz
		AVFLT = 0x2 (500Hz Butterworth tuned for 16kHz)		0.0156 x f_S		
		AVFLT = 0x3 (elliptical tuned for 8kHz GSM + 217Hz notch)		0.0279 x f_S		
		AVFLT = 0x4 (500Hz Butterworth tuned for 8kHz)		0.0312 x f_S		
		AVFLT = 0x5 (f_S/240 Butterworth)		0.0021 x f_S		
DC Attenuation	DC_{ATTEN}	AVFLT ≠ 000		90		dB
ADC STEREO AUDIO MODE DIGITAL FIR LOWPASS FILTER						
Passband Cutoff	f_{PLP}	With respect to f_S within ripple; f_S = 8kHz to 48kHz		0.43 x f_S		Hz
		-3dB cutoff		0.48 x f_S		
		-6.02dB cutoff		0.5 x f_S		
Passband Ripple		f < f_{PLP}		±0.1		dB
Stopband Cutoff	f_{SLP}	With respect to f_S; f_S = 8kHz to 48kHz		0.58 x f_S		Hz
Stopband Attenuation		f > f_{SLP}, f = 20Hz to 20kHz	60			dB

Electrical Characteristics (continued)

(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDIO} = +1.8V, R_L = ∞, headphone load (R_L) connected between _OUTP and _OUTN in differential mode, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{PRE} = +20dB, AV_{PGAM} = 0dB, AV_{DAC} = 0dB, AV_{LINE} = +20dB, AV_{VOL} = 0dB, MCLK = 13MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ADC STEREO AUDIO MODE DIGITAL DC BLOCKING HIGHPASS FILTER							
Passband Cutoff (-3dB from Peak)	f_{AHPPB}	AVFLT = 0x1			0.000625 x f_S		Hz
DC Attenuation	DC_{ATTEN}	AVFLT = 0x1			90		dB
OUTPUT VOLUME CONTROL							
Line Input to Output Volume Control	AV_{VOL}	VOLL/VOLR = 0x00		14.55	14.9	15.15	dB
		VOLL/VOLR = 0x01		14.1	14.4	14.6	
		VOLL/VOLR = 0x02		13.6	13.9	14.1	
		VOLL/VOLR = 0x04		12.6	12.9	13.1	
		VOLL/VOLR = 0x08		9.35	9.9	10.35	
		VOLL/VOLR = 0x10		0.35	0.9	1.35	
		VOLL/VOLR = 0x20		-50.15	-49.2	-48.15	
Output Volume Control Step Size		VOLL/VOLR = 0x00 to 0x06 (+6dB to +3dB)			0.5		dB
		VOLL/VOLR = 0x06 to 0x0F (+3dB to -6dB)			1		
		VOLL/VOLR = 0x0F to 0x17 (-6dB to -22dB)			2		
		VOLL/VOLR = 0x17 to 0x3F (-22dB to mute)			4		
Output Volume Control Mute Attenuation		f = 1kHz			100		dB
HEADPHONE AMPLIFIER (Note 8)							
Output Power per Channel (Differential Mode)	P_{OUT}	f = 1kHz, THD < 1%, T_A = +25°C	R_L = 16Ω	30	52		mW
			R_L = 32Ω		32		
Output Power per Channel (Capacitorless Mode)	P_{OUT}	f = 1kHz, THD < 1%, T_A = +25°C	R_L = 16Ω		19		mW
			R_L = 32Ω	8	10		
Total Harmonic Distortion + Noise (Differential Mode)	THD+N	R_L = 16Ω, P_{OUT} = 25mW, f = 1kHz			-76		dB
		R_L = 32Ω, P_{OUT} = 25mW, f = 1kHz	MCLK = 13MHz, f_S = 8kHz		-77	-70	
			MCLK = 12.288MHz, f_S = 48kHz		-80		
Total Harmonic Distortion + Noise (Capacitorless Mode)	THD+N	R_L = 16Ω, P_{OUT} = 6.25mW, f = 1kHz			-72		dB
		R_L = 32Ω, P_{OUT} = 6.25mW, f = 1kHz	MCLK = 13MHz, f_S = 8kHz		-74	-65	
			MCLK = 12.288MHz, f_S = 48kHz		-74		
Total Harmonic Distortion + Noise (SE Mode)	THD+N	R_L = 16Ω, P_{OUT} = 6.25mW, f = 1kHz			-74		dB
		R_L = 32Ω, P_{OUT} = 6.25mW, f = 1kHz	MCLK = 13MHz, f_S = 8kHz		-74	-65	
			MCLK = 12.288MHz, f_S = 48kHz		-76		
Dynamic Range	DR	AV_{VOL} = +6dB (Notes 5, 7)		76	90		dB

Electrical Characteristics (continued)

(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDIO} = +1.8V, R_L = ∞, headphone load (R_L) connected between _OUTP and _OUTN in differential mode, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{PRE} = +20dB, AV_{PGAM} = 0dB, AV_{DAC} = 0dB, AV_{LINE} = +20dB, AV_{VOL} = 0dB, MCLK = 13MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Power-Supply Rejection Ratio (Note 7)	PSRR	V_{AVDD} = V_{PVDD} = 1.65V to 1.95V		60	78		dB
		f = 217Hz, V_{RIPPLE} = 100mV_{P-P}, AV_{VOL} = 0dB			78		
		f = 1kHz, V_{RIPPLE} = 100mV_{P-P}, AV_{VOL} = 0dB			75		
		f = 10kHz, V_{RIPPLE} = 100mV_{P-P}, AV_{VOL} = 0dB			62		
Output Offset Voltage	V_{OS}	AV_{VOL} = -84dB differential mode	(LOUTP–LOUTN, ROUTP–ROUTN), T_A = +25°C		±0.2		mV
		AV_{VOL} = -84dB capacitorless mode	(LOUTP–LOUTN, ROUTP–LOUTN), T_A = +25°C		±0.8		
Crosstalk	X_{TALK}	Differential mode, P_{OUT} = 5mW, f = 1kHz			87		dB
		Capacitorless mode, P_{OUT} = 5mW, f = 1kHz	TQFN		55		
			WLP		60		
Capacitive Drive		No sustained oscillations	R_L = 32Ω		500		pF
			R_L = J		100		
Click-and-Pop Level (Differential, Capacitorless Modes)		Peak voltage, A-weighted, 32 samples per second	Into shutdown		-80		dBV
			Out of shutdown		-69		
Click-and-Pop Level (SE Mode)		Peak voltage, A-weighted, 32 samples per second	Into shutdown		-75		dBV
			Out of shutdown		-75		
MICROPHONE AMPLIFIER							
Preamplifier Gain	AV_{PRE}	PALEN/PAREN = 01		-0.5	0	+0.5	dB
		PALEN/PAREN = 10		19.5	20	20.5	
		PALEN/PAREN = 11		29.5	30	30.5	
MIC PGA Gain	AV_{PGAM}	PGAML/PGAMR = 0x1F		-0.6	-0.1	+0.4	dB
		PGAML/PGAMR = 0x00		19.3	19.75	20.3	
Common-Mode Rejection Ratio	CMRR	V_{IN} = 100mV_{P-P}, f = 217Hz			50		dB
MIC Input Resistance	R_{IN_MIC}	All gain settings		30	50		kΩ

Electrical Characteristics (continued)

(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDIO} = +1.8V, R_L = ∞, headphone load (R_L) connected between _OUTP and _OUTN in differential mode, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{PRE} = +20dB, AV_{PGAM} = 0dB, AV_{DAC} = 0dB, AV_{LINE} = +20dB, AV_{VOL} = 0dB, MCLK = 13MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Total Harmonic Distortion + Noise	THD+N	AV_{PRE} = 0dB, V_{IN} = $1V_{P-P}$, f = 1kHz		-80		dB
		AV_{PRE} = +30dB, V_{IN} = $32mV_{P-P}$, f = 1kHz, ($1V_{P-P}$ at ADC input)		-67		
Power-Supply Rejection Ratio	PSRR	V_{AVDD} = 1.65V to 1.95V, input referred	60	85		dB
		f = 217Hz, V_{RIPPLE} = 100mV, AV_{ADC} = 0dB, input referred		85		
		f = 1kHz, V_{RIPPLE} = 100mV, AV_{ADC} = 0dB, input referred		80		
		f = 10kHz, V_{RIPPLE} = 100mV, AV_{ADC} = 0dB, input referred		80		
MICROPHONE BIAS						
Output Voltage	$V_{MICBIAS}$	V_{AVDD} = 1.8V, I_{LOAD} = 1mA	1.5	1.525	1.55	V
Load Regulation		I_{LOAD} = 1mA to 2mA		0.2	10	V/A
Line Regulation		V_{AVDD} = 1.65V to 1.95V		10		µV/V
Power-Supply Rejection Ratio	PSRR	f = 217Hz, V_{RIPPLE} = $100mV_{P-P}$		85		dB
		f = 10kHz, V_{RIPPLE} = $100mV_{P-P}$		81		
Noise Voltage		A-weighted		9.1		$µV_{RMS}$
LINE INPUT						
Full-Scale Input	V_{IN}	AV_{LINE} = 0dB		1.0		V_{P-P}
Line Input Level Adjust Range	AV_{LINE}	LIGL/LIGR = 0xF to 0x0	-6.5		+24.5	dB
Line Input Mute Attenuation		f = 1kHz		100		dB
Input Resistance	R_{IN_LINE}	AV_{LINE} = +24dB	20			kΩ
Total Harmonic Distortion + Noise	THD+N	V_{IN} = $0.1V_{P-P}$, f = 1kHz, differential output		-83		dB
AUXIN INPUT						
Input DC Voltage Range		AUXEN = 1	0		0.738	V
AUXIN Input Resistance	R_{IN}	AUXEN = 1, 0V ≤ AUXIN ≤ 0.738V	10	40		MΩ
JACK SENSE OPERATION						
Threshold	V_{TH}	JDETEN = 1, $\overline{SHDN}$ = 1, JACKSNS	0.92 x MICBIAS	0.95 x MICBIAS	0.98 x MICBIAS	V
		JDETEN = 1, $\overline{SHDN}$ = 0, JACKSNS, LOUTP	AVDD - 0.8	AVDD - 0.4	AVDD - 0.15	
Pullup Current	I_{PU}	JDETEN = 1, $\overline{SHDN}$ = 1, JACKSNS = GND		4		µA
		JDETEN = 1, $\overline{SHDN}$ = 0, JACKSNS = LOUTP = GND		4	20	
Pullup Voltage		JDETEN = 1, JACKSNS, LOUTP		AVDD		V

Electrical Characteristics (continued)

(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDIO} = +1.8V, R_L = ∞, headphone load (R_L) connected between _OUTP and _OUTN in differential mode, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{PRE} = +20dB, AV_{PGAM} = 0dB, AV_{DAC} = 0dB, AV_{LINE} = +20dB, AV_{VOL} = 0dB, MCLK = 13MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DIGITAL SIDETONE							
Sidetone Gain Adjust Range	AV_{STGA}	Differential output mode, DVST = 0x1F to 0x01		-60		0	dB
Voice Path Phase Delay	P_{DLY}	MIC input to headphone output, f = 1kHz, HP filter disabled, f_S = 8kHz			2.2		ms
INPUT CLOCK CHARACTERISTICS							
MCLK Input Frequency	f_{MCLK}	For any LRCLK sample rate		10		60	MHz
MCLK Input Duty Cycle		Prescaler = /1 mode		40		60	%
		/2 or /4 modes		30		70	
Maximum MCLK Input Jitter		Maximum allowable RMS for performance limits			100		ps_{RMS}
LRCLK Sample Rate Range				8		48	kHz
LRCLK PLL Lock Time		Any allowable LRCLK and PCLK rate, slave mode	Rapid lock mode		2	7	ms
			Nonrapid lock mode		12	25	
LRCLK Acceptable Jitter for Maintaining PLL Lock		Allowable LRCLK period change from nominal for slave PLL mode at any allowable LRCLK and PCLK rates				±100	ns
LRCLK Average Frequency Error (Master and Slave Modes) (Note 9)		FREQ = 0x8 through 0xF		0		0	%
		PCLK = 192xf_S, 256xf_S, 384xf_S, 512xf_S, 768xf_S, and 1024xf_S		0		0	
		All other modes		-0.025		+0.025	
DIGITAL INPUT (MCLK)							
Input High Voltage	V_{IH}			1.2			V
Input Low Voltage	V_{IL}					0.6	V
Input Leakage Current	I_{IH}, I_{IL}	T_A = +25°C				±1	µA
Input Capacitance					10		pF
DIGITAL INPUTS (SDIN, BCLK, LRCLK)							
Input High Voltage	V_{IH}			0.7 x DVDDIO			V
Input Low Voltage	V_{IL}					0.3 x DVDDIO	V
Input Hysteresis					200		mV
Input Leakage Current	I_{IH}, I_{IL}	T_A = +25°C				±1	µA
Input Capacitance					10		pF

Electrical Characteristics (continued)

(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDIO} = +1.8V, R_L = ∞, headphone load (R_L) connected between _OUTP and _OUTN in differential mode, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{PRE} = +20dB, AV_{PGAM} = 0dB, AV_{DAC} = 0dB, AV_{LINE} = +20dB, AV_{VOL} = 0dB, MCLK = 13MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL INPUTS (SDA, SCL)						
Input High Voltage	V_{IH}		0.7 x DVDD			V
Input Low Voltage	V_{IL}				0.3 x DVDD	V
Input Hysteresis				200		mV
Input Leakage Current	I_{IH}, I_{IL}	T_A = +25°C			±1	µA
Input Capacitance				10		pF
DIGITAL INPUT (DIGMICDATA)						
Input High Voltage	V_{IH}		0.65 x DVDD			V
Input Low Voltage	V_{IL}				0.35 x DVDD	V
Input Hysteresis				100		mV
Input Leakage Current	I_{IH}, I_{IL}	T_A = +25°C			±35	µA
Input Capacitance				10		pF
CMOS DIGITAL OUTPUTS (BCLK, LRCLK, SDOUT)						
Output Low Voltage	V_{OL}	I_{OL} = 3mA			0.4	V
Output High Voltage	V_{OH}	I_{OH} = 3mA	DVDDIO - 0.4			V
CMOS DIGITAL OUTPUT (DIGMICCLK)						
Output Low Voltage	V_{OL}	I_{OL} = 1mA			0.4	V
Output High Voltage	V_{OH}	I_{OH} = 1mA	DVDD - 0.4			V
OPEN-DRAIN DIGITAL OUTPUTS (SDA, $\overline{IRQ}$)						
Output High Current	I_{OH}	V_{OUT} = V_{DVDD}, T_A = +25°C			1	µA
Output Low Voltage	V_{OL}	I_{OL} = 3mA			0.2 x DVDD	V
DIGITAL MICROPHONE TIMING CHARACTERISTICS (V_{DVDD} = 1.65V)						
DIGMICCLK Divide Ratio	f_{MICCLK}	MICCLK = 00		PCLK/8		MHz
		MICCLK = 01		PCLK/6		
DIGMICDATA to DIGMICCLK Setup Time	$t_{SU, MIC}$	Either clock edge	20			ns
DIGMICDATA to DIGMICCLK Hold Time	$t_{HD, MIC}$	Either clock edge	0			ns
DIGITAL AUDIO INTERFACE TIMING CHARACTERISTICS (V_{DVDD} = 1.65V)						
Minimum BCLK Cycle Time	t_{BCLKS}	Slave operation		75		ns
	t_{BCLKM}	Master operation		325		ns

Electrical Characteristics (continued)

(V_{AVDD} = V_{PVDD} = V_{DVDD} = V_{DVDDIO} = +1.8V, R_L = ∞, headphone load (R_L) connected between _OUTP and _OUTN in differential mode, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{PRE} = +20dB, AV_{PGAM} = 0dB, AV_{DAC} = 0dB, AV_{LINE} = +20dB, AV_{VOL} = 0dB, MCLK = 13MHz, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

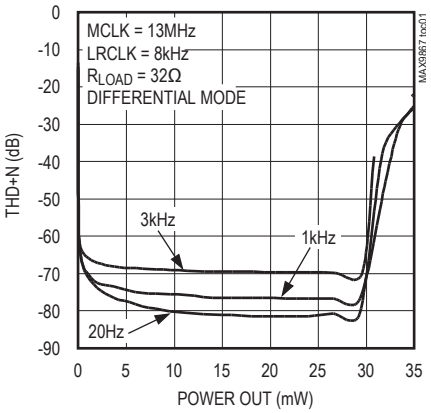
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Minimum BCLK High Time	t_{BCLKH}	Slave operation		30		ns
Minimum BCLK Low Time	t_{BCLKL}	Slave operation		30		ns
BCLK or LRCLK Rise and Fall Time	t_R, t_F	Master operation, C_L = 15pF		7		ns
SDIN or LRCLK to BCLK Setup Time	t_{SU}		20			ns
SDIN or LRCLK to BCLK Hold Time	t_{HD}		0			ns
SDOUT Delay Time from BCLK Rising Edge	t_{DLY}	C_L = 30pF	0		40	ns
I²C TIMING CHARACTERISTICS (V_{DVDD} = 1.65V)						
Serial-Clock Frequency	f_{SCL}		0		400	kHz
Bus Free Time Between STOP and START Conditions	t_{BUF}		1.3			µs
Hold Time (REPEATED) START Condition	$t_{HD, STA}$		0.6			µs
SCL Pulse-Width Low	t_{LOW}		1.3			µs
SCL Pulse-Width High	t_{HIGH}		0.6			µs
Setup Time for a REPEATED START Condition	$t_{SU, STA}$		0.6			µs
Data Hold Time	$t_{HD, DAT}$	$R_{PU, SDA}$ = 475Ω	0		900	ns
Data Setup Time	$t_{SU, DAT}$		100			ns
SDA and SCL Receiving Rise Time	t_R	(Note 10)	20 + 0.1C_B		300	ns
SDA and SCL Receiving Fall Time	t_F	(Note 10)	20 + 0.1C_B		300	ns
SDA Transmitting Fall Time	t_F	$R_{PU, SDA}$ = 475Ω (Note 10)	20 + 0.1C_B		250	ns
Setup Time for STOP Condition	$t_{SU, STO}$		0.6			µs
Bus Capacitance	C_B				400	pF
Pulse Width of Suppressed Spike	t_{SP}		0		50	ns

Note 2: The MAX9867 is 100% production tested at T_A = +25°C. Specifications over temperature limits are guaranteed by design.
Note 3: Clocking all zeros into the DAC, master mode, and differential headphone mode.
Note 4: DAC performance measured at the headphone outputs.
Note 5: Dynamic range measured using the EIAJ method. -60dBFS 1kHz output signal, A-weighted, and normalized to 0dBFS. f = 20Hz to 20kHz.
Note 6: Performance measured using microphone inputs, unless otherwise stated.
Note 7: Performance measured using line inputs.
Note 8: Performance measured using DAC, unless otherwise stated. LRCLK = 8kHz, unless otherwise stated.
Note 9: In master-mode operation, the accuracy of the MCLK input proportionally determines the accuracy of the sample clock rate.
Note 10: C_B is in pF.

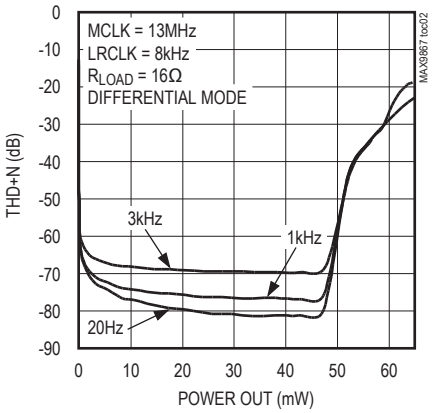
Typical Operating Characteristics

(V_{AVDD} = V_{DVDD} = V_{PVDD} = +1.8V, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{MICPGA} = 0dB, MCLK = 13MHz, LRCLK = 8kHz, BW = 20Hz to f_S/2, T_A = +25°C, unless otherwise noted.)

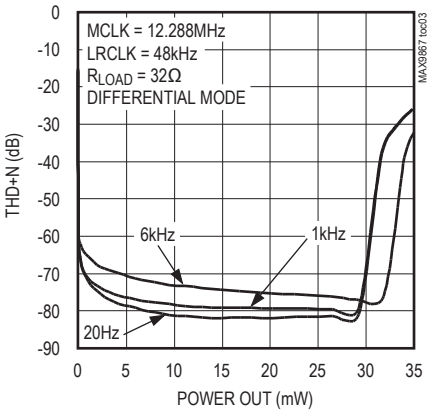
TOTAL HARMONIC DISTORTION + NOISE vs. POWER OUT (DAC TO HEADPHONE)



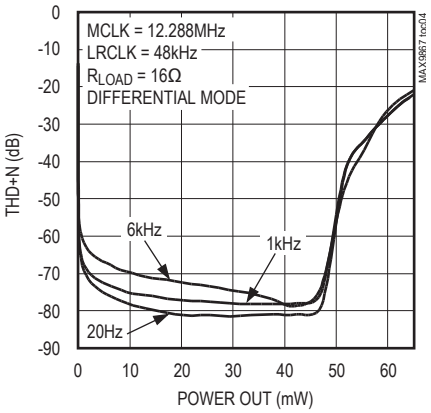
TOTAL HARMONIC DISTORTION + NOISE vs. POWER OUT (DAC TO HEADPHONE)



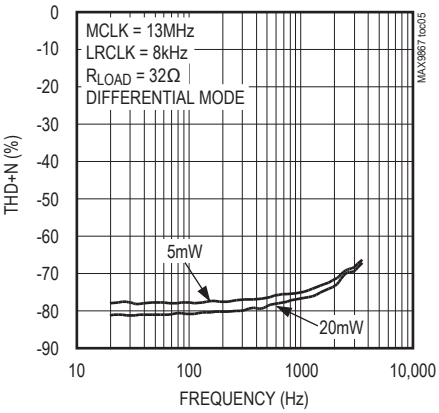
TOTAL HARMONIC DISTORTION + NOISE vs. POWER OUT (DAC TO HEADPHONE)



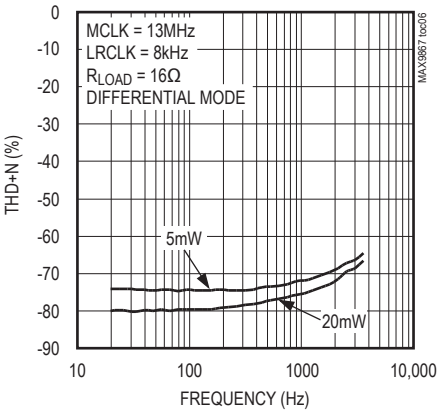
TOTAL HARMONIC DISTORTION + NOISE vs. POWER OUT (DAC TO HEADPHONE)



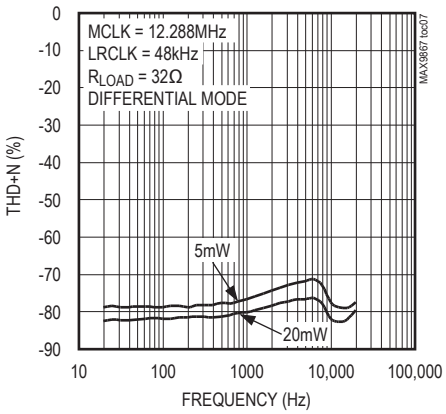
TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (DAC TO HEADPHONE)



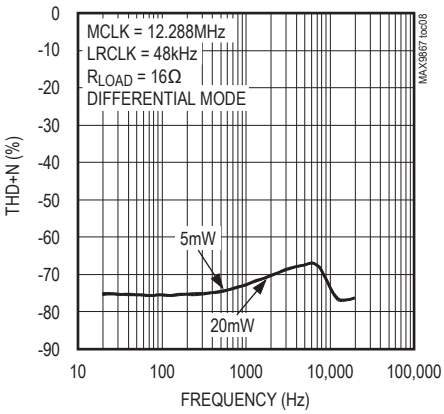
TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (DAC TO HEADPHONE)



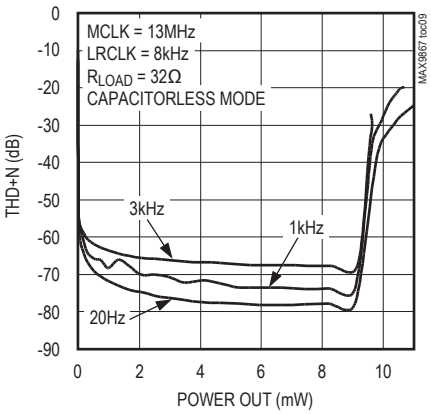
TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (DAC TO HEADPHONE)



TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (DAC TO HEADPHONE)



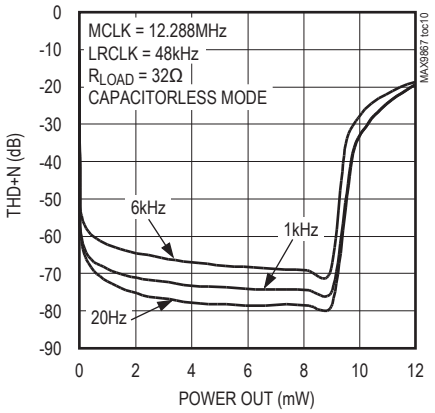
TOTAL HARMONIC DISTORTION + NOISE vs. POWER OUT (DAC TO HEADPHONE)



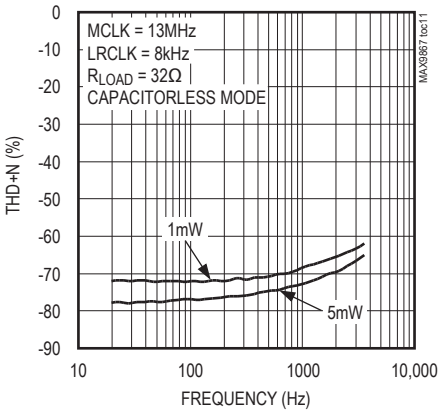
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{DVDD} = V_{PVDD} = +1.8V, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{MICPGA} = 0dB, MCLK = 13MHz, LRCLK = 8kHz, BW = 20Hz to f_S/2, T_A = +25°C, unless otherwise noted.)

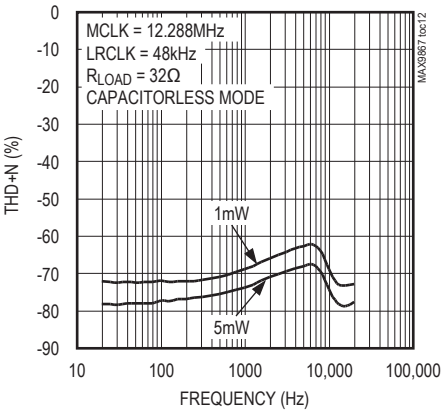
TOTAL HARMONIC DISTORTION + NOISE vs. POWER OUT (DAC TO HEADPHONE)



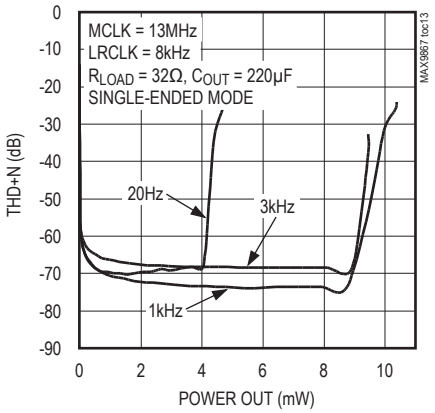
TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (DAC TO HEADPHONE)



TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (DAC TO HEADPHONE)



TOTAL HARMONIC DISTORTION + NOISE vs. POWER OUT (DAC TO HEADPHONE)



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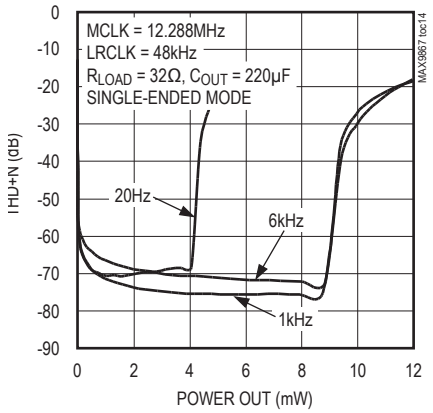
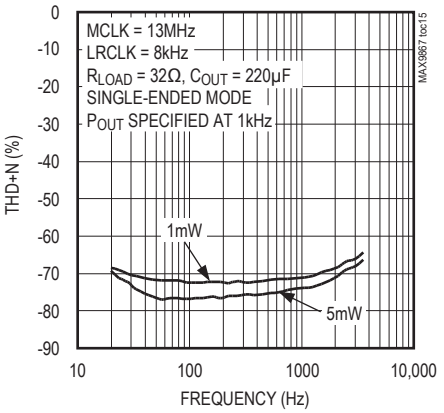
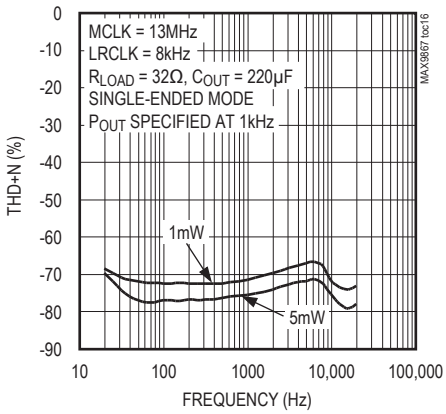


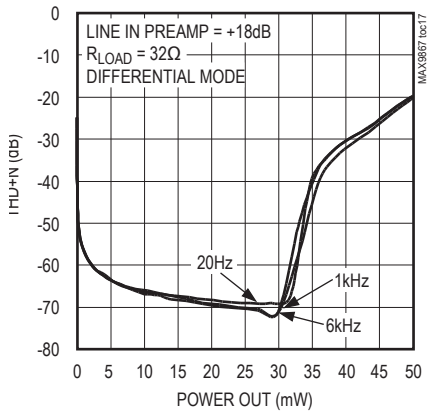
TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (DAC TO HEADPHONE)



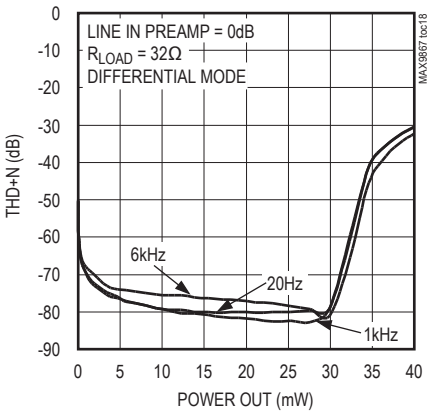
TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (DAC TO HEADPHONE)



TOTAL HARMONIC DISTORTION + NOISE vs. POWER OUT (LINE IN TO HEADPHONE)



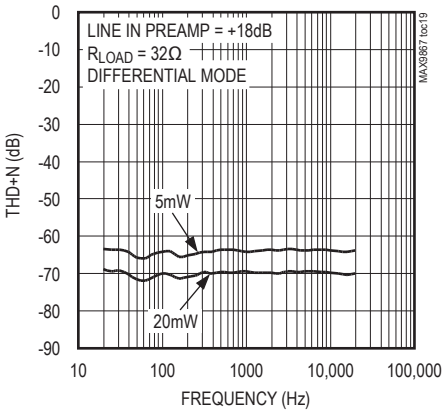
TOTAL HARMONIC DISTORTION + NOISE vs. POWER OUT (LINE IN TO HEADPHONE)



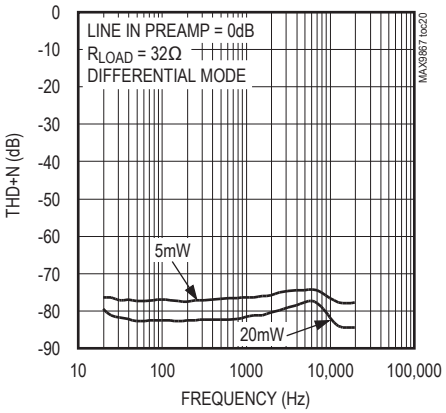
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{DVDD} = V_{PVDD} = +1.8V, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{MICPGA} = 0dB, MCLK = 13MHz, LRCLK = 8kHz, BW = 20Hz to f_S/2, T_A = +25°C, unless otherwise noted.)

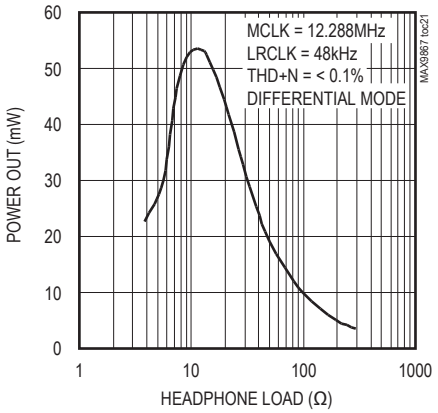
TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (LINE IN TO HEADPHONE)



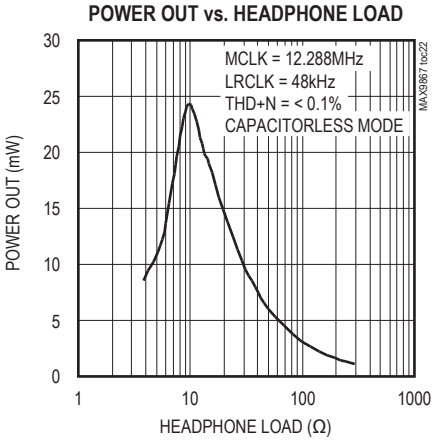
TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (LINE IN TO HEADPHONE)



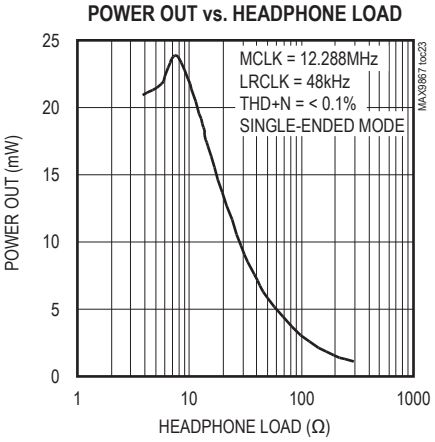
POWER OUT vs. HEADPHONE LOAD



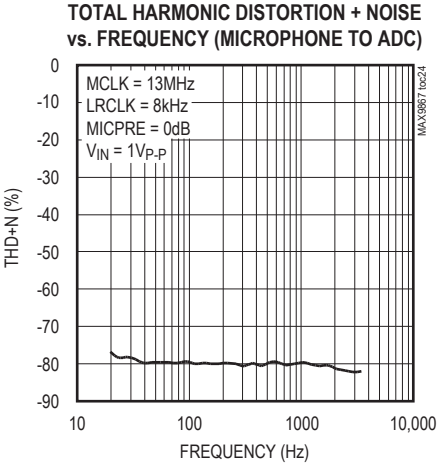
POWER OUT vs. HEADPHONE LOAD



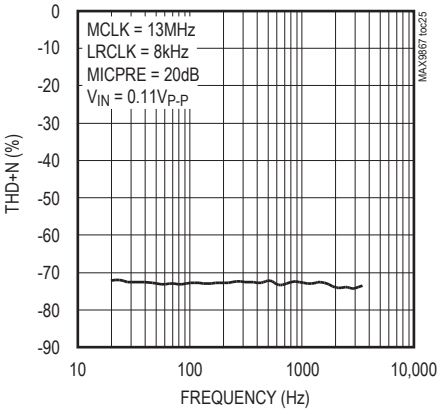
POWER OUT vs. HEADPHONE LOAD



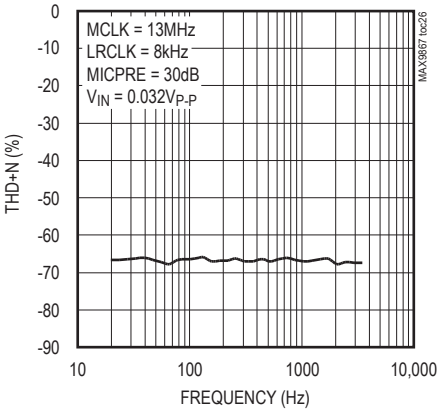
TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (MICROPHONE TO ADC)



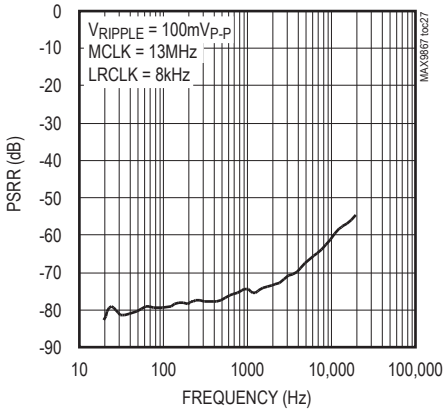
TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (MICROPHONE TO ADC)



TOTAL HARMONIC DISTORTION + NOISE vs. FREQUENCY (MICROPHONE TO ADC)



POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (DAC TO HEADPHONE)



Typical Operating Characteristics (continued)

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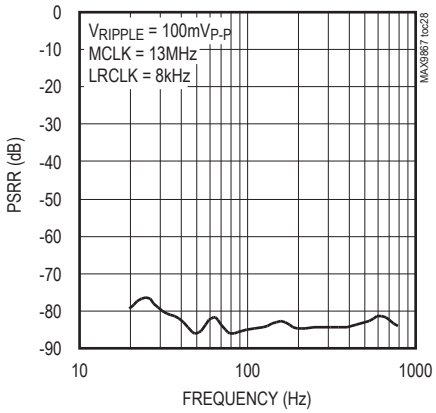
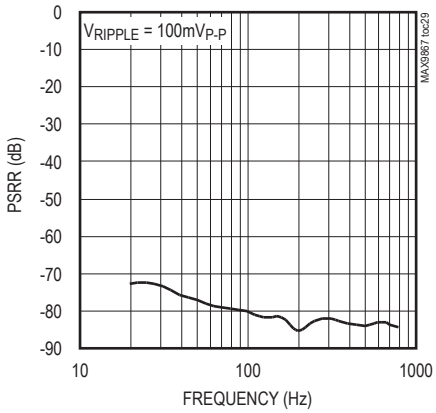
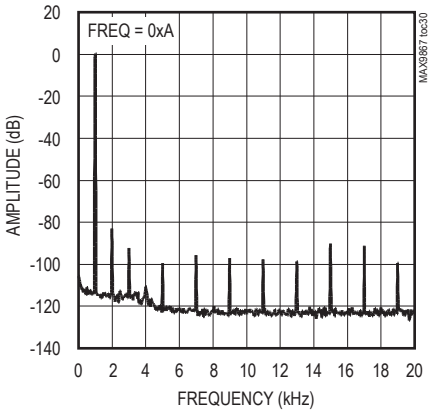
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (MIC TO ADC)



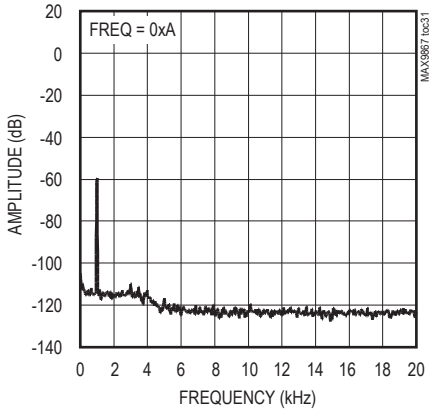
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY (MICBIAS)



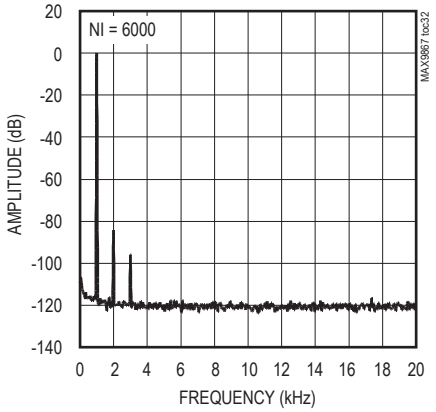
FFT, DAC TO HEADPHONE, 0dBFS, MCLK = 13MHz, LRCLK = 8kHz



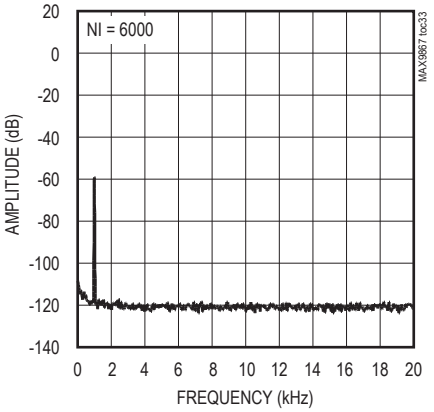
FFT, DAC TO HEADPHONE, -60dBFS, MCLK = 13MHz, LRCLK = 8kHz



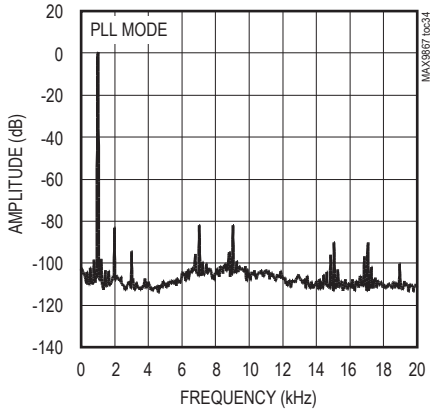
FFT, DAC TO HEADPHONE, 0dBFS, MCLK = 12.288MHz, LRCLK = 48kHz



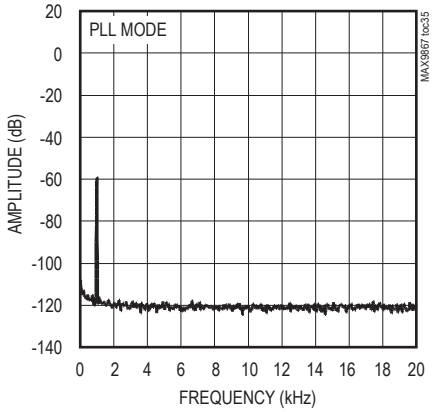
FFT, DAC TO HEADPHONE, -60dBFS, MCLK = 12.288MHz, LRCLK = 48kHz



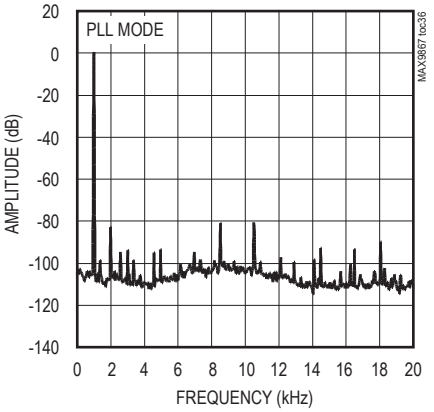
FFT, DAC TO HEADPHONE, 0dBFS, MCLK = 13MHz, LRCLK = 48kHz



FFT, DAC TO HEADPHONE, -60dBFS, MCLK = 13MHz, LRCLK = 48kHz



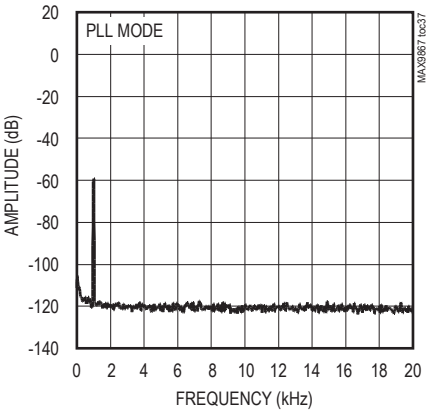
FFT, DAC TO HEADPHONE, 0dBFS, MCLK = 13MHz, LRCLK = 44.1kHz



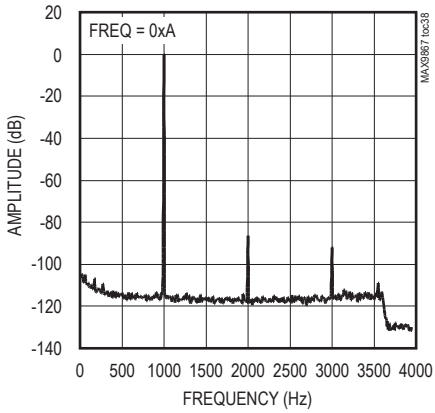
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{DVDD} = V_{PVDD} = +1.8V, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{MICPGA} = 0dB, MCLK = 13MHz, LRCLK = 8kHz, BW = 20Hz to $f_S/2$, T_A = +25°C, unless otherwise noted.)

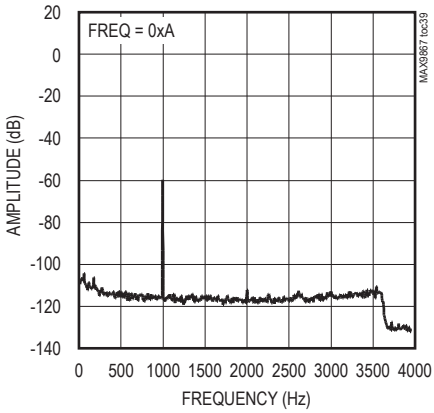
FFT, DAC TO HEADPHONE, -60dBFS, MCLK = 13MHz, LRCLK = 44.1kHz



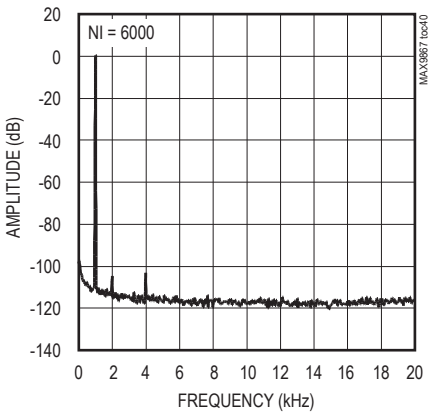
FFT, MICROPHONE TO ADC, 0dBFS, MCLK = 13MHz, LRCLK = 8kHz



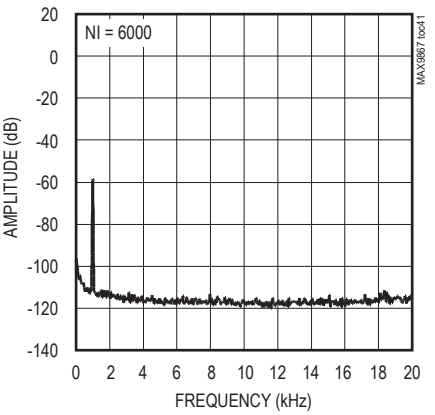
FFT, MICROPHONE TO ADC, -60dBFS, MCLK = 13MHz, LRCLK = 8kHz



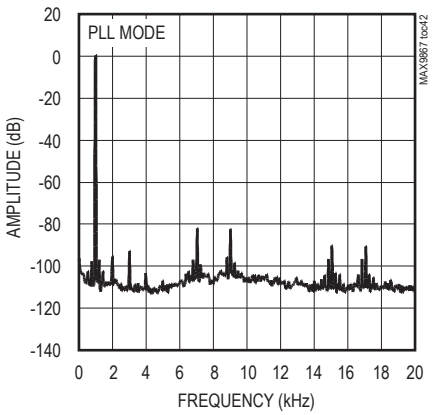
FFT, MICROPHONE TO ADC, 0dBFS, MCLK = 12.288MHz, LRCLK = 48kHz



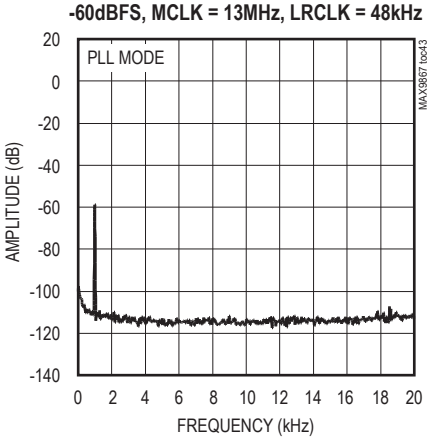
FFT, MICROPHONE TO ADC, -60dBFS, MCLK = 12.288MHz, LRCLK = 48kHz



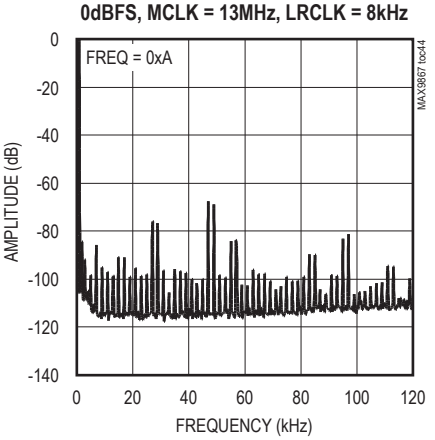
FFT, MICROPHONE TO ADC, 0dBFS, MCLK = 13MHz, LRCLK = 48kHz



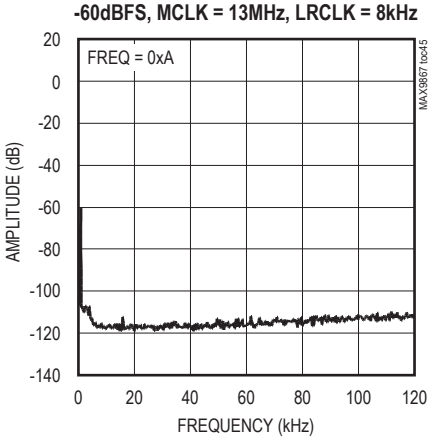
FFT, MICROPHONE TO ADC, -60dBFS, MCLK = 13MHz, LRCLK = 48kHz



WIDEBAND FFT, DAC TO HEADPHONE, 0dBFS, MCLK = 13MHz, LRCLK = 8kHz



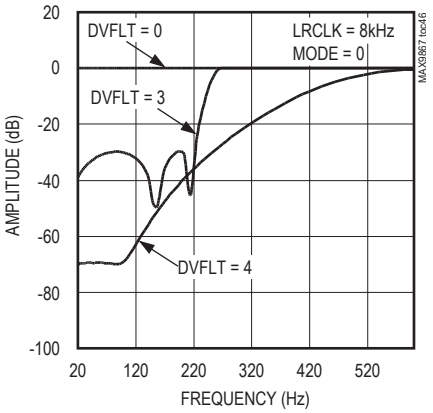
WIDEBAND FFT, DAC TO HEADPHONE, -60dBFS, MCLK = 13MHz, LRCLK = 8kHz



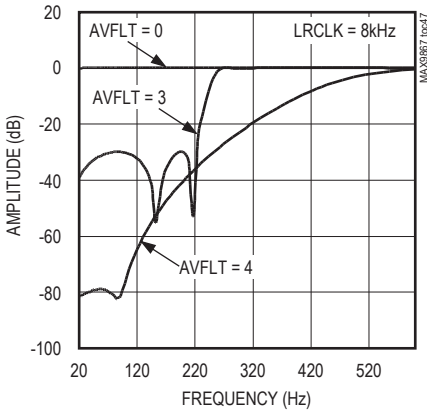
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{DVDD} = V_{PVDD} = +1.8V, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{MICPGA} = 0dB, MCLK = 13MHz, LRCLK = 8kHz, BW = 20Hz to $f_S/2$, T_A = +25°C, unless otherwise noted.)

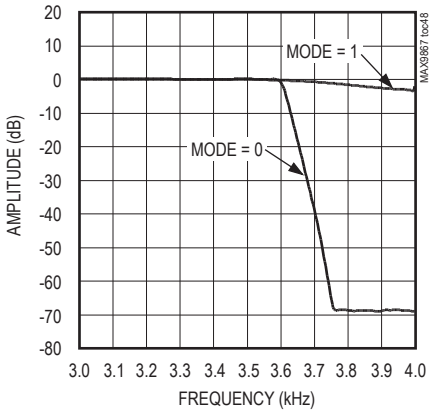
DAC IIR HIGHPASS FILTER FREQUENCY RESPONSE, MODE = 0



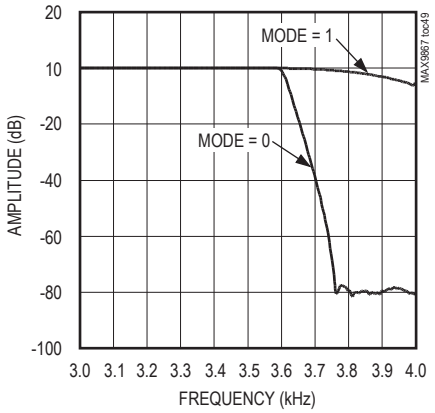
DAC IIR HIGHPASS FILTER FREQUENCY RESPONSE, MODE = 0



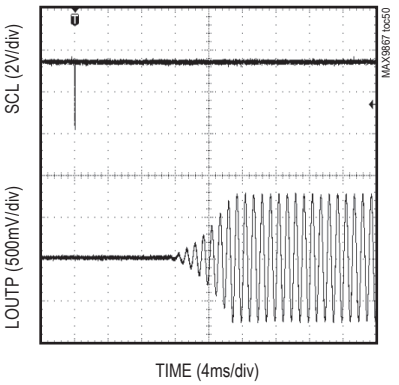
DAC IIR/FIR LOWPASS FILTER FREQUENCY RESPONSE (8kHz)



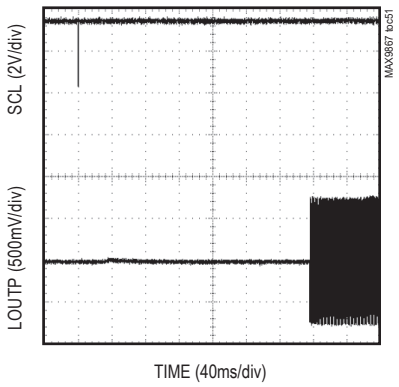
ADC IIR/FIR LOWPASS FILTER FREQUENCY RESPONSE (8kHz)



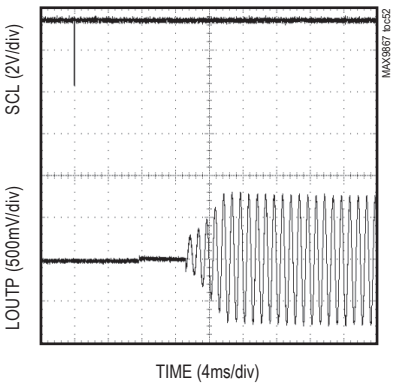
SHUTDOWN TO DAC FULL OPERATION (CAPACITORLESS OR DIFFERENTIAL MODE)



SHUTDOWN TO DAC FULL OPERATION (CLICKLESS SINGLE-ENDED MODE)



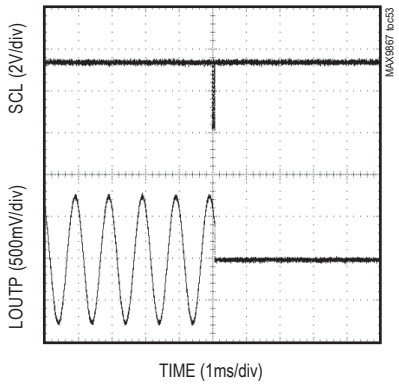
SHUTDOWN TO DAC FULL OPERATION (FAST TURN-ON SINGLE-ENDED MODE)



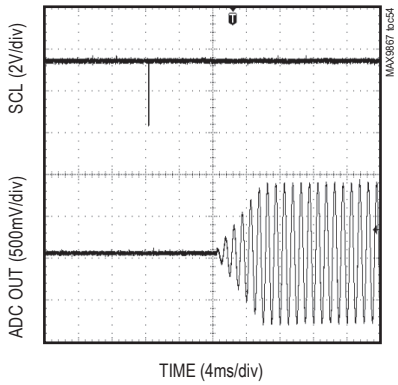
Typical Operating Characteristics (continued)

(V_{AVDD} = V_{DVDD} = V_{PVDD} = +1.8V, C_{REF} = 2.2µF, $C_{MICBIAS}$ = C_{PREG} = C_{REG} = 1µF, AV_{MICPGA} = 0dB, MCLK = 13MHz, LRCLK = 8kHz, BW = 20Hz to f_S/2, T_A = +25°C, unless otherwise noted.)

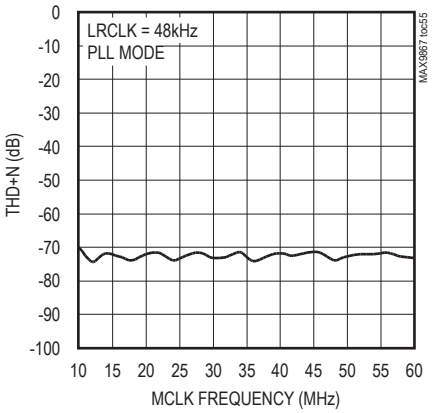
FULL OPERATION TO SHUTDOWN (DAC)



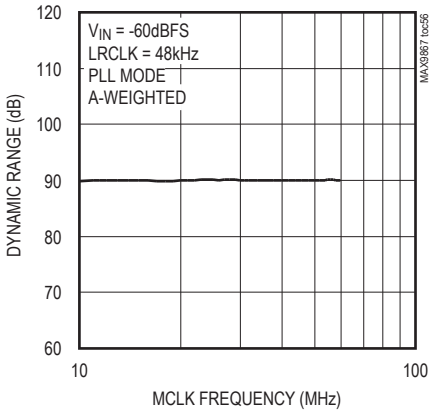
ADC SOFT-START



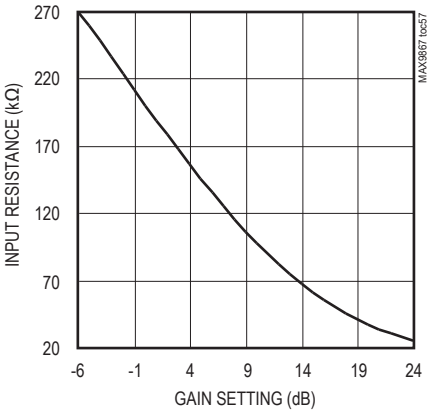
TOTAL HARMONIC DISTORTION + NOISE vs. MCLK FREQUENCY, 0dBFS



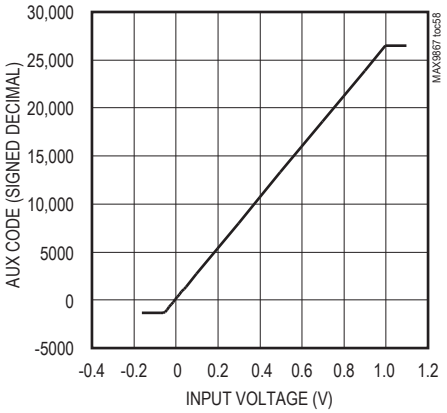
DYNAMIC RANGE vs. MCLK FREQUENCY



LINE INPUT RESISTANCE vs. GAIN SETTING



AUX CODE vs. INPUT VOLTAGE



Pin Description

PIN/BUMP		NAME	FUNCTION
TQFN-EP	WLP		
1	A2	DGND	Digital Ground
2	B3	SCL	I²C Serial-Clock Input. Connect a pullup resistor to a 1.7V to 3.3V supply.
3	A3	SDA	I²C Serial-Data Input/Output. Connect a pullup resistor to a 1.7V to 3.3V supply.
4	C3	$\overline{IRQ}$	Hardware Interrupt Output. $\overline{IRQ}$ can be programmed to pull low when bits in status register 0x00 are set. Read status register 0x00 to clear $\overline{IRQ}$ once set. Repeat faults have no effect on $\overline{IRQ}$ until it is cleared by reading register 0x00. Connect a 10kΩ pullup resistor to a 1.7V to 3.3V supply.
5	A4	AVDD	Analog Power Supply. Bypass to AGND with a 1µF capacitor.
6	B4	REF	Converter Reference. Bypass to AGND with a 2.2µF capacitor (1.23V nominal).
7	A5	PREG	Positive Internal Regulated Supply. Bypass to AGND with a 1µF capacitor (1.6V nominal).
8	B5	REG	PREG/2 Voltage Reference. Bypass to AGND with a 1µF capacitor (0.8V nominal).
9	A6	AGND	Analog Ground
10	B6	MICBIAS	Low-Noise Microphone Bias. Connect a 2.2kΩ to 470Ω resistor to the positive output of a microphone (1.525V nominal). Bypass to AGND with a 1µF capacitor.
11	C5	MICLN/ DIGMICCLK	Left Negative Differential Microphone Input or Digital Microphone Clock Output. For analog microphones, AC-couple to the negative output of a microphone with a 1µF capacitor. For digital microphones, connect to the clock input of the microphone.
12	C6	MICLP/ DIGMICDATA	Left Positive Differential Microphone Input or Digital Microphone Data Input. For analog microphones, AC-couple to the positive output of a microphone with a 1µF capacitor. For digital microphones, connect to the data output of the microphone(s). Up to two digital microphones can be connected.
13	C4	MICRP	Right Positive Differential Microphone Input. AC-couple to the positive output of a microphone with a 1µF capacitor.
14	D6	MICRN	Right Negative Differential Microphone Input. AC-couple to the negative output of a microphone with a 1µF capacitor.
15	D5	LINL	Left-Line Input. AC-couple analog audio signal to LINL with a 1µF capacitor.
16	E6	LINR	Right-Line Input. AC-couple analog audio signal to LINR with a 1µF capacitor.
17	D4	JACKSNS/AUX	Jack Sense or Auxiliary ADC Input. When configured for jack detection, JACKSNS detects the presence or absence of a jack. See the *Mode Configuration* section for details. When configured as an auxiliary ADC input, AUX is used to measure DC voltages.
18	E5	PGND	Headphone Power Ground
19	D3	ROUTP	Positive Right-Channel Headphone Output. Connect directly to the load in differential and capacitorless mode. AC-couple to the load in single-ended mode.
20	E4	ROUTN	Negative Right-Channel Headphone Output. Inverting output in differential mode. Leave unconnected in capacitorless and fast turn-on single-ended mode. Bypass with a 1µF capacitor to AGND in clickless, single-ended mode.
21	D2	LOUTN	Negative Left-Channel Headphone Output. Noninverting output in differential mode. Common headphone return in capacitorless mode. Leave unconnected in fast turn-on single-ended mode. Bypass with a 1µF capacitor to AGND in clickless single-ended mode.

Pin Description (continued)

PIN/BUMP		NAME	FUNCTION
TQFN-EP	WLP		
22	E3	LOUTP	Positive Left-Channel Headphone Output. Connect directly to the load in differential and capacitorless mode. AC-couple to the load in single-ended mode.
23	E2	PVDD	Headphone Power Supply. Bypass to PGND with a 1µF capacitor.
24, 25	—	N.C.	No Connection
26	E1	DVDDIO	Digital Audio Interface Power Supply. Bypass to DGND with a 1µF capacitor.
27	D1	SDOUT	Digital Audio Serial-Data ADC Output
28	C2	SDIN	Digital Audio Serial-Data DAC Input
29	C1	LRCLK	Digital Audio Left-Right Clock Input/Output. LRCLK is the audio sample rate clock and determines whether the audio data on SDIN is routed to the left or right channel. In TDM mode, LRCLK is a frame synchronization pulse. LRCLK is an input when the MAX9867 is in slave mode and an output when in master mode.
30	B1	BCLK	Digital Audio Bit Clock Input/Output. BCLK is an input when the MAX9867 is in slave mode and an output when in master mode.
31	B2	MCLK	Master Clock Input. Acceptable input frequency range: 10MHz to 60MHz.
32	A1	DVDD	Digital Power Supply. Supply for the digital circuitry and I^2C interface. Bypass to DGND with a 1µF capacitor.
—	—	EP	Exposed Pad. Connect the exposed thermal pad to AGND.

Detailed Description

The MAX9867 is a low-power stereo audio codec designed for portable applications requiring minimum power consumption.

The stereo playback path accepts digital audio through a flexible interface compatible with I^2S, TDM, and left-justified signals. An oversampling sigma-delta DAC converts the incoming digital data stream to analog audio and outputs the audio through the stereo headphone amplifier. The headphone amplifier can be configured in differential, single-ended, and capacitorless output modes.

The stereo record path has two analog microphone inputs with selectable gain. An integrated microphone bias can be used to power the microphones. The left analog microphone inputs can also accept data from up to two digital microphones. An oversampling sigmadelta ADC converts the microphone signals and outputs the digital bit stream over the digital audio interface.

Integrated digital filtering provides a range of notch and highpass filters for both the playback and record paths to limit undesirable low-frequency signals and GSM transmission noise. The digital filtering provides attenuation of out-of-band energy by over 70dB, eliminating audible aliasing. A digital sidetone function allows audio from the record path to be summed into the playback path after digital filtering.

The MAX9867 also includes two stereo, single-ended line inputs with gain adjustment, which can be recorded by the ADCs and/or output by the headphone amplifiers. An auxiliary ADC accurately measures a DC voltage by utilizing the right audio ADC and reporting the DC voltage through the I^2C interface. A jack detection function allows the detection of headphone, microphone, and headset jacks. Insertion and removal events can be programmed to trigger a hardware interrupt and flag an I^2C register bit.

The MAX9867's flexible clock circuitry utilizes a programmable clock divider and a digital PLL, allowing the DAC and ADC to operate at maximum dynamic range for all combinations of master clock (MCLK) and sample rate (LRCLK) without consuming extra supply current. Any master clock between 10MHz and 60MHz is supported as are all sample rates from 8kHz to 48kHz. Master and slave modes are supported for maximum flexibility.

I²C Registers

The MAX9867 audio codec is completely controlled through software using an I²C interface. The power-on default setting is complete shutdown, requiring that the internal registers be programmed to activate the device. See Table 1 for the device's complete register map.

I²C Slave Address

The MAX9867 responds to the slave address 0x30 for all write commands and 0x31 for all read operations.

Table 1. I²C Register Map

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REGISTER ADDRESS	POWER-ON RESET STATE
STATUS										
Status (Read Only)	CLD	SLD	ULK	0	0	0	JDET	0	0x00	—
Jack Sense (Read Only)	LSNS	JKSNS	JKMIC	0	0	0	0	0	0x01	—
AUX High (Read Only)	AUX[15:8]								0x02	—
AUX Low (Read Only)	AUX[7:0]								0x03	—
Interrupt Enable	ICLD	ISLD	IULK	0	0	$\overline{\text{SDODLY}}$	IJDET	0	0x04	0x00
CLOCK CONTROL										
System Clock	0	0	PSCLK		FREQ				0x05	0x00
Stereo Audio Clock Control High	PLL	NI[14:8]							0x06	0x00
Stereo Audio Clock Control Low	NI[7:1]							RLK/ NI[0]	0x07	0x00
DIGITAL AUDIO INTERFACE										
Interface Mode	MAS	WCI	BCI	DLY	HIZOFF	TDM	0	0	0x08	0x00
Interface Mode	0	0	0	LVOLFIX	DMONO	BSEL			0x09	0x00
DIGITAL FILTERING										
Codec Filters	MODE	AVFLT			0	DVFLT			0x0A	0x00
LEVEL CONTROL										
Sidetone	DSTS		0	DVST					0x0B	0x00
DAC Level	0	DACM	DACG		DACA				0x0C	0x00
ADC Level	AVL				AVR				0x0D	0x00
Left-Line Input Level	0	LILM	0	0	LIGL				0x0E	0x00
Right-Line Input Level	0	LIRM	0	0	LIGR				0x0F	0x00
Left Volume Control	0	VOLLM	VOLL						0x10	0x00
Right Volume Control	0	VOLRM	VOLR						0x11	0x00
Left Microphone Gain	0	PALEN	PGAML						0x12	0x00
Right Microphone Gain	0	PAREN	PGAMR						0x13	0x00
CONFIGURATION										
ADC Input	MXINL		MXINR		AUXCAP	AUXGAIN	AUXCAL	AUXEN	0x14	0x00
Microphone	MICCLK		DIGMICL	DIGMICR	0	0	0	0	0x15	0x00
Mode	DSLEW	$\overline{\text{VSEN}}$	$\overline{\text{ZDEN}}$	0	JDETEN	HPMODE			0x16	0x00
POWER MANAGEMENT										
System Shutdown	$\overline{\text{SHDN}}$	LNLEN	LNREN	0	DALEN	DAREN	ADLEN	ADREN	0x17	0x00
Revision	REV								0xFF	0x42

Device Status

Status registers 0x00 and 0x01 are read-only registers that report the status of various device functions. The status register bits are cleared upon reading the status register and are set the next time the event occurs. Registers 0x02 and 0x03 report the DC level applied to AUX. See the *ADC* section for more details and Table 2.

Table 2. Status Registers

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REGISTER ADDRESS
Status (Read Only)	CLD	SLD	ULK	0	0	0	JDET	0	0x00
Jack Sense (Read Only)	LSNS	JKSNS	JKMIC	0	0	0	0	0	0x01
AUX High (Read Only)	AUX[15:8]								0x02
AUX Low (Read Only)	AUX[7:0]								0x03

BITS	FUNCTION
CLD	**Clip Detect Flag** Indicates that a signal has reached or exceeded full scale in the ADC or DAC.
SLD	**Slew Level Detect Flag** When volume or gain changes are made, the slewing circuitry smoothly steps through all intermediate settings. When SLD is set high, all slewing has completed and the volume or gain is at its final value. SLD is also set when soft-start or stop is complete.
ULK	**Digital PLL Unlock Flag** Indicates that the digital audio PLL has become unlocked and digital signal data is not reliable.
JDET	**Headset Configuration Change Flag** JDET is set whenever there is a change in register 0x01, indicating that the headset configuration has changed.
LSNS	**LOUTP State (Valid if $\overline{\text{SHDN}}$ = 0, JDETEN = 1)** LSNS is set when the voltage at LOUTP exceeds AVDD - 0.4V. An internal pullup from AVDD to LOUTP causes this condition whenever there is no load on LOUTP. LSNS is only valid in differential and capacitorless output modes.
JKSNS	**JACKSNS State (Valid if JDETEN = 1)** JKSNS is set when the voltage at JACKSNS exceeds AVDD - 0.4V. An internal pullup from AVDD to JACKSNS causes this condition whenever there is no load on JACKSNS.
JKMIC	**Microphone Detection (Valid if PALEN or PAREN ≠ 00 and JDETEN = 1)** JKMIC is set when JACKSNS exceeds 0.95 x $V_{MICBIAS}$.
AUX	**Auxiliary Input Measurement** AUX is a 16-bit signed two's complement number representing the voltage measured at JACKSNS/AUX. Before reading a value from AUX, set AUXCAP to 1 to ensure a stable reading. After reading the value, set AUXCAP to 0. Use the following formula to convert the AUX value into an equivalent JACKSNS/AUX voltage: $\text{Voltage} = 0.738\text{V} \times \left(\frac{\text{AUX}}{\text{k}}\right)$ k = AUX value when AUXGAIN = 1. See the *ADC* section for complete details.

Hardware Interrupts

Hardware interrupts are reported on the open-drain $\overline{IRQ}$ pin. When an interrupt occurs, $\overline{IRQ}$ remains low until the interrupt is serviced by reading the status register 0x00. If a flag is set, it is reported as a hardware interrupt only if the corresponding interrupt enable is set. Each bit enables interrupts for the status flag in the respective bit location in register 0x00. See Table 3.

$\overline{SDODLY}$ is used to control the SDOUT timing. See the *Digital Audio Interface* section for a detailed description.

Clock Control

The MAX9867 can work with a master clock (MCLK) supplied from any system clock within the 10MHz-to-60MHz range. Internally, the MAX9867 requires a 10MHz-to-20MHz clock. A prescaler divides MCLK by 1, 2, or 4 to create the internal clock (PCLK). PCLK is used to clock all portions of the MAX9867. See Table 4.

The MAX9867 is capable of supporting any sample rate from 8kHz to 48kHz, including all common sample rates (8kHz, 16kHz, 24kHz, 32kHz, 44.1kHz, and 48kHz). To accommodate a wide range of system architectures, the MAX9867 supports three main clocking modes:

- **Normal:** This mode uses a 15-bit clock divider coefficient to set the sample rate relative to the prescaled MCLK input (PCLK). This allows high flexibility in both the MCLK and LRCLK frequencies and can be used in either master or slave mode.
- **Exact Integer:** In both master and slave mode, common MCLK frequencies (12MHz, 13MHz, 16MHz, and 19.2MHz) can be programmed to operate in exact integer mode for both 8kHz and 16kHz sample rates. In these modes, the MCLK and LRCLK rates are selected by using the FREQ bits instead of the NI and PLL control bits.
- **PLL:** When operating in slave mode, a PLL can be enabled to lock onto externally generated LRCLK signals that are not integer related to PCLK. Prior to enabling the interface, program NI to the nearest desired ratio and set the NI[0] = 1 to enable the PLL's rapid lock mode. If NI[0] = 0, then NI is ignored and PLL lock time is slower.

Table 3. Interrupt Register

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REGISTER ADDRESS
Interrupt Enable	ICLD	ISLD	IULK	0	0	$\overline{SDODLY}$	IJDET	0	0x04

Table 4. Clock Control Registers

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REGISTER ADDRESS
System Clock	0	0	PSCLK		FREQ				0x05
Stereo Audio Clock Control High	PLL	NI[14:8]							0x06
Stereo Audio Clock Control Low	NI[7:1]							NI[0]	0x07

BITS	FUNCTION
PSCLK	**MCLK Prescaler** Divides MCLK to generate a PCLK between 10MHz and 20MHz. 00 = Disable clock for low-power shutdown. 01 = Select if MCLK is between 10MHz and 20MHz. 10 = Select if MCLK is between 20MHz and 40MHz. 11 = Select if MCLK is between 40MHz and 60MHz.

Table 4. Clock Control Registers (continued)

<table>
<tr><th>BITS</th><th colspan="4">FUNCTION</th></tr>
<tr><td rowspan="9">FREQ</td><td colspan="4">Exact Integer Modes
Allows integer sampling for specific PCLK (prescaled MCLK) frequencies and 8kHz or 16kHz sample rates.</td></tr>
<tr><td>FREQ[3:0]</td><td>PCLK (MHz)</td><td>LRCLK (kHz)</td><td>PCLK/LRCLK</td></tr>
<tr><td>0x00</td><td colspan="3">Normal or PLL mode</td></tr>
<tr><td>0x1–0x7</td><td>Reserved</td><td>Reserved</td><td>Reserved</td></tr>
<tr><td>0x8
0x9</td><td>12
12</td><td>8
16</td><td>1500
750</td></tr>
<tr><td>0xA
0xB</td><td>13
13</td><td>8
16</td><td>1625
812.5</td></tr>
<tr><td>0xC
0xD</td><td>16
16</td><td>8
16</td><td>2000
1000</td></tr>
<tr><td>0xE
0xF</td><td>19.2
19.2</td><td>8
16</td><td>2400
1200</td></tr>
<tr><td colspan="4">Modes 0x8–0xF are available in either master or slave mode. In slave mode, if the indicated PCLK/LRCLK ratio cannot be guaranteed, use PLL mode instead.</td></tr>
<tr><td>PLL</td><td colspan="4">PLL Mode Enable
0= Valid for slave and master mode. The frequency of LRCLK is set by the NI divider bits. In master mode, the MAX9867 generates LRCLK using the specified divide ratio. In slave mode, the MAX9867 expects an LRCLK as specified by the divide ratio.
1= Valid for slave mode only. A digital PLL locks on to any externally supplied LRCLK signal.

Rapid Lock Mode
To enable rapid lock mode, set NI to the nearest desired ratio and set NI[0] = 1 before enabling the interface.</td></tr>
<tr><td>NI</td><td colspan="4">Normal Mode LRCLK Divider
When PLL = 0, the frequency of LRCLK is determined by NI. See Table 5 for common NI values.

$NI = (65536 \times 96 \times f_{LRCLK})/f_{PCLK}$

f_{LRCLK} = LRCLK frequency
f_{PCLK} = Prescaled MCLK internal clock frequency (PCLK)

LRCLK > 24kHz is only valid for MODE = 0 (stereo audio mode). MODE = 1 (voice mode) requires LRCLK ≤ 24kHz.</td></tr>
</table>

Table 5. Common NI Values

MCLK (MHz)	LRCLK (kHz)						
	PSCLK	**8**	**16**	**24**	**32**	**44.1**	**48**
11.2896	01	0x116A	0x22D4	0x343F	0x45A9	**0x6000**	0x687D
12	01	0x1062	0x20C5	0x3127	0x4189	0x5A51	0x624E
12.288	01	**0x1000**	**0x2000**	**0x3000**	**0x4000**	**0x5833**	**0x6000**
13	01	0x0F20	0x1E3F	0x2D5F	0x3C7F	0x535F	0x5ABE
19.2	01	0x0A3D	0x147B	0x1EB8	0x28F6	0x3873	0x3D71
24	10	0x1062	0x20C5	0x1893	0x4189	0x5A51	0x624E
26	10	0x0F20	0x1E3F	0x16AF	0x3C7F	0x535F	0x5ABE
27	10	0x0E90	0x1D21	0x15D8	0x3A41	0x5048	0x5762

Note: *Bolded values are exact integers that provide maximum full-scale performance.*

Digital Audio Interface

The MAX9867's digital audio interface supports a wide range of operating modes to ensure maximum compatibility. See Figures 1–4 for timing diagrams. In master mode, the MAX9867 outputs LRCLK and BCLK, while in slave mode they are inputs. When operating in master mode, BCLK can be configured in a number of ways to ensure compatiblity with other audio devices.

LVOLFIX is used to fix the line input playback volume to 0dB regardless of VOLL and VOLR. See the *Line Inputs* section for complete details and Table 6.

Table 6. Digital Audio Interface Registers

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REGISTER ADDRESS
Interface Mode	MAS	WCI	BCI	DLY	HIZOFF	TDM	0	0	0x08
Interface Mode	0	0	0	LVOLFIX	DMONO	BSEL			0x09

BITS	FUNCTION
MAS	**Master Mode** 0 = The MAX9867 operates in slave mode with LRCLK and BCLK configured as inputs. 1 = The MAX9867 operates in master mode with LRCLK and BCLK configured as outputs.
WCI	**LRCLK Invert** 0 = Left-channel data is input and output while LRCLK is low. 1 = Right-channel data is input and output while LRCLK is low. **Note:** WCI is ignored when TDM = 1.
BCI	**BCLK Invert** In master and slave modes: 0 = SDIN is latched into the part on the rising edge of BCLK. SDOUT transitions after the rising edge of BCLK as determined by $\overline{\text{SDODLY}}$. 1 = SDIN is latched into the part on the falling edge of BCLK. SDOUT transitions after the falling edge of BCLK as determined by $\overline{\text{SDODLY}}$. In master mode: 0 = LRCLK changes state immediately after the rising edge of BCLK. 1 = LRCLK changes state immediately after the falling edge of BCLK.
$\overline{\text{SDODLY}}$	**SDOUT Delay** 0 = SDOUT transitions one half BCLK cycle after SDIN is latched into the part. 1 = SDOUT transitions on the same BCLK edge as SDIN is latched into the part. See Figures 1–4 for complete details. See Register 0x04 (interrupt registers).
DLY	**Delay Mode** 0 = SDIN/SDOUT data is latched on the first BCLK edge following an LRCLK edge. 1 = SDIN/SDOUT data is assumed to be delayed one BCLK cycle so that it is latched on the 2nd BCLK edge following an LRCLK edge (I^2S-compatible mode). Note: DLY is ignored when TDM = 1.
HIZOFF	**SDOUT High-Impedance Mode** 0 = SDOUT goes to a high-impedance state after all data bits have been transferred out of the MAX9867, allowing SDOUT to be shared by other devices. 1 = SDOUT is set either high or low after all data bits have been transferred out of the MAX9867. **Note:** High-impedance mode is intended for use when TDM = 1.
LVOLFIX	See the *Line Inputs* section.

Table 6. Digital Audio Interface Registers (continued)

BITS	FUNCTION
TDM	**TDM Mode Select** 0 = LRCLK signal polarity indicates left and right audio. 1 = LRCLK is a framing pulse that transitions polarity to indicate the start of a frame of audio data consisting of multiple channels. When operating in TDM mode, the left channel is output immediately following the frame sync pulse. If right-channel data is being transmitted, the 2nd channel of data immediately follows the 1st channel data.
DMONO	**Mono Playback Mode** 0 = Stereo data input on SDIN is processed separately. 1 = Stereo data input on SDIN is mixed to a single channel and routed to both the left and right DAC.
BSEL	**BCLK Select** Configures BCLK when operating in master mode. BSEL has no effect in slave mode. Set BSEL = 010, unless sharing the bus with multiple devices: 000 = Off 001 = 64x LRCLK (192x internal clock divided by 3) 010 = 48x LRCLK (192x internal clock divided by 4) 011 = Reserved for future use. 100 = PCLK/2 101 = PCLK/4 110 = PCLK/8 111 = PCLK/16

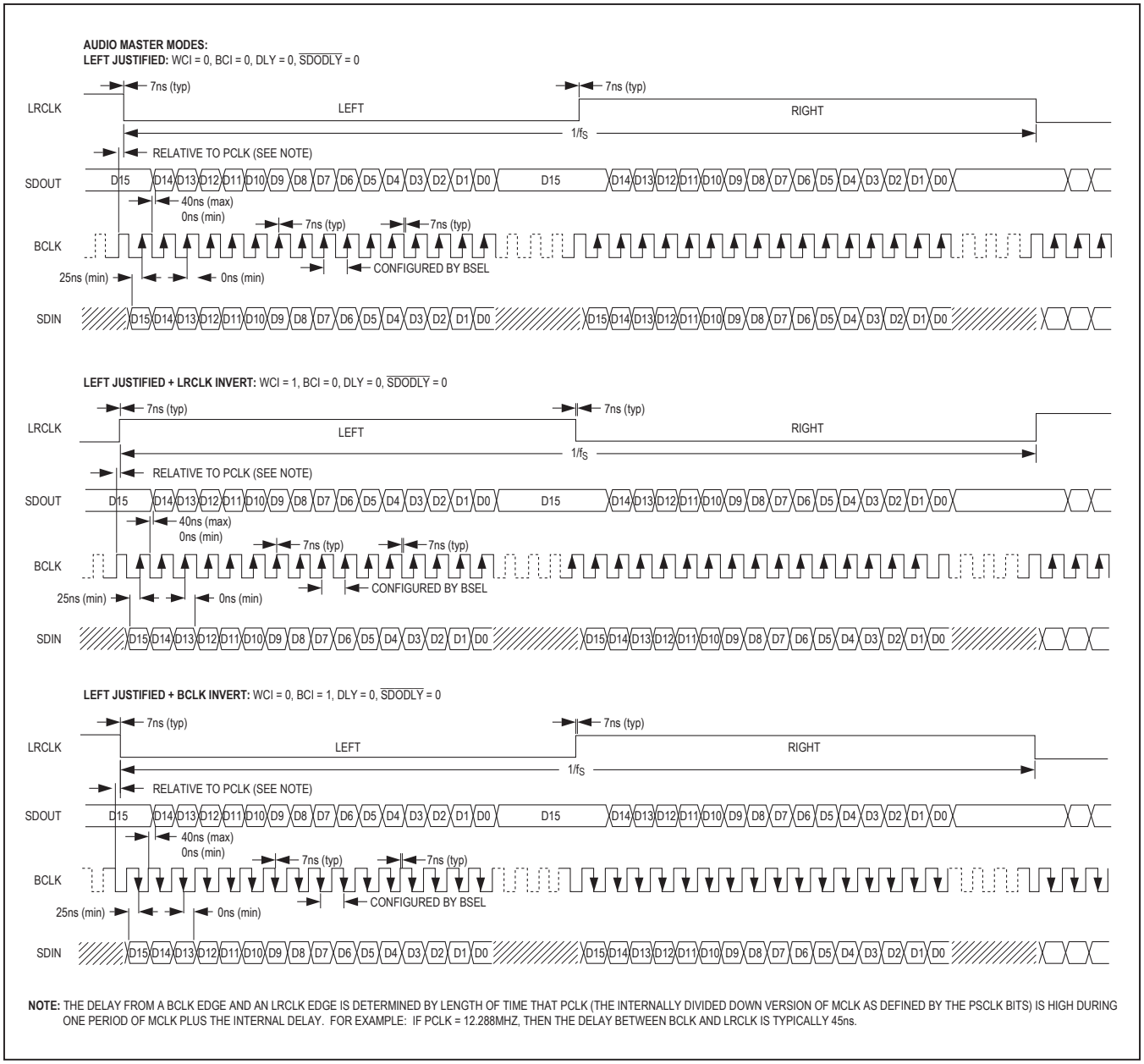


Figure 1. Digital Audio Interface Audio Master Mode Example (Sheet 1 of 2)

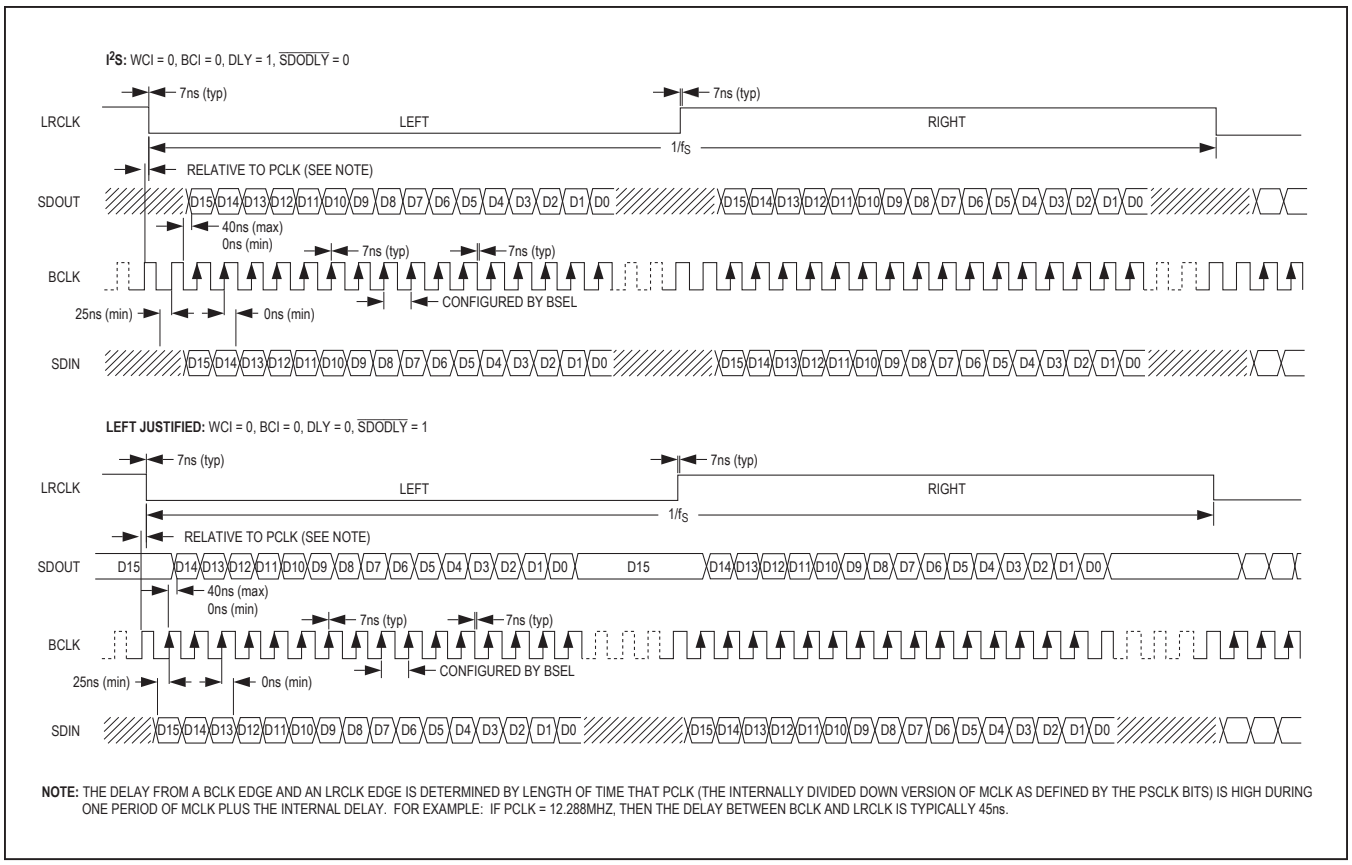
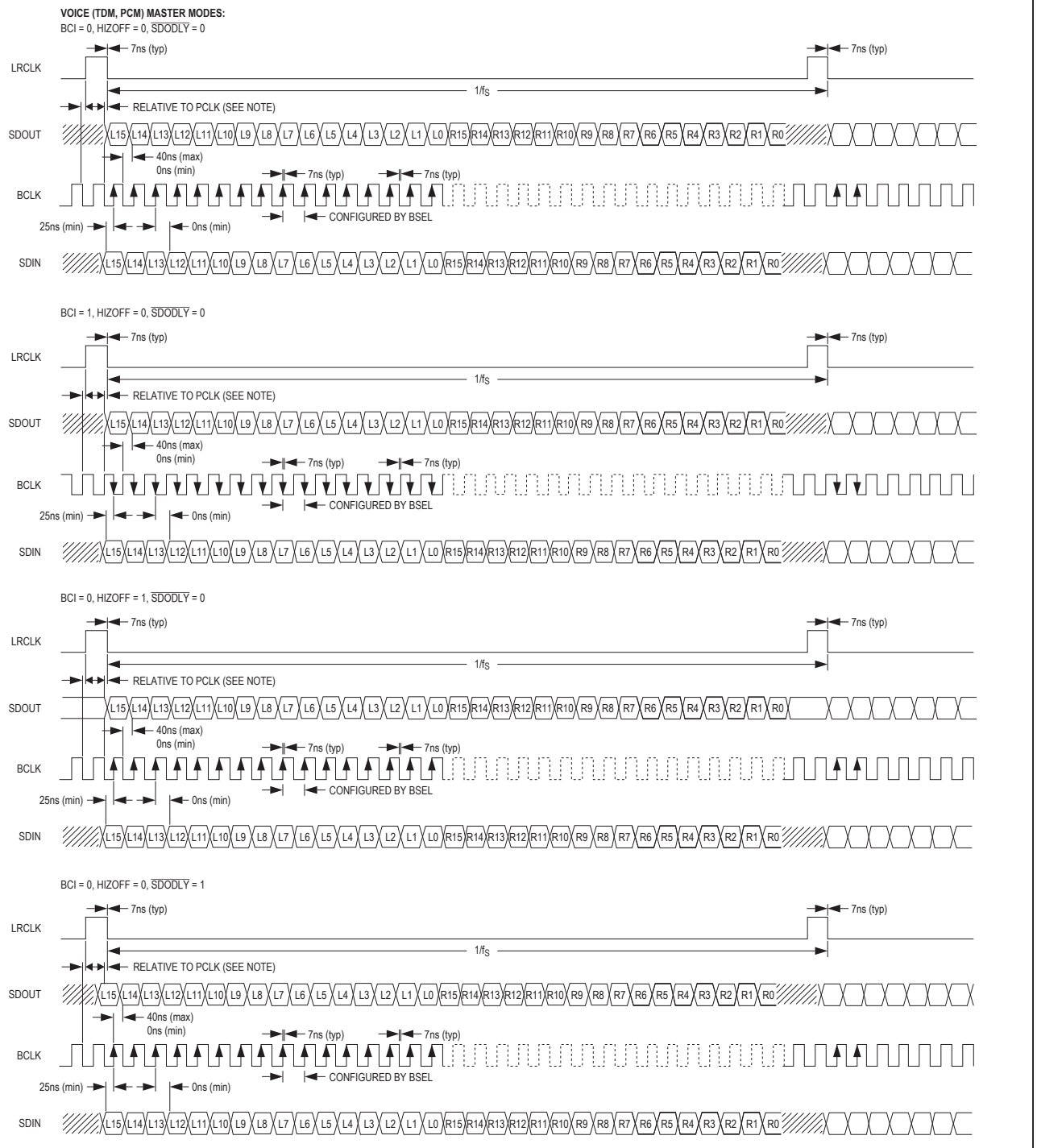


Figure 1. Digital Audio Interface Audio Master Mode Example (Sheet 2 of 2)



NOTE 1: THE DELAY FROM A BCLK EDGE AND AN LRCLK EDGE IS DETERMINED BY LENGTH OF TIME THAT PCLK (THE INTERNALLY DIVIDED DOWN VERSION OF MCLK AS DEFINED BY THE PSCLK BITS) IS HIGH DURING ONE PERIOD OF MCLK PLUS THE INTERNAL DELAY. FOR EXAMPLE: IF PCLK = 12.288MHZ, THEN THE DELAY BETWEEN BCLK AND LRCLK IS TYPICALLY 45NS.

Figure 2. Digital Audio Interface Voice Master Mode Examples

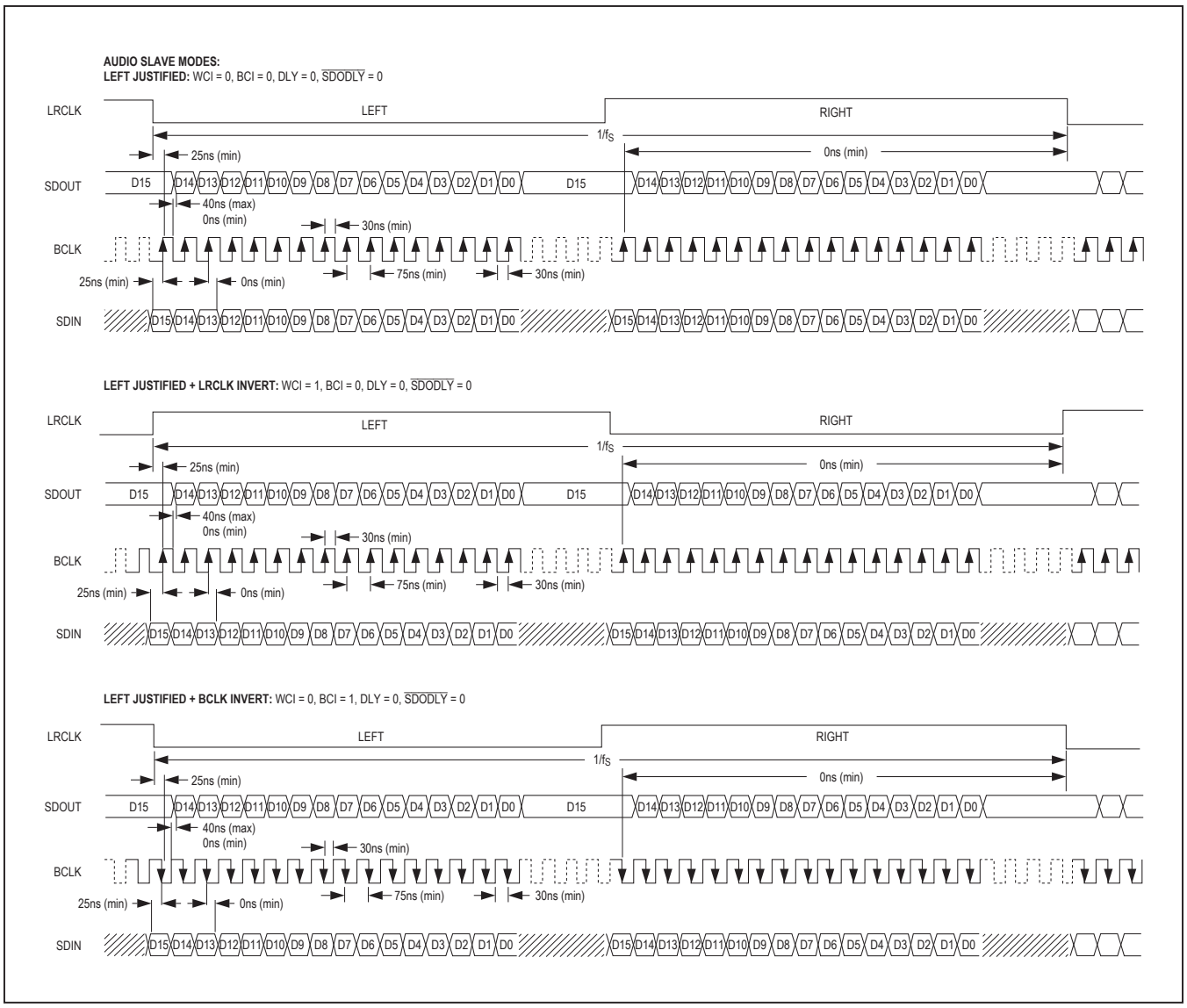


Figure 3. Digital Audio Interface Audio Slave Mode Examples (Sheet 1 of 2)

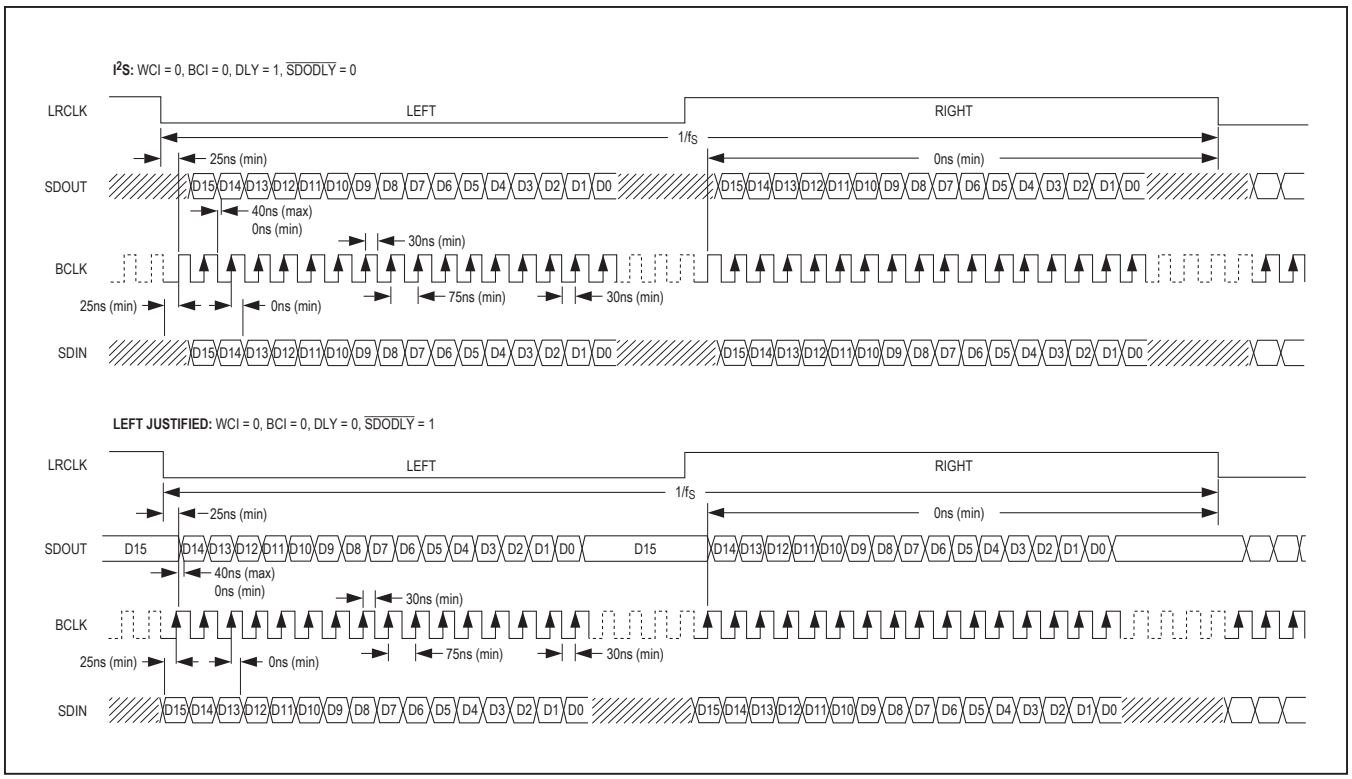


Figure 3. Digital Audio Interface Audio Slave Mode Examples (Sheet 2 of 2)

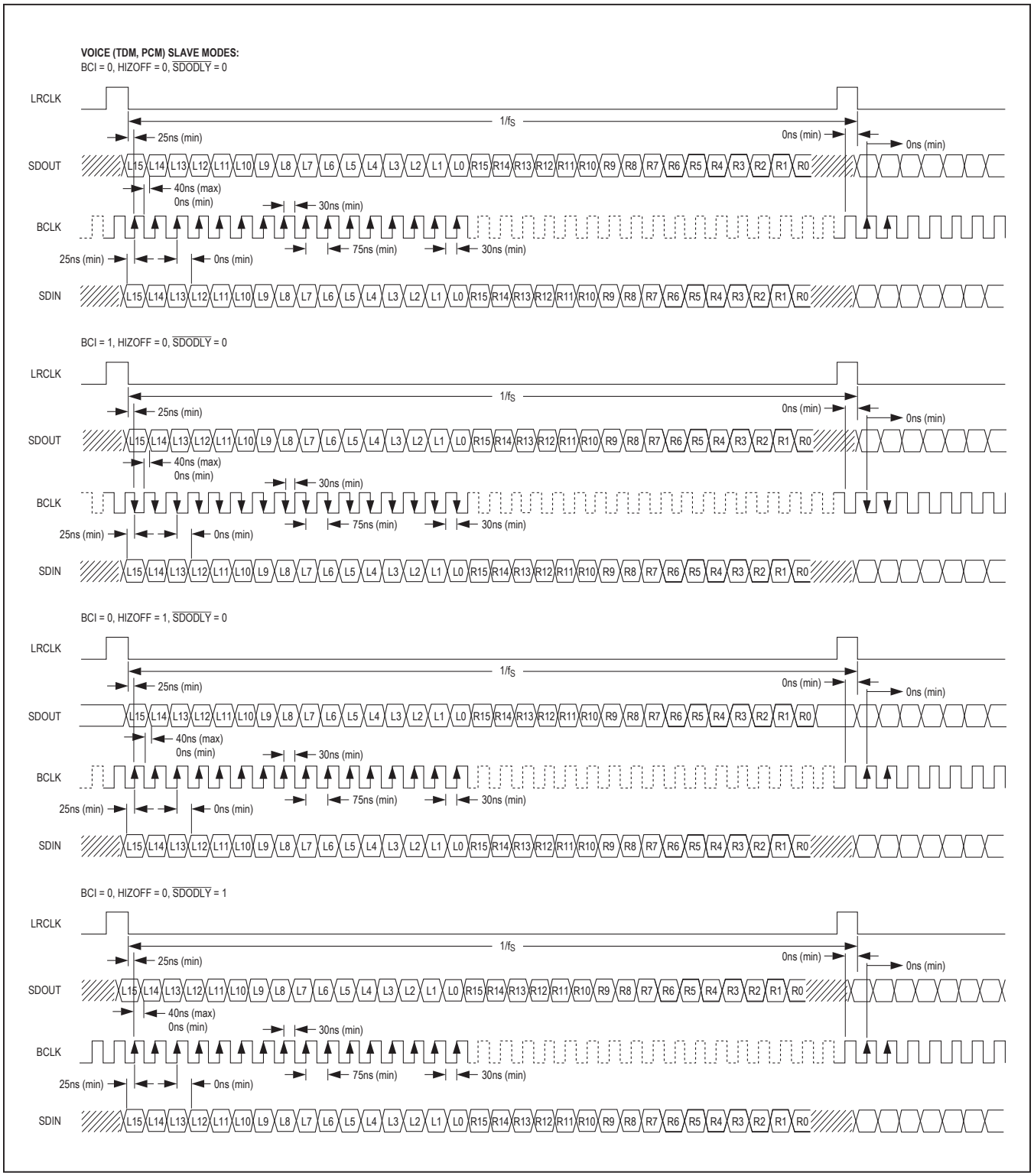


Figure 4. Digital Audio Interface Voice Slave Mode Examples

Digital Filtering

The MAX9867 incorporates both IIR (voice) and FIR (audio) digital filters to accomodate a wide range of audio sources. The IIR fiilters provide over 70dB of stopband attenuation as well as selectable highpass filters. The FIR filters provide low-power consumption and are linear phase to maintain stereo imaging. Table 7 is the digital filtering register.

Table 7. Digital Filtering Register

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REGISTER ADDRESS
Codec Filters	MODE	AVFLT			0	DVFLT			0x0A

BITS	FUNCTION
MODE	**Digital Audio Filter Mode** 0 = IIR Voice Filters 1 = FIR Audio Filters
AVFLT	**ADC Digital Audio Filter** **MODE = 0** Select the desired digital filter response from Table 8. See the Frequency Response graph in the *Typical Operating Characteristics* section for details on each filter. **MODE = 1** 0x0 = DC-blocking filter is disabled. Any other setting = DC-blocking filter is enabled.
DVFLT	**DAC Digital Audio Filter** **MODE = 0** Select the desired digital filter response from Table 8. See the Frequency Response graph in the *Typical Operating Characteristics* section for details on each filter. **MODE = 1** 0x0 = DC-blocking filter is disabled. Any other setting = DC-blocking filter is enabled.

Table 8. IIR Highpass Digital Filters

CODE	FILTER TYPE	INTENDED SAMPLE RATE (kHz)	HIGHPASS CORNER FREQUENCY (Hz)	217Hz NOTCH
0x0	Disabled			
0x1	Elliptical	16	256	Yes
0x2	Butterworth	16	500	No
0x3	Elliptical	8	256	Yes
0x4	Butterworth	8	500	No
0x5	Butterworth	8 to 24	$f_S/240$	No
0x6 to 0x7	Reserved			

Digital Gain Control

The MAX9867 includes digital gain adjustment for the playback and record paths. Independent gain adjustment is provided for the two record channels. Sidetone gain adjustment is also provided to set the sidetone level relative to the playback level. Table 9 is the digital gain registers.

Table 9. Digital Gain Registers

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REGISTER ADDRESS
Sidetone	DSTS		0	DVST					0x0B
DAC Level	0	DACM	DACG		DACA				0x0C
ADC Level	AVL				AVR				0x0D

BITS	FUNCTION
DSTS	**Digital Sidetone Source Mixer** 00 = No sidetone is selected. 01 = Left ADC 10 = Right ADC 11 = Left + right ADC
DVST	**Digital Sidetone Level Control** All gain settings are relative to the ADC input voltage.

Differential Headphone Output Mode

SETTING	GAIN (dB)	SETTING	GAIN (dB)	SETTING	GAIN (dB)
0x00	Off	0x0B	-20	0x16	-42
0x01	0	0x0C	-22	0x17	-44
0x02	-2	0x0D	-24	0x18	-46
0x03	-4	0x0E	-26	0x19	-48
0x04	-6	0x0F	-28	0x1A	-50
0x05	-8	0x10	-30	0x1B	-52
0x06	-10	0x11	-32	0x1C	-54
0x07	-12	0x12	-34	0x1D	-56
0x08	-14	0x13	-36	0x1E	-58
0x09	-16	0x14	-38	0x1F	-60
0x0A	-18	0x15	-40	—	—

Capacitorless and Single-Ended Headphone Output Mode

SETTING	GAIN (dB)	SETTING	GAIN (dB)	SETTING	GAIN (dB)
0x00	Off	0x0B	-25	0x16	-47
0x01	-5	0x0C	-27	0x17	-49
0x02	-7	0x0D	-29	0x18	-51
0x03	-9	0x0E	-31	0x19	-53
0x04	-11	0x0F	-33	0x1A	-55
0x05	-13	0x10	-35	0x1B	-57
0x06	-15	0x11	-37	0x1C	-59
0x07	-17	0x12	-39	0x1D	-61
0x08	-19	0x13	-41	0x1E	-63
0x09	-21	0x14	-43	0x1F	-65
0x0A	-23	0x15	-45	—	—

BITS	FUNCTION
DACM	**DAC Mute Enable** 0 = No mute 1 = Mute

Table 9. Digital Gain Registers (continued)

BITS	FUNCTION			
DACG	**DAC Gain** 00 = 0dB 01 = +6dB 10 = +12dB 11 = +18dB **Note:** DACG is only used when MODE = 0. If MODE = 1, the DAC level is only set by DACA.			
DACA	**DAC Level Control** DACA works in all modes.			
	SETTING	**GAIN (dB)**	**SETTING**	**GAIN (dB)**
	0x0	0	0x8	-8
	0x1	-1	0x9	-9
	0x2	-2	0xA	-10
	0x3	-3	0xB	-11
	0x4	-4	0xC	-12
	0x5	-5	0xD	-13
	0x6	-6	0xE	-14
	0x7	-7	0xF	-15
AVL/AVR	**ADC Left/Right Level Control**			
	SETTING	**GAIN (dB)**	**SETTING**	**GAIN (dB)**
	0x0	+3	0x8	-5
	0x1	+2	0x9	-6
	0x2	+1	0xA	-7
	0x3	0	0xB	-8
	0x4	-1	0xC	-9
	0x5	-2	0xD	-10
	0x6	-3	0xE	-11
	0x7	-4	0xF	-12

Line Inputs

The MAX9867 includes one pair of single-ended line inputs. When enabled, the line inputs connect directly to the headphone amplifier and can be optionally connected to the ADC for recording. Table 10 lists the line input registers.

Table 10. Line Input Registers

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REGISTER ADDRESS
Left-Line Input Level	0	LILM	0	0	LIGL				0x0E
Right-Line Input Level	0	LIRM	0	0	LIGR				0x0F

Table 10. Line Input Registers (continued)

<table>
<tr><th>BITS</th><th colspan="4">FUNCTION</th></tr>
<tr><td>LILM/LIRM</td><td colspan="4">Line-Input Left/Right Playback Mute
0 = Line input is connected to the headphone amplifiers.
1 = Line input is disconnected from the headphone amplifiers.</td></tr>
<tr><td rowspan="10">LIGL/LIGR</td><td colspan="4">Line-Input Left/Right Gain</td></tr>
<tr><td>SETTING</td><td>GAIN (dB)</td><td>SETTING</td><td>GAIN (dB)</td></tr>
<tr><td>0x0</td><td>+24</td><td>0x8</td><td>+8</td></tr>
<tr><td>0x1</td><td>+22</td><td>0x9</td><td>+6</td></tr>
<tr><td>0x2</td><td>+20</td><td>0xA</td><td>+4</td></tr>
<tr><td>0x3</td><td>+18</td><td>0xB</td><td>+2</td></tr>
<tr><td>0x4</td><td>+16</td><td>0xC</td><td>0</td></tr>
<tr><td>0x5</td><td>+14</td><td>0xD</td><td>-2</td></tr>
<tr><td>0x6</td><td>+12</td><td>0xE</td><td>-4</td></tr>
<tr><td>0x7</td><td>+10</td><td>0xF</td><td>-6</td></tr>
<tr><td>LVOLFIX</td><td colspan="4">Fix Line Input Volume
0 = Line input to headphone output volume tracks VOLL and VOLR bits.
1 = Line input to headphone output volume fixed at VOLL and VOLR bits.
See the Digital Audio Interface section.</td></tr>
</table>

Playback Volume

The MAX9867 incorporates volume and mute control to allow level control for the playback audio path. Program registers 0x10 and 0x11 to set the desired volume. See Table 11.

Table 11. Playback Volume Registers

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REGISTER ADDRESS
Left Volume Control	0	VOLLM	VOLL						0x10
Right Volume Control	0	VOLRM	VOLR						0x11

Table 11. Playback Volume Registers (continued)

<table>
<tr><th>BITS</th><th colspan="6">FUNCTION</th></tr>
<tr><td>VOLLM/VOLRM</td><td colspan="6">Left/Right Playback Mute
VOLLM and VOLRM mute both the DAC and line input audio signals.
0 = Audio playback is unmuted.
1 = Audio playback is muted
Note: VSEN has no effect on the mute function. When VOLLM or VOLRM is set, the output is muted immediately ($\overline{ZDEN}$ = 1) or at the next zero-crossing ($\overline{ZDEN}$ = 0).</td></tr>
<tr><td rowspan="16">VOLL/VOLR</td><td colspan="6">Left/Right Playback Volume
VOLL and VOLR control the playback volume for both the DAC and line input audio signals.</td></tr>
<tr><td>SETTING</td><td>GAIN (dB)</td><td>SETTING</td><td>GAIN (dB)</td><td>SETTING</td><td>GAIN (dB)</td></tr>
<tr><td>0x00</td><td>+6</td><td>0x0E</td><td>-5</td><td>0x1C</td><td>-42</td></tr>
<tr><td>0x01</td><td>+5.5</td><td>0x0F</td><td>-6</td><td>0x1D</td><td>-46</td></tr>
<tr><td>0x02</td><td>+5</td><td>0x10</td><td>-8</td><td>0x1E</td><td>-50</td></tr>
<tr><td>0x03</td><td>+4.5</td><td>0x11</td><td>-10</td><td>0x1F</td><td>-54</td></tr>
<tr><td>0x04</td><td>+4</td><td>0x12</td><td>-12</td><td>0x20</td><td>-58</td></tr>
<tr><td>0x05</td><td>+3.5</td><td>0x13</td><td>-14</td><td>0x21</td><td>-62</td></tr>
<tr><td>0x06</td><td>+3</td><td>0x14</td><td>-16</td><td>0x22</td><td>-66</td></tr>
<tr><td>0x07</td><td>+2</td><td>0x15</td><td>-18</td><td>0x23</td><td>-70</td></tr>
<tr><td>0x08</td><td>+1</td><td>0x16</td><td>-20</td><td>0x24</td><td>-74</td></tr>
<tr><td>0x09</td><td>0</td><td>0x17</td><td>-22</td><td>0x25</td><td>-78</td></tr>
<tr><td>0x0A</td><td>-1</td><td>0x18</td><td>-26</td><td>0x26</td><td>-82</td></tr>
<tr><td>0x0B</td><td>-2</td><td>0x19</td><td>-30</td><td>0x27</td><td>-84</td></tr>
<tr><td>0x0C</td><td>-3</td><td>0x1A</td><td>-34</td><td rowspan="2">0x28 to 0x3F</td><td rowspan="2">MUTE</td></tr>
<tr><td>0x0D</td><td>-4</td><td>0x1B</td><td>-38</td></tr>
<tr><td colspan="6">Note: Gain settings apply when the headphone amplifier is configured in differential mode. In the single-ended and capacitorless modes, the actual gain is 5dB lower for each setting.</td></tr>
</table>

Microphone Inputs

Two differential microphone inputs and a low-noise microphone bias for powering the microphones are provided by the MAX9867. In typical applications, the left microphone records a voice signal and the right microphone records a background noise signal. In applications that require only one microphone, use the left microphone input and disable the right ADC. The microphone signals are amplified by two stages of gain and then routed to the ADCs. The first stage offers selectable 0dB, 20dB, or 30dB settings. The second stage is a programmable gain amplifier (PGA) adjustable from 0dB to 20dB in 1dB steps. Zero-crossing detection is included on the PGA to minimize zipper noise while making gain changes. See Figure 5 for a detailed diagram of the microphone input structure. Table 12 is the microphone input register.

Table 12. Microphone Input Registers

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REGISTER ADDRESS
Left Microphone Gain	0	PALEN		PGAML					0x12
Right Microphone Gain	0	PAREN		PGAMR					0x13

Table 12. Microphone Input Registers (continued)

<table>
<tr><th>BITS</th><th colspan="4">FUNCTION</th></tr>
<tr><td>PALEN/PAREN</td><td colspan="4">Left/Right Microphone Preamplifier Gain
Enables the microphone circuitry and sets the preamplifier gain.
00 = Disabled
01 = 0dB
10 = +20dB
11 = +30dB</td></tr>
<tr><td rowspan="13">PGAML/PGAMR</td><td colspan="4">Left/Right Microphone Programmable Gain Amplifier</td></tr>
<tr><td>SETTING</td><td>GAIN (dB)</td><td>SETTING</td><td>GAIN (dB)</td></tr>
<tr><td>0x00</td><td>+20</td><td>0x0B</td><td>+9</td></tr>
<tr><td>0x01</td><td>+19</td><td>0x0C</td><td>+8</td></tr>
<tr><td>0x02</td><td>+18</td><td>0x0D</td><td>+7</td></tr>
<tr><td>0x03</td><td>+17</td><td>0x0E</td><td>+6</td></tr>
<tr><td>0x04</td><td>+16</td><td>0x0F</td><td>+5</td></tr>
<tr><td>0x05</td><td>+15</td><td>0x10</td><td>+4</td></tr>
<tr><td>0x06</td><td>+14</td><td>0x11</td><td>+3</td></tr>
<tr><td>0x07</td><td>+13</td><td>0x12</td><td>+2</td></tr>
<tr><td>0x08</td><td>+12</td><td>0x13</td><td>+1</td></tr>
<tr><td>0x09</td><td>+10</td><td rowspan="2">0x14
to 0x1F</td><td rowspan="2">0</td></tr>
<tr><td>0x0A</td><td>+11</td></tr>
</table>

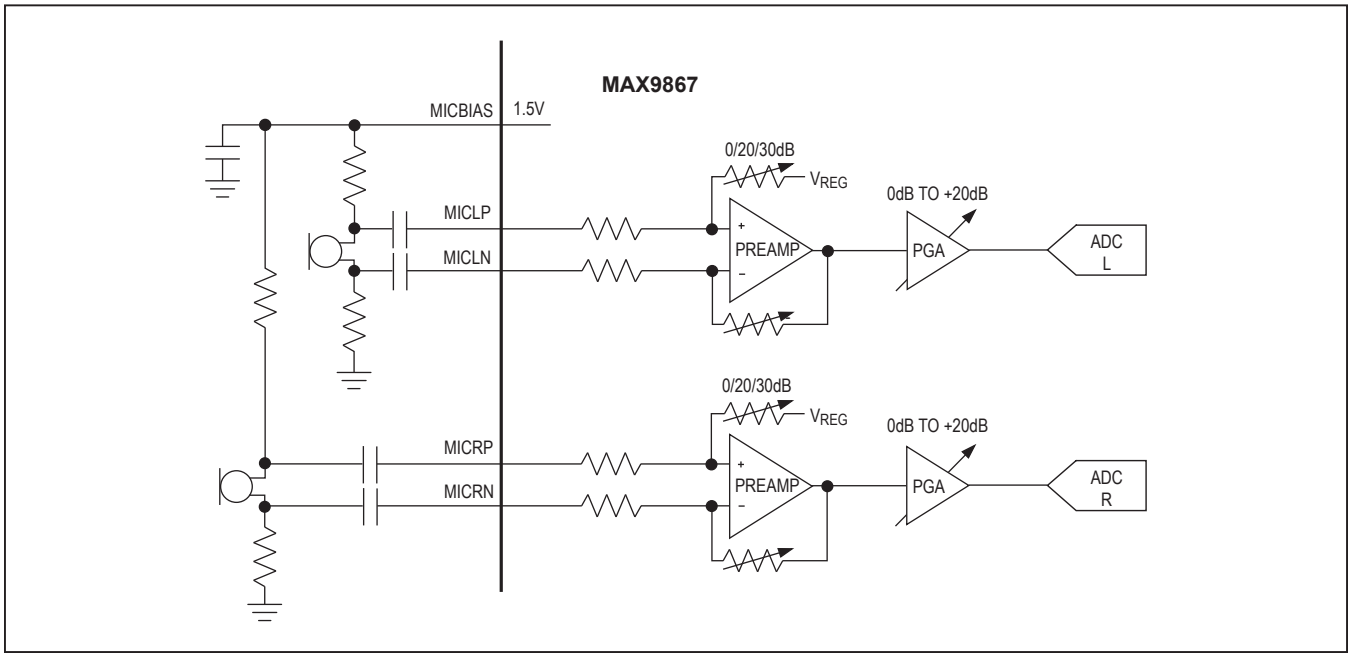


Figure 5. Microphone Input Signal Path

ADC

The MAX9867 includes two 16-bit ADCs. The first ADC is used to record left-channel microphone and line-input audio signals. The second ADC can be used to record right-channel microphone and line-input signals, or it can be configured to accurately measure DC voltages.

When measuring DC voltages, both the left and right ADCs must be enabled by setting ADLEN and ADREN in register 0x17. The input to the second ADC is JACKSNS

AUX and the output is reported in AUX (registers 0x02 and 0x03). Since the audio ADC is used to perform the measurement, the digital audio interface must be properly configured. If the left ADC is being used to convert audio, the DC measurement is performed at the same sample rate. When not using the left ADC, configure the digital interface for a 48kHz sample rate to ensure the fastest possible settling time.

To ensure accurate results, the MAX9867 includes two calibration routines. Calibrate the ADC each time the MAX9867 is powered on. Calibration settings are not lost if the MAX9867 is placed in shutdown. When making a measurement, set AUXCAP to 1 to prevent AUX from changing while reading the registers.

Setup Procedure

1) Ensure a valid MCLK signal is provided and configure PSCLK appropriately.
2) Choose a clocking mode. The following options are possible:
   - **Slave mode with LRCLK and BCLK signals provided.** The measurement sample rate is determined by the external clocks.
   - **Slave mode with no LRCLK and BCLK signals provided.** Configure the device for normal clock mode using the NI ratio. Select f_S = 48kHz to allow for the fastest settling times.
   - **Master mode with audio.** Configure the device in normal mode using the NI ratio or exact integer mode using FREQ as required by the audio signal.
   - **Master mode without audio.** Configure the device in normal mode using the NI ratio. Select f_S = 48kHz to allow for the fastest settling times.
3) Ensure JACKSNS is disabled.
4) Enable the left and right ADC; take the MAX9867 out of shutdown.

Offset Calibration Procedure

Perform the following steps before the first DC measurement is taken after applying power to the MAX9867:

Table 13. AUX ADC Wait Times

WAIT TIMES	
LRCLK (kHz)	**WAIT TIME (ms)**
48	40
44.1	44
32	60
24	80
22.05	90
16	120
12	160
11.025	175
8	240

1) Enable the AUX input (AUXEN = 1).
2) Enable the offset calibration (AUXCAL = 1).
3) Wait the appropriate time (see Table 13).
4) Complete calibration (AUXCAL = 0).

Gain Calibration Procedure

Perform the following steps the first time a DC measurement is taken after applying power to the MAX9867 or if the temperature changes significantly:

1) Enable the AUX input (AUXEN = 1).
2) Start gain calibration (AUXGAIN = 1).
3) Wait the appropriate time (see Table 13).
4) Freeze the measurement results (AUXCAP = 1).
5) Read AUX and store the value in memory to correct all future measurements (k = AUX[15:0], k is typically 19500).
6) Complete calibration (AUXGAIN = AUXCAP = 0).

DC Measurement Procedure

Perform the following steps after offset and gain calibration are complete:

1. Enable the AUX input (AUXEN = 1).
2. Wait the appropriate time (see Table 13).
3. Freeze the measurement results (AUXCAP = 1).
4. Read AUX and correct with the gain calibration value:

$$V_{AUX} = 0.738\left(\frac{AUX[15:0]}{k}\right)$$

5. Complete measurement (AUXCAP = 0).

Complete DC Measurement Example

MCLK = 13MHz, slave mode, BCLK and LRCLK not externally supplied:

1) Configure the digital audio interface for fS = 48kHz (PSCLK = 01, FREQ = 0x0, PLL = 0, NI = 0x5ABE, MAS = 0).
2) Disable JACKSNS (JDETEN = 0).
3) Enable the left and right ADC; take the MAX9867 out of shutdown (ADLEN = ADREN = $\overline{SHDN}$ = 1).
4) Calibrate the offset:
   a. Enable the AUX input (AUXEN = 1).
   b. Enable the offset calibration (AUXCAL = 1).
   c. Wait 40ms.
   d. Complete calibration (AUXCAL = 0).
5) Calibrate the gain:
   a. Start gain calibration (AUXGAIN = 1).
   b. Wait 40ms.
   c. Freeze the measurement results (AUXCAP = 1).
   d. Read AUX and store the value in memory to correct all future measurements (k = AUX[15:0]).
   e. Complete calibration (AUXGAIN = AUXCAP = AUXEN = 0).
6) Measure the voltage on JACKSNS/AUX:
   a. Enable the AUX input (AUXEN = 1).
   b. Wait 40ms.
   c. Freeze the measurement results (AUXCAP = 1).
   d. Read AUX and correct with the gain calibration value.
   e. Complete measurement (AUXCAP = 0).
7) DC measurement complete.

Table 14. ADC Input Register

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REGISTER ADDRESS
ADC Input	MXINL		MXINR		AUXCAP	AUXGAIN	AUXCAL	AUXEN	0x14

BITS	FUNCTION
MXINL/MXINR	**Left/Right ADC Audio Input Mixer** 00 = No input is selected. 01 = Left/right analog microphone 10 = Left/right line input 11 = Left/right analog microphone + line input **Note:** If the right-line input is disabled, then the left-line input is connected to both mixers. Enabling the left and right digital microphones disables the left and right audio mixers, respectively. See DIGMICL/ DIGMICR in Table 15 for more details.
AUXCAP	**Auxiliary Input Capture** 0 = Update AUX with the voltage at JACKSNS/AUX. 1 = Hold AUX for reading.
AUXGAIN	**Auxiliary Input Gain Calibration** 0 = Normal operation 1 = The input buffer is disconnected from JACKSNS/AUX and connected to an internal voltage reference. While in this mode, read the AUX register and store the value. Use the stored value as a gain calibration factor, K, on subsequent readings.
AUXCAL	**Auxiliary Input Offset Calibration** 0 = Normal operation 1 = JACKSNS/AUX is disconnected from the input and the ADC automatically calibrates out any internal offsets.
AUXEN	**Auxiliary Input Enable** 0 = Use JACKSNS/AUX for jack detection. 1 = Use JACKSNS/AUX for DC measurements. **Note:** For AUXEN = 1, set MXINR = 00, ADLEN = 1, and ADREN = 1.

Digital Microphone Input

The MAX9867 can accept audio from up to two digital microphones. When using digital microphones, the left analog microphone input is retasked as a digital microphone input. The right analog microphone input is still available to allow a combination of analog and digital microphones to be used. Figure 6 shows the digital microphone interface timing diagram. See Table 15.

Table 15. Digital Microphone Input Register

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REGISTER ADDRESS
Microphone	MICCLK		DIGMICL	DIGMICR	0	0	0	0	0x15

BITS	FUNCTION			
MICCLK	**Digital Microphone Clock** 00 = PCLK/8 01 = PCLK/6 10 = Reserved 11 = Reserved			
DIGMICL/DIGMICR	**Digital Left/Right Microphone Enable**			
	DIGMICL	**DIGMICR**	**Left ADC Input**	**Right ADC Input**
	0	0	ADC input mixer	ADC input mixer
	0	1	Line input (left analog microphone unavailable)	Right digital microphone
	1	0	Left digital microphone	ADC input mixer
	1	1	Left digital microphone	Right digital microphone
	Note: The left analog microphone input is never available when DIGMICL or DIGMICR = 1.			

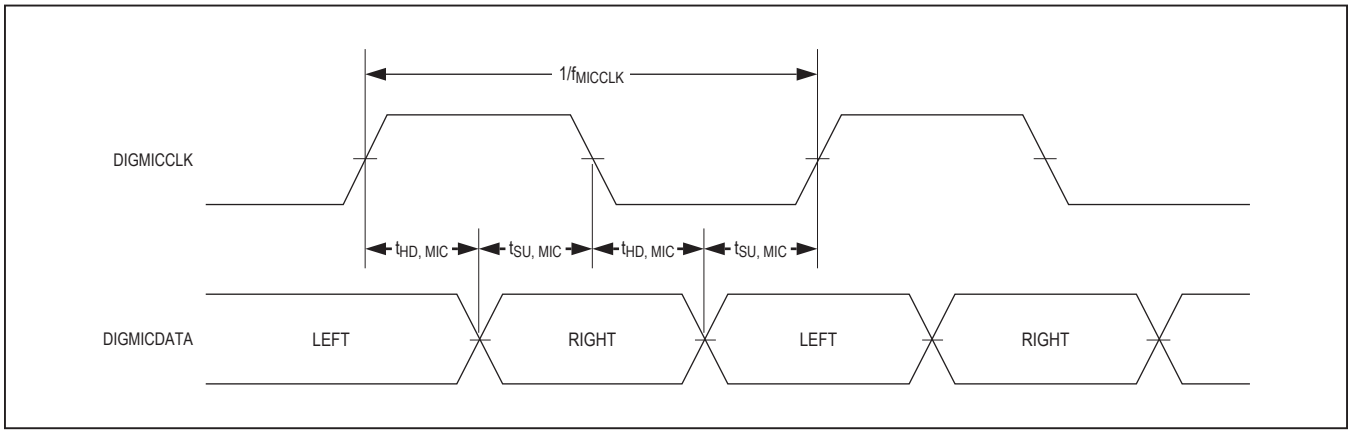


Figure 6. Digital Microphone Timing Diagram

Mode Configuration

The MAX9867 includes circuitry to minimize click-and-pop during volume changes, detect headsets, and configure the headphone amplifier mode. Both volume slewing and zero-crossing detection are included to ensure click-and-pop free volume transitions. Table 16 is the mode configuration register.

Headset Detection Overview

The MAX9867 features headset detection that can detect the insertion and removal of a jack as well as the load type. When a jack is detected, an interrupt on $\overline{IRQ}$ can be triggered to alert the microcontroller of the event. Figure 7 shows the typical configuration for jack detection.

Sleep-Mode Headset Detection

When the MAX9867 is in shutdown and the power supply is available, sleep-mode headset detection can be enabled to detect jack insertion. Sleep mode applies a 4µA pullup current to JACKSNS/AUX and LOUTP that forces the voltage on JACKSNS/AUX and LOUTP to AVDD when no load is applied. When a jack is inserted, either JACKSNS, LOUTP (assuming the headphone amplifier is not configured in single-ended mode), or both are loaded sufficiently to reduce the output voltage to nearly 0V and clear the JKSNS or LSNS bits, respectively. The change in the LSNS and JKSNS bits sets JDET and triggers an interrupt on $\overline{IRQ}$ if IJDET is set. The interrupt signals the microcontroller that a jack has been inserted, allowing the microcontroller to respond as desired.

Powered-On Headset Detection

When the MAX9867 is in normal operation and the microphone interface is enabled, jack insertion and removal can be detected through the JACKSNS/AUX pin. As shown in Figure 7, V_{MIC} is pulled up by MICBIAS. When a microphone is connected, V_{MIC} is assumed to be between 0V and 95% of $V_{MICBIAS}$. If the jack is removed, V_{MIC} increases to $V_{MICBIAS}$. This event causes JKMIC to be set, alerting the system that the headset has been removed. Alternatively, if the jack is inserted, V_{MIC} decreases to below 95% of $V_{MICBIAS}$ and JKMIC is cleared, alerting the system that a jack has been inserted. The JKMIC bit can be configured to create a hardware interrupt that alerts the microcontroller of jack removal and insertion events.

Headphone Modes

The headphone amplifier supports differential, singleended, and capacitorless output modes, as shown in Figure 8. In each mode, the amplifier can be configured for stereo or mono operation. The differential and capacitorless modes are inherently click and pop free. The single-ended mode optionally includes click-and-pop reduction to eliminate the click and pop that would normally be caused by the output coupling capacitor. When click-and-pop reduction is not required in the single-ended configuration, leave LOUTN and ROUTN unconnected.

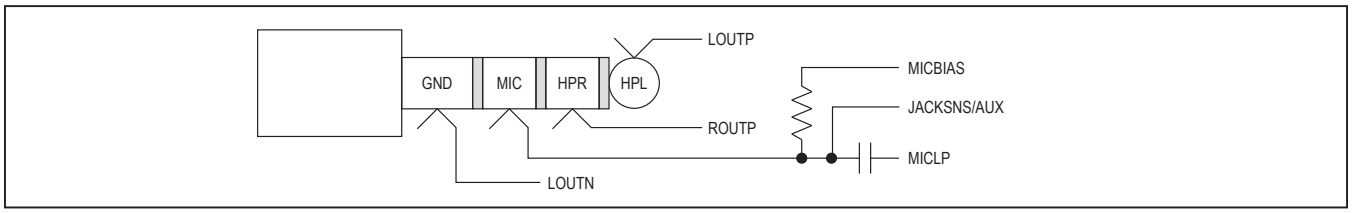


Figure 7. Typical Configuration for Headset Detection

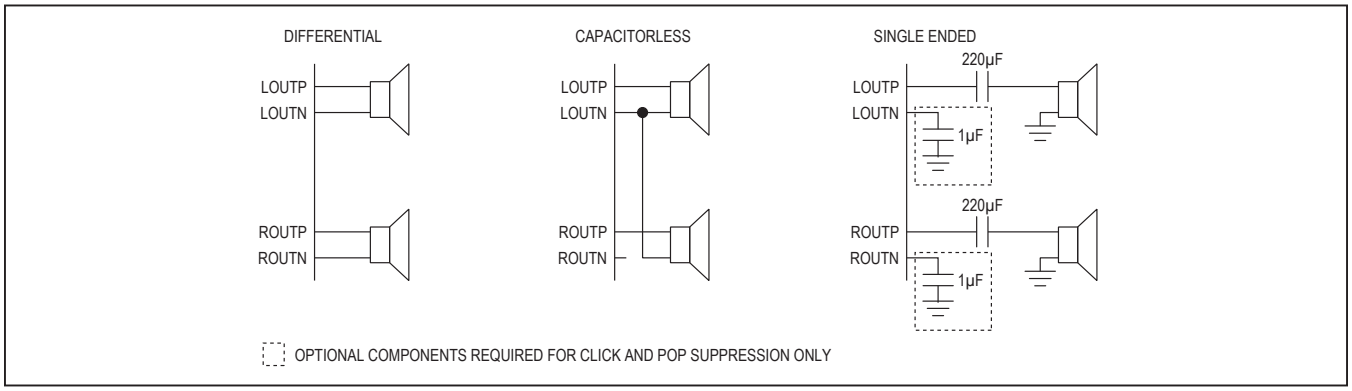


Figure 8. Headphone Amplifier Modes

Table 16. Mode Configuration Register

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REGISTER ADDRESS
Mode	DSLEW	$\overline{VSEN}$	$\overline{ZDEN}$	0	JDETEN	HPMODE			0x16

BITS	FUNCTION
DSLEW	**Digital Volume Slew Speed** 0 = Digital volume changes are slewed over 10ms. 1 = Digital volume changes are slewed over 80ms.
$\overline{VSEN}$	**Volume Change Smoothing** 0 = Volume changes slew through all intermediate values. 1 = Volume changes occur in one step.
$\overline{ZDEN}$	**Line Input Zero-Crossing Detection** 0 = Line input volume changes occur at zero crossings in the audio waveform or after 62ms if no zero crossing occurs. 1 = Line-input volume changes occur immediately.
JDETEN	**Jack Detection Enable** **$\overline{SHDN}$ = 0: Sleep Mode** Enables pullups on LOUTP and JACKSNS/AUX to detect jack insertion. LSNS and JKSNS are valid. LOUTP detection is only valid in differential and capacitorless output modes. **$\overline{SHDN}$ = 1: Normal Mode** Enables the comparator circuitry on JACKSNS/AUX to detect voltage changes. JKMIC is valid if the microphone circuitry is enabled. **Note:** AUXEN must be set to 0 for jack detection to function.
HPMODE	**Headphone Amplifier Mode**

HPMODE	Mode
000	Stereo differential (clickless)
001	Mono (left) differential (clickless)
010	Stereo capacitorless (clickless)
011	Mono (left) capacitorless (clickless)
100	Stereo single-ended (clickless)
101	Mono (left) single-ended (clickless)
110	Stereo single-ended (fast turn-on)
111	Mono (left) single-ended (fast turn-on)

Note: In mono operation, the right amplifier is disabled.

Power Management

The MAX9867 includes complete power management control to minimize power usage. The DAC and both ADC can be independently enabled so that only the required circuitry is active. Toggle the $\overline{SHDN}$ bit whenever a configuration change is made. Table 17 is the power-management register.

Table 17. Power-Management Register

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REGISTER ADDRESS
System Shutdown	$\overline{SHDN}$	LNLEN	LNREN	0	DALEN	DAREN	ADLEN	ADREN	0x17

BITS	FUNCTION
$\overline{SHDN}$	**Shutdown** Places the device in low-power shutdown mode.
LNLEN	**Left-Line Input Enable** Enables the left-line input preamp and automatically enables the left and right headphone amplifiers. If LNREN = 0, the left-line input signal is also routed to the right ADC input mixer and right headphone amplifier. **Note:** Control of the right headphone amplifier can be overridden by HPMODE.
LNREN	**Right-Line Input Enable** Enables the right-line input preamp and automatically enables the right headphone amplifier. **Note:** Control of the right headphone amplifier can be overridden by HPMODE.
DALEN	**Left DAC Enable** Enables the left DAC and automatically enables the left and right headphone amplifiers. If DAREN = 0, the left DAC signal is also routed to the right headphone amplifier. Note: Control of the right headphone amplifier can be overridden by HPMODE.
DAREN	**Right DAC Enable** Enabling the right DAC must be done in the same I^2C write operation that enables the left DAC. Right DAC operation requires DALEN = 1.
ADLEN	**Left ADC Enable**
ADREN	**Right ADC Enable** Enabling the right ADC must be done in the same I^2C write operation that enables the left ADC. The right ADC can be enabled while the left ADC is running if used for DC measurements. $\overline{SHDN}$ must be toggled to disable the right ADC in this case. Right ADC operation requires ADLEN = 1.

Revision Code

The MAX9867 includes a revision code to allow easy identification of the device revision. The revision code is 0x42. See Table 18 for the revision code register.

Table 18. Revision Code Register

REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	REGISTER ADDRESS
Revision	REV								0xFF

I²C Serial Interface

The MAX9867 features an I²C/SMBus-compatible, 2-wire serial interface consisting of a serial-data line (SDA) and a serial-clock line (SCL). SDA and SCL facilitate communication between the MAX9867 and the master at clock rates up to 400kHz. Figure 9 shows the 2-wire interface timing diagram. The master generates SCL and initiates data transfer on the bus. The master device writes data to the MAX9867 by transmitting the proper slave address followed by the register address and then the data word. Each transmit sequence is framed by a START (S) or REPEATED START (Sr) condition and a STOP (P) condition. Each word transmitted to the MAX9867 is 8 bits long and is followed by an acknowledge clock pulse. A master reading data from the MAX9867 transmits the proper slave address followed by a series of nine SCL pulses. The MAX9867 transmits data on SDA in sync with the master-generated SCL pulses. The master acknowledges receipt of each byte of data. Each read sequence is framed by a START or REPEATED START condition, a not acknowledge, and a STOP condition. SDA operates as both an input and an open-drain output. A pullup resistor, typically greater than 500Ω is required on SDA. SCL operates only as an input. A pullup resistor, typically greater than 500Ω, is required on SCL if there are multiple masters on the bus, or if the single master has an open-drain SCL output. Series resistors in line with SDA and SCL are optional. Series resistors protect the digital inputs of the MAX9867 from high-voltage spikes on the bus lines, and minimize crosstalk, and undershoot of the bus signals.

Bit Transfer

One data bit is transferred during each SCL cycle. The data on SDA must remain stable during the high period of the SCL pulse. Changes in SDA while SCL is high are control signals. See the *START and STOP Conditions* section.

START and STOP Conditions

SDA and SCL idle high when the bus is not in use. A master initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA while SCL is high (Figure 10). A START condition from the master signals the beginning of a transmission to the MAX9867. The master terminates transmission, and frees the bus, by issuing a STOP condition. The bus remains active if a REPEATED START condition is generated instead of a STOP condition.

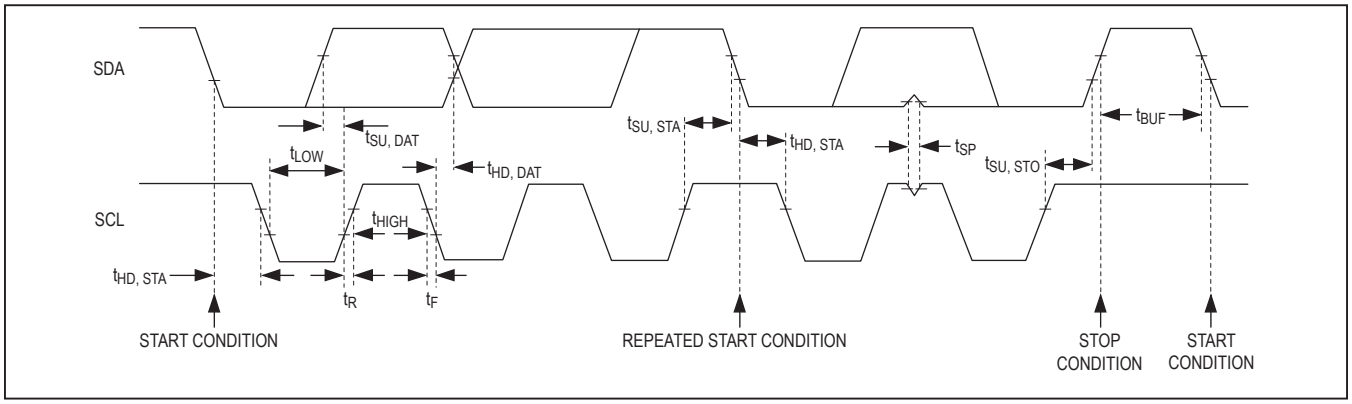


Figure 9. 2-Wire Interface Timing Diagram

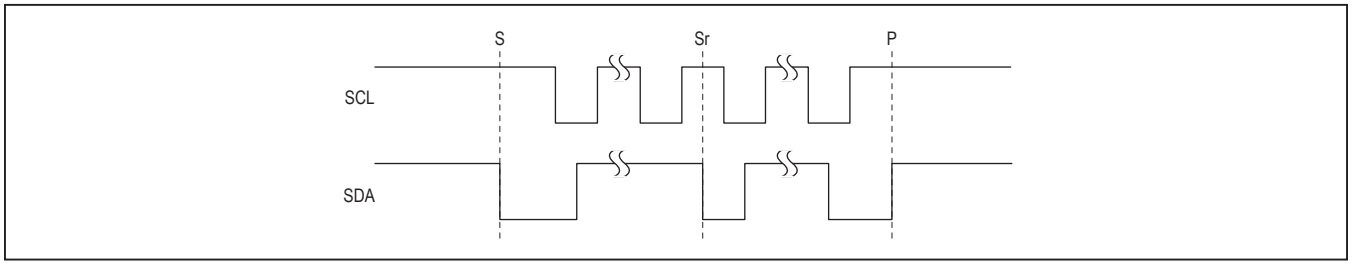


Figure 10. START, STOP, and REPEATED START Conditions

Early STOP Conditions

The MAX9867 recognizes a STOP condition at any point during data transmission except if the STOP condition occurs in the same high pulse as a START condition. For proper operation, do not send a STOP condition during the same SCL high pulse as the START condition.

Slave Address

The slave address is defined as the 7 most significant bits (MSBs) followed by the read/write bit. For the MAX9867, the 7 most significant bits are 0011000. Setting the read/write bit to 1 (slave address = 0x31) configures the MAX9867 for read mode. Setting the read/write bit to 0 (slave address = 0x30) configures the MAX9867 for write mode. The address is the first byte of information sent to the MAX9867 after the START condition.

Acknowledge

The acknowledge bit (ACK) is a clocked 9th bit that the MAX9867 uses to handshake receipt each byte of data when in write mode (see Figure 11). The MAX9867 pulls down SDA during the entire master-generated 9th clock pulse if the previous byte is successfully received. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master retries communication. The master pulls down SDA during the 9th clock cycle to acknowledge receipt of data when the MAX9867 is in read mode. An acknowledge is sent by the master after each read byte to allow data transfer to continue. A not acknowledge is sent when the master reads the final byte of data from the MAX9867, followed by a STOP condition.

Write Data Format

A write to the MAX9867 includes transmission of a START condition, the slave address with the R/$\overline{W}$ bit set to 0, 1 byte of data to configure the internal register address pointer, 1 or more bytes of data, and a STOP condition. Figure 12 illustrates the proper frame format for writing 1 byte of data to the MAX9867. Figure 13 illustrates the frame format for writing n bytes of data to the MAX9867.

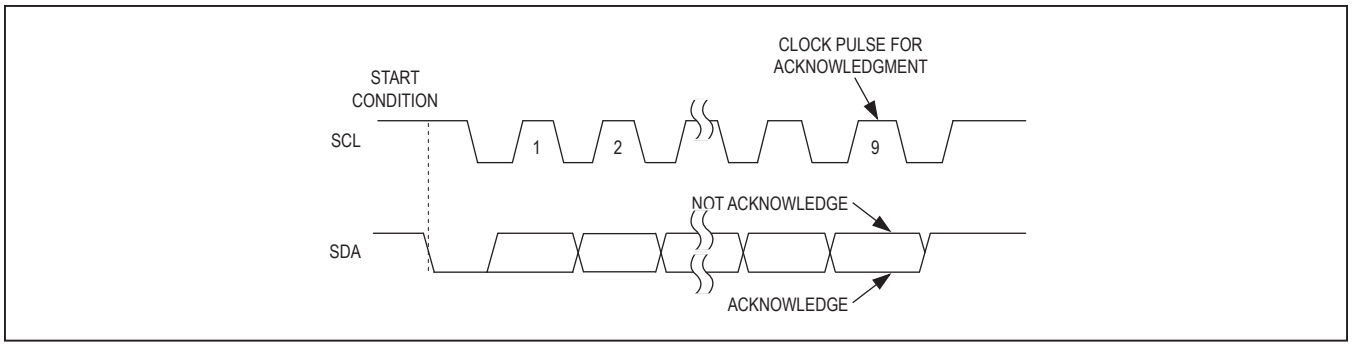


Figure 11. Acknowledge

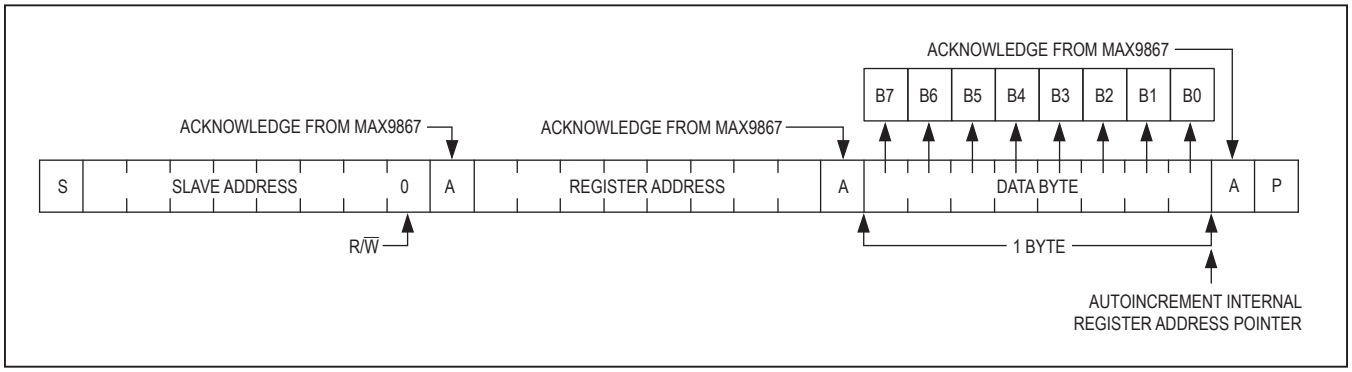


Figure 12. Writing 1 Byte of Data to the MAX9867

The slave address with the R/$\overline{W}$ bit set to 0 indicates that the master intends to write data to the MAX9867. The MAX9867 acknowledges receipt of the address byte during the master-generated 9th SCL pulse.

The second byte transmitted from the master configures the MAX9867's internal register address pointer. The pointer tells the MAX9867 where to write the next byte of data. An acknowledge pulse is sent by the MAX9867 upon receipt of the address pointer data.

The third byte sent to the MAX9867 contains the data that is written to the chosen register. An acknowledge pulse from the MAX9867 signals receipt of the data byte. The address pointer autoincrements to the next register address after each received data byte. This autoincrement feature allows a master to write to sequential registers within one continuous frame. Figure 13 illustrates how to write to multiple registers with one frame. The master signals the end of transmission by issuing a STOP condition. Register addresses greater than 0x17 are reserved. Do not write to these addresses.

Read Data Format

Send the slave address with the R/$\overline{W}$ bit set to 1 to initiate a read operation. The MAX9867 acknowledges receipt of its slave address by pulling SDA low during the 9th SCL clock pulse. A START command followed by a read command resets the address pointer to register 0x00.

The first byte transmitted from the MAX9867 is the content of register 0x00. Transmitted data is valid on the rising edge of SCL. The address pointer autoincrements after each read data byte. This autoincrement feature allows all registers to be read sequentially within one continuous frame. A STOP condition can be issued after any number of read data bytes. If a STOP condition is issued followed by another read operation, the first data byte to be read is from register 0x00.

The address pointer can be preset to a specific register before a read command is issued. The master presets the address pointer by first sending the MAX9867's slave address with the R/W bit set to 0 followed by the register address. A REPEATED START condition is then sent followed by the slave address with the R/$\overline{W}$ bit set to 1. The MAX9867 then transmits the contents of the specified register. The address pointer autoincrements after transmitting the first byte.

The master acknowledges receipt of each read byte during the acknowledge clock pulse. The master must acknowledge all correctly received bytes except the last byte. The final byte must be followed by a not acknowledge from the master and then a STOP condition. Figure 14 illustrates the frame format for reading 1 byte from the MAX9867. Figure 15 illustrates the frame format for reading multiple bytes from the MAX9867.

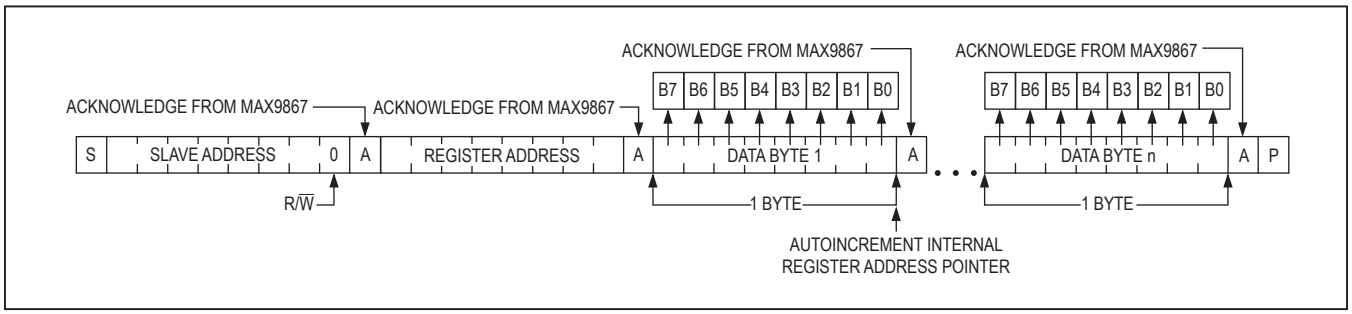


Figure 13. Writing n Bytes of Data to the MAX9867

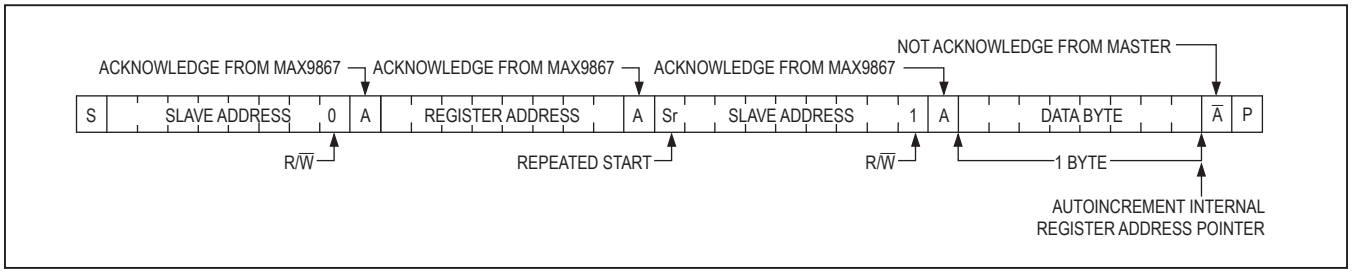


Figure 14. Reading 1 Byte of Data from the MAX9867

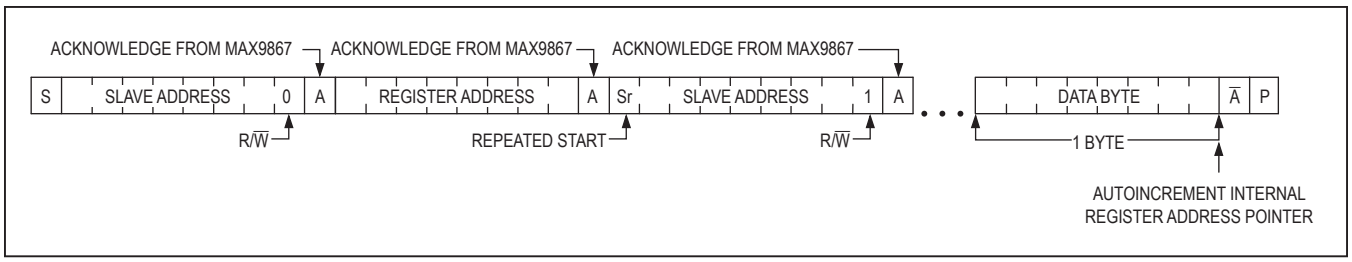


Figure 15. Reading n Bytes of Data from the MAX9867

Applications Information

Proper layout and grounding are essential for optimum performance. When designing a PCB for the MAX9867, partition the circuitry so that the analog sections of the MAX9867 are separated from the digital sections. This ensures that the analog audio traces are not routed near digital traces.

Use a large continuous ground plane on a dedicated layer of the PCB to minimize loop areas. Connect AGND and DGND directly to the ground plane using the shortest trace length possible. Proper grounding improves audio performance, minimizes crosstalk between channels, and prevents any digital noise from coupling into the analog audio signals.

Ground the bypass capacitors on MICBIAS, REG, PREG, and REF directly to the ground plane with minimum trace length. Also be sure to minimize the path length to AGND. Bypass AVDD directly to AGND.

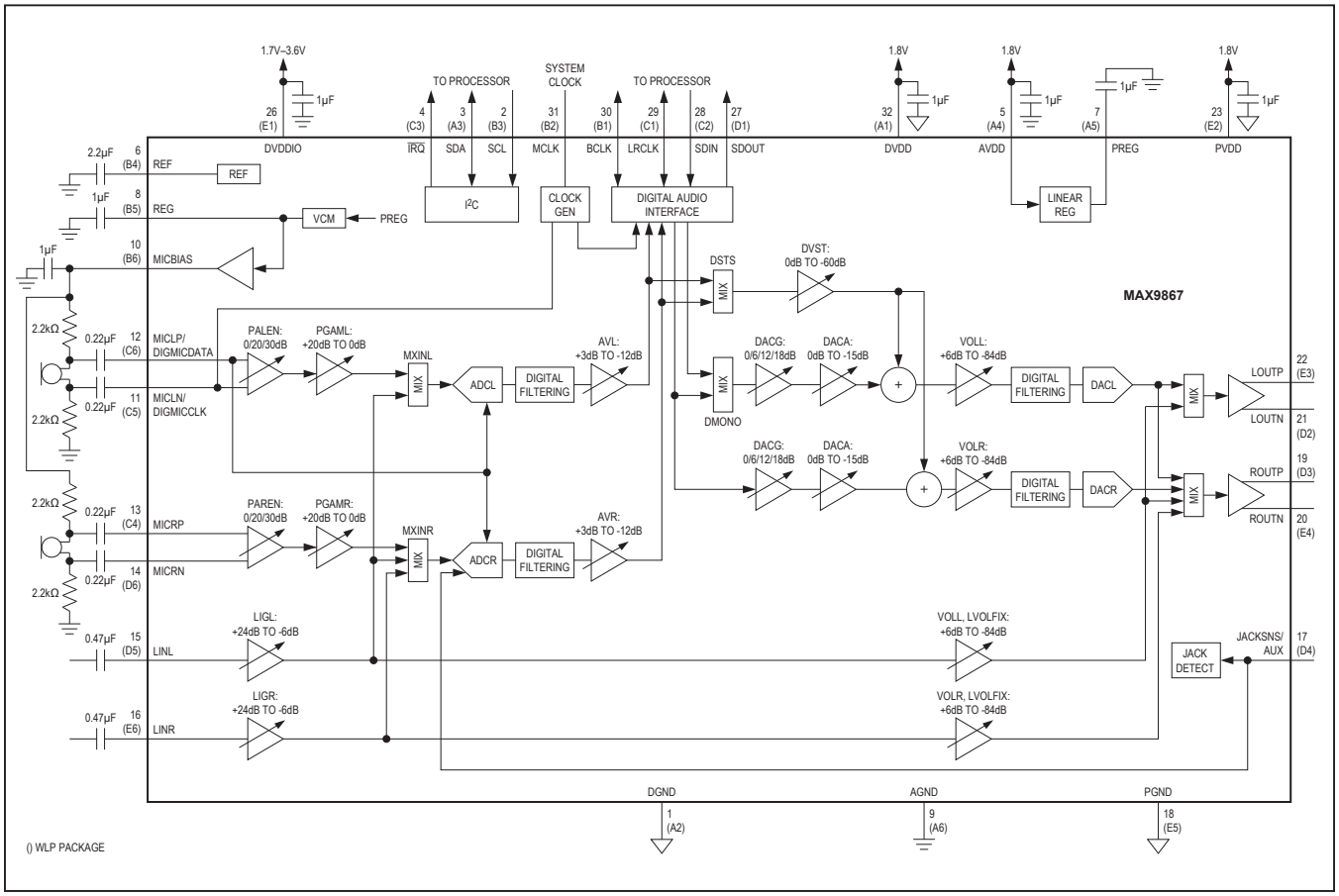
Connect all digital I/O termination to the ground plane with minimum path length to DGND. Bypass DVDD and DVDDIO directly to DGND.

Route microphone signals from the microphone to the MAX9867 as a differential pair, ensuring that the positive and negative signals follow the same path as closely as possible with equal trace length. When using single-ended microphones or other single-ended audio sources, ground the negative microphone input as near as possible to the audio source and then treat the positive and negative traces as differential pairs.

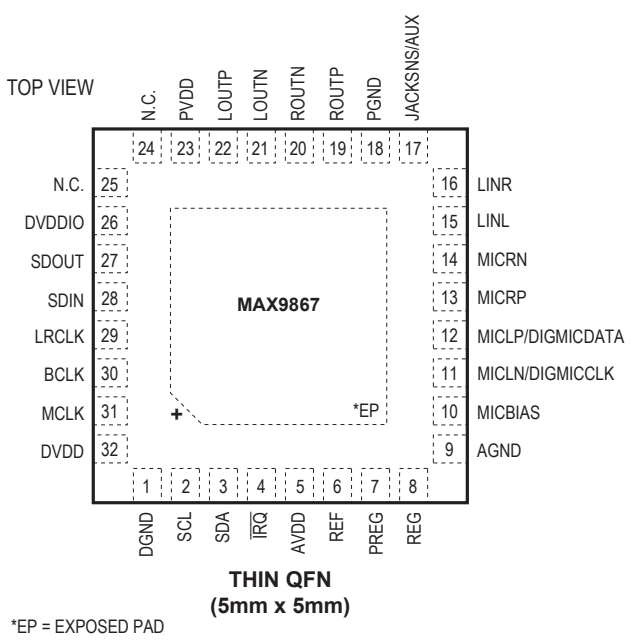
The MAX9867 TQFN package features an exposed thermal pad on its underside. Connect the exposed thermal pad to AGND.

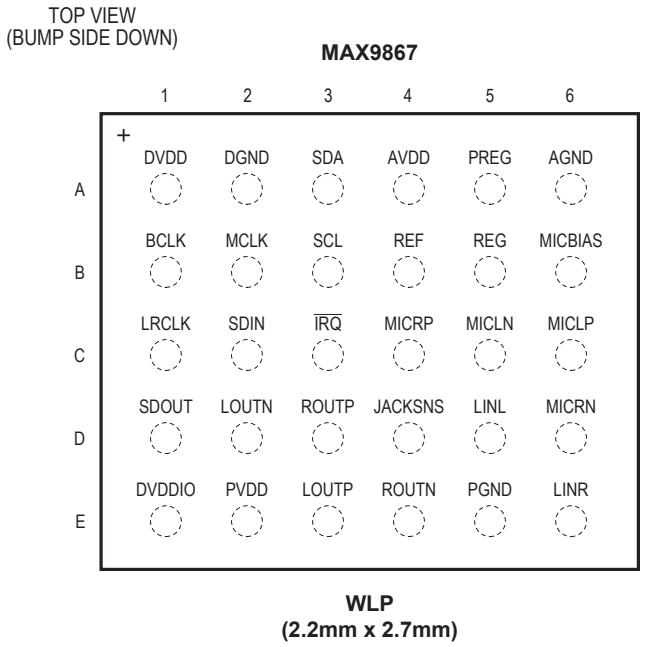
An evaluation kit (EV Kit) is available to provide an example layout for the MAX9867. The EV kit allows quick setup of the MAX9867 and includes easy-to-use software, allowing all internal registers to be controlled.

Functional Diagram/Typical Operating Circuit



Pin Configurations

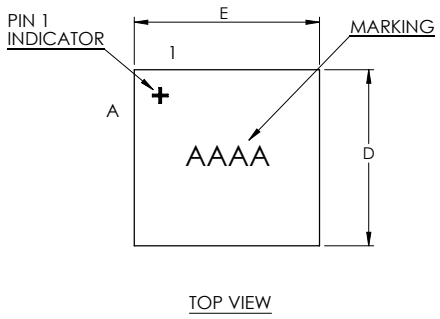




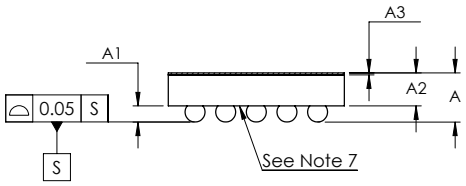
Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
30 WLP	W302A2+3	21-0211	—
32 TQFN-EP	T3255+4	21-0140	90-0012

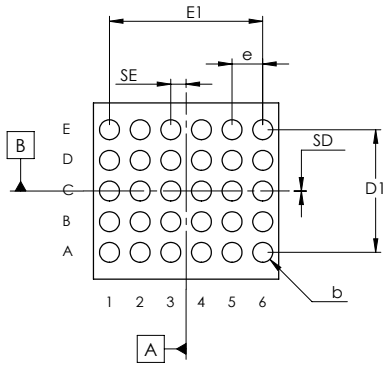


TOP VIEW



SIDE VIEW

COMMON DIMENSIONS		
A	0.64	±0.05
A1	0.21	±0.03
A2	0.43	REF
A3	0.025	BASIC
b	Ø0.26	±0.03
D1	1.60	BASIC
E1	2.00	BASIC
e	0.40	BASIC
SD	0.00	BASIC
SE	0.20	BASIC



BOTTOM VIEW

PKG. CODE	E		D		DEPOPULATED BUMPS
	MIN	MAX	MIN	MAX	
W302A2+1	2.61	2.73	2.31	2.44	NONE
W302A2+2	2.36	2.57	1.96	2.16	NONE
W302A2+3	2.57	2.77	2.16	2.36	NONE

NOTES:
1. Terminal pitch is defined by terminal center to center value.
2. Outer dimension is defined by center lines between scribe lines.
3. All dimensions in millimeter.
4. Marking shown is for package orientation reference only.
5. Tolerance is ± 0.02 unless specified otherwise.
6. All dimensions apply to PbFree (+) package codes only.
7. Front - side finish can be either Black or Clear.

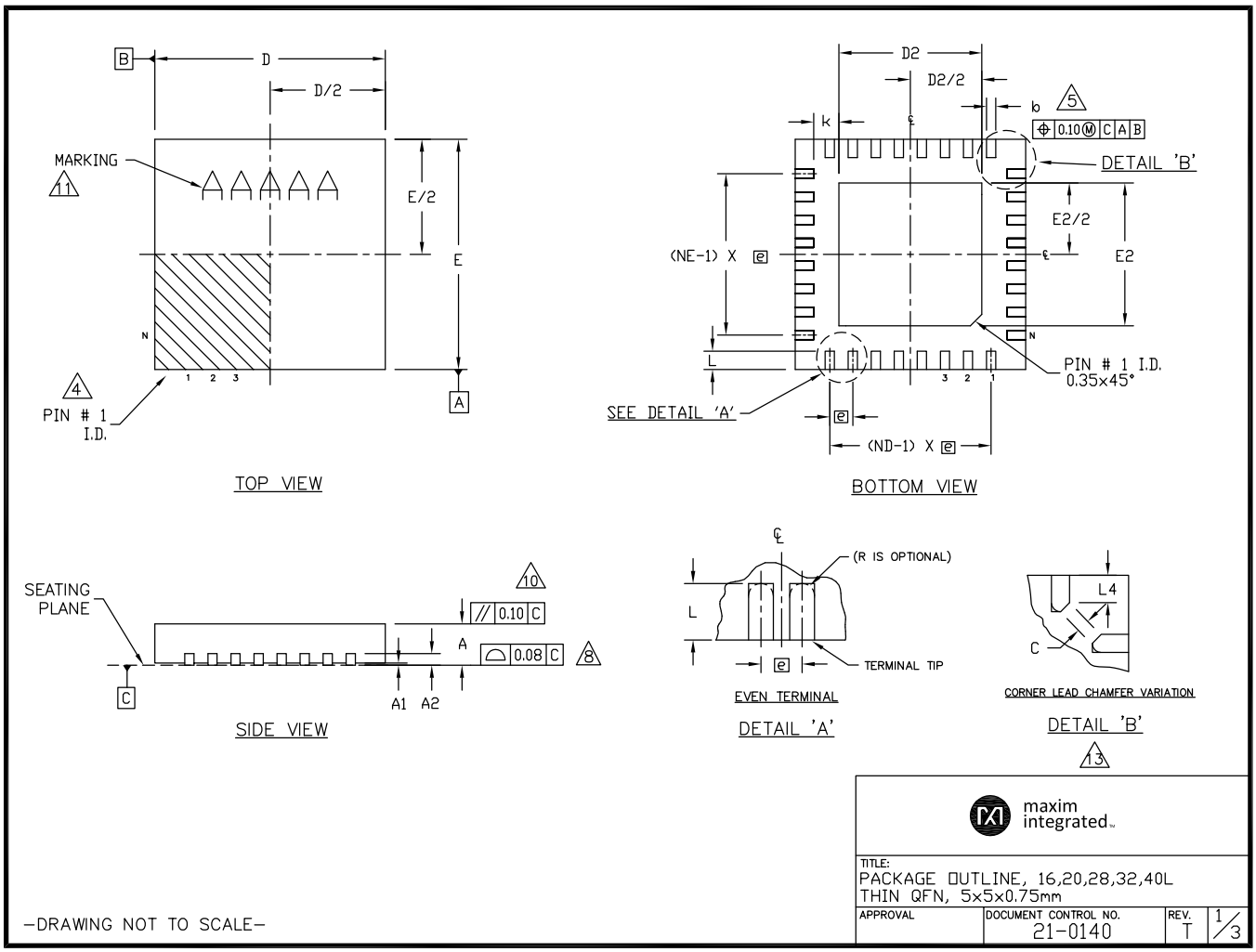
-DRAWING NOT TO SCALE-

TITLE: PACKAGE OUTLINE
30 BUMPS, WLP PKG. 0.4mm PITCH

APPROVAL | DOCUMENT CONTROL NO. 21-0211 | REV. E | 1/1

Package Information (continued)

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.



Package Information (continued)

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

COMMON DIMENSIONS

PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5			40L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–	0.25	–	–
L	0.30	0.40	0.50	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	16			20			28			32			40		
ND	4			5			7			8			10		
NE	4			5			7			8			10		
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2			-----		

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CORNER LEAD CHAMFER VARIATION

PKG. CODES	C	L4
T3255-3	0.120 X 45° REF	0.31 REF
T3255-4	0.120 X 45° REF	0.31 REF
T3255-5	0.120 X 45° REF	0.31 REF
T3255M-4	0.120 X 45° REF	0.31 REF
T3255M-5	0.120 X 45° REF	0.31 REF
T3255MK-1	0.120 X 45° REF	0.31 REF
T3255N-1	0.120 X 45° REF	0.31 REF
T4055-1	0.160 X 45° REF	0.28 REF
T4055-1C	0.160 X 45° REF	0.28 REF
T4055-2	0.160 X 45° REF	0.28 REF
T4055MN-1	0.160 X 45° REF	0.28 REF
T4055N-1	0.160 X 45° REF	0.28 REF

DIMENSION VARIATION

PKG. CODES	D2			E2			L
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	±0.10
T1655-2	3.00	3.10	3.20	3.00	3.10	3.20	--
T1655-3	3.00	3.10	3.20	3.00	3.10	3.20	--
T1655-4	2.19	2.29	2.39	2.19	2.29	2.39	--
T1655N-1	3.00	3.10	3.20	3.00	3.10	3.20	--
T2055-3	3.00	3.10	3.20	3.00	3.10	3.20	--
T2055M-3	3.00	3.10	3.20	3.00	3.10	3.20	--
T2055-4	3.00	3.10	3.20	3.00	3.10	3.20	--
T2055-5	3.15	3.25	3.35	3.15	3.25	3.35	0.40
T2055MN-5	3.15	3.25	3.35	3.15	3.25	3.35	0.40
T2855-3	3.15	3.25	3.35	3.15	3.25	3.35	--
T2855-4	2.60	2.70	2.80	2.60	2.70	2.80	--
T2855-5	2.60	2.70	2.80	2.60	2.70	2.80	--
T2855M-5	2.60	2.70	2.80	2.60	2.70	2.80	--
T2855-6	3.15	3.25	3.35	3.15	3.25	3.35	--
T2855-7	2.60	2.70	2.80	2.60	2.70	2.80	--
T2855-8	3.15	3.25	3.35	3.15	3.25	3.35	0.40
T2855MK-8	3.15	3.25	3.35	3.15	3.25	3.35	0.40
T2855N-1	3.15	3.25	3.35	3.15	3.25	3.35	--
T3255-3	3.00	3.10	3.20	3.00	3.10	3.20	--
T3255-4	3.00	3.10	3.20	3.00	3.10	3.20	--
T3255M-4	3.00	3.10	3.20	3.00	3.10	3.20	--
T3255-5	3.00	3.10	3.20	3.00	3.10	3.20	--
T3255M-5	3.00	3.10	3.20	3.00	3.10	3.20	--
T3255N-1	3.00	3.10	3.20	3.00	3.10	3.20	--
T4055-1	3.40	3.50	3.60	3.40	3.50	3.60	--
T4055-1C	3.40	3.50	3.60	3.40	3.50	3.60	--
T4055-2	3.40	3.50	3.60	3.40	3.50	3.60	--
T4055N-1	3.40	3.50	3.60	3.40	3.50	3.60	--
T4055MN-1	3.40	3.50	3.60	3.40	3.50	3.60	--

maxim integrated

TITLE:
PACKAGE OUTLINE, 16,20,28,32,40L
THIN QFN, 5x5x0.75mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0140	T	2/3

-DRAWING NOT TO SCALE-

Package Information (continued)

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NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-3, T2855-6, T4055-1 AND T4055-2.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. REFER TO DIMENSION VARIATION TABLE FOR LEAD LENGTH VARIATION
13. APPLICABLE ONLY FOR PACKAGES WITH TIGHT CORNER LEADS METAL TO METAL CLEARANCE.
14. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
15. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION "e", ±0.05.
16. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKG. CODES.

—DRAWING NOT TO SCALE—

maxim integrated™

TITLE: PACKAGE OUTLINE, 16,20,28,32,40L THIN QFN, 5x5x0.75mm			
APPROVAL	DOCUMENT CONTROL NO. 21-0140	REV. T	3/3

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	4/09	Initial release	—
1	5/10	Added lead temperature and soldering temperatures, updated V_{OS} specification	2, 8
2	6/10	Corrected error in TOC20	15
3	10/21	Updated 32 TQFN-EP Land Pattern in *Package Information* section	52
4	12/21	Updated 32 TQFN-EP Land Pattern in *Package Information* section	52