SN74LVCH8T245 8-BIT Dual-Supply Bus Transceiver With Configurable Level-Shifting, Voltage Translation, and 3-State Outputs

1 Features

- Control Inputs (DIR and $\overline{OE}$) V_{IH} and V_{IL} Levels are Referenced to V_{CCA}
- Bus Hold on Data Inputs Eliminates the Need for External Pullup and Pulldown Resistors
- V_{CC} Isolation
- Fully Configurable Dual-Rail Design
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22

2 Applications

- Personal Electronics
- Industrial
- Enterprise
- Telecommunications

3 Description

The SN74LVCH8T245 is an 8-bit noninverting bus transceiver that uses two separate configurable power-supply rails. The A port is designed to track V_{CCA}, which accepts any supply voltage from 1.65 V to 5.5 V. The B port is designed to track V_{CCB}, which also accepts any supply voltage from 1.65 V to 5.5 V. This allows for universal low-voltage bidirectional translation between any of the 1.8-V, 2.5-V, 3.3-V, and 5.5-V voltage nodes.

The SN74LVCH8T245 is designed for asynchronous communication between two data buses. The logic levels of the direction-control (DIR) input and the output-enable ($\overline{OE}$) input activate either the B-port outputs, the A-port outputs, or place both output ports into a high-impedance state. The device transmits data from the A bus to the B bus when the B-port outputs are activated, and from the B bus to the A bus when the A-port outputs are activated. The input circuitry on both A and B ports are always active.

The SN74LVCH8T245 is designed so that the control pins (DIR and $\overline{OE}$) are referenced to V_{CCA}.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device.

The V_{CC} isolation feature ensures that if either V_{CCA} or V_{CCB} is at GND, then the outputs are in the high-impedance state.

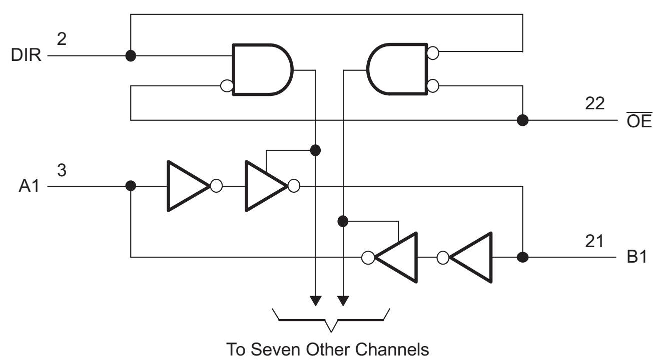
To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CCA} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LVCH8T245	SSOP (24)	8.65 mm × 3.90 mm
	TVSOP (24)	5.00 mm × 4.40 mm
	TSSOP (24)	7.80 mm × 4.40 mm
	VQFN (24)	5.50 mm × 3.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram (Positive Logic)



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4 Revision History

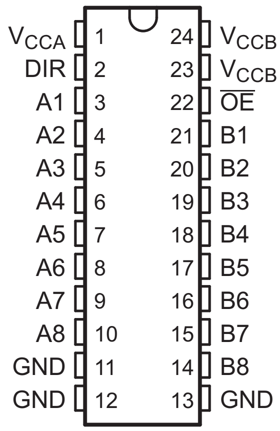
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (February 2007) to Revision B **Page**

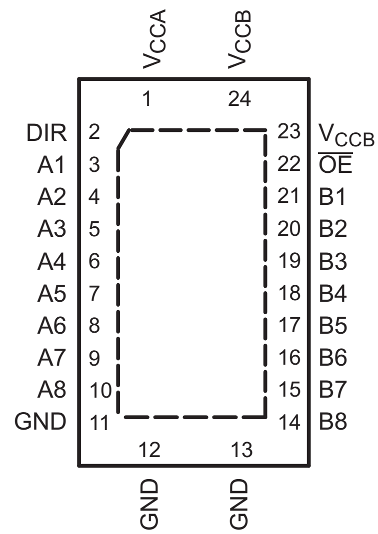
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

5 Pin Configuration and Functions

DB, DGV, or PW Packages
24-Pin SSOP, TVSOP, or TSSOP
Top View



RHL Package
24-Pin VQFN
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	SSOP, TVSOP, TSSOP	VQFN		
A1	3	3	I/O	Input/output A1. Referenced to V_{CCA}.
A2	4	4	I/O	Input/output A2. Referenced to V_{CCA}.
A3	5	5	I/O	Input/output A3. Referenced to V_{CCA}.
A4	6	6	I/O	Input/output A4. Referenced to V_{CCA}.
A5	7	7	I/O	Input/output A5. Referenced to V_{CCA}.
A6	8	8	I/O	Input/output A6. Referenced to V_{CCA}.
A7	9	9	I/O	Input/output A7. Referenced to V_{CCA}.
A8	10	10	I/O	Input/output A8. Referenced to V_{CCA}.
B1	21	21	I/O	Input/output B1. Referenced to V_{CCB}.
B2	20	20	I/O	Input/output B2. Referenced to V_{CCB}.
B3	19	19	I/O	Input/output B3. Referenced to V_{CCB}.
B4	18	18	I/O	Input/output B4. Referenced to V_{CCB}.
B5	17	17	I/O	Input/output B5. Referenced to V_{CCB}.
B6	16	16	I/O	Input/output B6. Referenced to V_{CCB}.
B7	15	15	I/O	Input/output B7. Referenced to V_{CCB}.
B8	14	14	I/O	Input/output B8. Referenced to V_{CCB}.
DIR	2	2	I	Direction-control signal. Referenced to V_{CCA}.
$\overline{OE}$	22	22	I	3-state output-mode enables. Pull $\overline{OE}$ high to place all outputs in 3-state mode. Referenced to V_{CCA}.
V_{CCA}	1	1	—	A-port supply voltage. 1.65 V ≤ V_{CCA} ≤ 5.5 V
V_{CCB}	23, 24	23, 24	—	B-port supply voltage. 1.65 V ≤ V_{CCA} ≤ 5.5 V
GND	11, 12, 13	11, 12, 13	—	Ground

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Supply voltage	V_{CCA} and V_{CCB}	–0.5	6.5	V
Input voltage[2]	I/O ports (A port)	–0.5	6.5	V
	I/O ports (B port)	–0.5	6.5	
	Control inputs	–0.5	6.5	
Voltage range applied to any output in the high-impedance or power-off state[2]	A port	–0.5	6.5	V
	B port	–0.5	6.5	
Voltage range applied to any output in the high or low state[2][3]	A port	–0.5	V_{CCA} + 0.5	V
	B port	–0.5	V_{CCB} + 0.5	
Input clamp current	V_I < 0		–50	mA
Output clamp current	V_O < 0		–50	mA
Continuous output current, I_O			±50	mA
Continuous through current	V_{CCA}, V_{CCB}, and GND		±100	mA
Junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The output positive-voltage rating may be exceeded up to 6.5 V maximum if the output current rating is observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101[2]	±1000	
		Machine model (MM)	±200	

(1) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)[1][2][3]

				MIN	MAX	UNIT
V_{CCA}	Supply voltage			1.65	5.5	V
V_{CCB}				1.65	5.5	
V_{IH}	High-level input voltage[1]	Data inputs[4]	V_{CCI} = 1.65 V to 4.5 V	V_{CCI} × 0.65		V
			V_{CCI} = 2.3 V to 2.7 V	1.7		
			V_{CCI} = 3 V to 3.6 V	2		
			V_{CCI} = 4.5 V to 5.5 V	V_{CCI} × 0.7		
V_{IL}	Low-level input voltage[1]	Data inputs[4]	V_{CCI} = 1.65 V to 4.5 V		V_{CCI} × 0.35	V
			V_{CCI} = 2.3 V to 2.7 V		0.7	
			V_{CCI} = 3 V to 3.6 V		0.8	
			V_{CCI} = 4.5 V to 5.5 V		V_{CCI} × 0.3	

(1) V_{CCI} is the V_{CC} associated with the data input port.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) All unused control inputs of the device must be held at V_{CCA} or GND to ensure proper device operation and minimize power consumption. See *Implications of Slow or Floating CMOS Inputs*, SCBA004.
(4) For V_{CCI} values not specified in the data sheet, V_{IH} min = V_{CCI} × 0.7 V, V_{IL} (max) = V_{CCI} × 0.3 V.

Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)(1)(2)(3)

				MIN	MAX	UNIT
V_{IH}	High-level input voltage	Control inputs (referenced to V_{CCA})(5)	V_{CCI} = 1.65 V to 4.5 V	V_{CCA} × 0.65		V
			V_{CCI} = 2.3 V to 2.7 V	1.7		
			V_{CCI} = 3 V to 3.6 V	2		
			V_{CCI} = 4.5 V to 5.5 V	V_{CCA} × 0.7		
V_{IL}	Low-level input voltage	Control inputs (referenced to V_{CCA})(5)	V_{CCI} = 1.65 V to 4.5 V		V_{CCA} × 0.35	V
			V_{CCI} = 2.3 V to 2.7 V		0.7	
			V_{CCI} = 3 V to 3.6 V		0.8	
			V_{CCI} = 4.5 V to 5.5 V		V_{CCA} × 0.3	
V_I	Input voltage	Control inputs(3)		0	5.5	V
$V_{I/O}$	Input/output voltage(2)	Active state		0	V_{CCO}	V
		3-State		0	5.5	
I_{OH}	High-level output current		V_{CCO} = 1.65 V to 4.5 V		–4	mA
			V_{CCO} = 2.3 V to 2.7 V		–8	
			V_{CCO} = 3 V to 3.6 V		–24	
			V_{CCO} = 4.5 V to 5.5 V		–32	
I_{OL}	Low-level output current		V_{CCO} = 1.65 V to 4.5 V		4	mA
			V_{CCO} = 2.3 V to 2.7 V		8	
			V_{CCO} = 3 V to 3.6 V		24	
			V_{CCO} = 4.5 V to 5.5 V		32	
Δt/Δv	Input transition rise or fall rate	Data inputs	V_{CCI} = 1.65 V to 4.5 V		20	ns/V
			V_{CCI} = 2.3 V to 2.7 V		20	
			V_{CCI} = 3 V to 3.6 V		10	
			V_{CCI} = 4.5 V to 5.5 V		5	
T_A	Operating free-air temperature			–40	85	°C

(5) For V_{CCA} values not specified in the data sheet, V_{IH} min = V_{CCA} × 0.7 V, V_{IL} (max) = V_{CCA} × 0.3 V.

6.4 Thermal Information

THERMAL METRIC(1)		SN74LVCH8T245				UNIT
		DB (SSOP)	DGV (TVSOP)	PW (TSSOP)	RHL (VQFN)	
		24 PINS	24 PINS	24 PINS	24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	88.5	91.1	90.6	37.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	48.7	23.7	27.6	38.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	44.1	44.5	45.3	15.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	12.8	0.6	1.3	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	43.6	44.1	44.8	15.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	—	4.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

All typical limits apply over T_A = 25°C, and all maximum and minimum limits apply over T_A = –40°C to 85°C (unless otherwise noted).(1)(2)

PARAMETER		TEST CONDITIONS				MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage(1)	I_{OH} = –100 µA, $V_I = V_{IH}$		$V_{CCA} = V_{CCB}$ = 1.65 V to 4.5 V		$V_{CCO} = 0.1$			V
		I_{OH} = –4 mA, $V_I = V_{IH}$		$V_{CCA} = V_{CCB}$ = 1.65 V		1.2			
		I_{OH} = –8 mA, $V_I = V_{IH}$		$V_{CCA} = V_{CCB}$ = 2.3 V		1.9			
		I_{OH} = –24 mA, $V_I = V_{IH}$		$V_{CCA} = V_{CCB}$ = 3 V		2.4			
		I_{OH} = –32 mA, $V_I = V_{IH}$		$V_{CCA} = V_{CCB}$ = 4.5 V		3.8			
V_{OL}	Low-level output voltage	I_{OL} = 100 µA, $V_I = V_{IL}$		$V_{CCA} = V_{CCB}$ = 1.65 V to 4.5 V				0.1	V
		I_{OL} = 4 mA, $V_I = V_{IL}$		$V_{CCA} = V_{CCB}$ = 1.65 V				0.45	
		I_{OL} = 8 mA, $V_I = V_{IL}$		$V_{CCA} = V_{CCB}$ = 2.3 V				0.3	
		I_{OL} = 24 mA, $V_I = V_{IL}$		$V_{CCA} = V_{CCB}$ = 3 V				0.55	
		I_{OL} = 32 mA, $V_I = V_{IL}$		$V_{CCA} = V_{CCB}$ = 4.5 V				0.55	
I_I	Control inputs	$V_I = V_{CCA}$ or GND		$V_{CCA} = V_{CCB}$ = 1.65 V to 4.5 V			±0.5	±2	µA
I_{BHL}(3)	Bus-hold low sustaining current	V_I = 0.58 V		$V_{CCA} = V_{CCB}$ = 1.65 V		15			µA
		V_I = 0.7 V		$V_{CCA} = V_{CCB}$ = 2.3 V		45			
		V_I = 0.8 V		$V_{CCA} = V_{CCB}$ = 3 V		75			
		V_I = 1.35 V		$V_{CCA} = V_{CCB}$ = 4.5 V		100			
I_{BHH}(4)	Bus-hold high sustaining current	V_I = 1.07 V		$V_{CCA} = V_{CCB}$ = 1.65 V		–15			µA
		V_I = 1.7 V		$V_{CCA} = V_{CCB}$ = 2.3 V		–45			
		V_I = 2 V		$V_{CCA} = V_{CCB}$ = 3 V		–75			
		V_I = 3.15 V		$V_{CCA} = V_{CCB}$ = 4.5 V		–100			
I_{BHLO}(5)	Bus-hold low overdrive current	V_I = 0 to V_{CC}		$V_{CCA} = V_{CCB}$ = 1.95 V		200			µA
				$V_{CCA} = V_{CCB}$ = 2.7 V		300			
				$V_{CCA} = V_{CCB}$ = 3.6 V		500			
				$V_{CCA} = V_{CCB}$ = 5.5 V		900			
I_{BHHO}(6)	Bus-hold high overdrive current	V_I = 0 to V_{CC}		$V_{CCA} = V_{CCB}$ = 1.95 V		–200			µA
				$V_{CCA} = V_{CCB}$ = 2.7 V		–300			
				$V_{CCA} = V_{CCB}$ = 3.6 V		–500			
				$V_{CCA} = V_{CCB}$ = 5.5 V		–900			
I_{off}	Input and output power-off leakage current	V_I or V_O = 0 to 5.5 V		V_{CCA} = 0 V, V_{CCB} = 0 to 5.5 V	A Port		±0.5	±2	µA
				V_{CCA} = 0 to 5.5 V, V_{CCB} = 0 V	B Port		±0.5	±2	
I_{OZ}	Off-state output current	$V_O = V_{CCO}$ or GND, $V_I = V_{CCI}$ or GND	$\overline{OE} = V_{IH}$	$V_{CCA} = V_{CCB}$ = 1.65 V to 4.5 V	A Port, B Port			±2	µA
			$\overline{OE}$ = X	V_{CCA} = 0 V, V_{CCB} = 5.5 V	B Port			±2	
				V_{CCA} = 5.5 V, V_{CCB} = 0 V	A Port			±2	
I_{CCA}	Supply current A port	$V_I = V_{CCI}$ or GND, I_O = 0		$V_{CCA} = V_{CCB}$ = 1.65 V to 4.5 V				20	µA
				V_{CCA} = 5 V, V_{CCB} = 0 V				20	
				V_{CCA} = 0 V, V_{CCB} = 5 V				–2	

(1) V_{CCO} is the V_{CC} associated with the output port.
(2) V_{CCI} is the V_{CC} associated with the input port.
(3) The bus-hold circuit can sink at least the minimum low sustaining current at the V_{IL} maximum. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{IL} maximum.
(4) The bus-hold circuit can source at least the minimum high sustaining current at V_{IH} min. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to V_{IH} min.
(5) An external driver must source at least I_{BHLO} to switch this node from low to high.
(6) An external driver must sink at least I_{BHHO} to switch this node from high to low.

Electrical Characteristics (continued)

All typical limits apply over T_A = 25°C, and all maximum and minimum limits apply over T_A = –40°C to 85°C (unless otherwise noted).(1)(2)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{CCB}	Supply current B port	$V_I = V_{CCI}$ or GND, I_O = 0	$V_{CCA} = V_{CCB}$ = 1.65 V to 4.5 V			20	µA
			V_{CCA} = 5 V, V_{CCB} = 0 V			–2	
			V_{CCA} = 0 V, V_{CCB} = 5 V			20	
	Combined supply current	$V_I = V_{CCI}$ or GND, I_O = 0	$V_{CCA} = V_{CCB}$ = 1.65 V to 4.5 V			30	µA
ΔI_{CCA}	Supply-current change DIR	DIR at V_{CCA} - 0.6 V, B port = open, A port at V_{CCA} or GND	$V_{CCA} = V_{CCB}$ = 3 to 5.5 V			50	µA
C_i	Input capacitance control inputs	$V_I = V_{CCA}$ or GND	$V_{CCA} = V_{CCB}$ = 3.3 V		4	5	pF
C_{io}	Input and output capacitance A or B port	$V_O = V_{CCA/B}$ or GND	$V_{CCA} = V_{CCB}$ = 3.3 V		8.5	10	pF

6.6 Switching Characteristics: V_{CCA} = 1.8 V ± 0.15 V

over recommended operating free-air temperature range, V_{CCA} = 1.8 V ± 0.15 V (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}, t_{PHL}	A	B	V_{CCB} = 1.8 V ± 0.15 V	1.7	21.9	ns
			V_{CCB} = 2.5 V ± 0.2 V	1.3	9.2	
			V_{CCB} = 3.3 V ± 0.3 V	1	7.4	
			V_{CCB} = 5 V ± 0.5 V	0.4	7.1	
t_{PLH}, t_{PHL}	B	A	V_{CCB} = 1.8 V ± 0.15 V	0.9	23.8	ns
			V_{CCB} = 2.5 V ± 0.2 V	0.8	23.6	
			V_{CCB} = 3.3 V ± 0.3 V	0.7	23.4	
			V_{CCB} = 5 V ± 0.5 V	0.7	23.4	
t_{PHZ}, t_{PLZ}	$\overline{OE}$	A	V_{CCB} = 1.8 V ± 0.15 V	1.5	29.6	ns
			V_{CCB} = 2.5 V ± 0.2 V	1.5	29.4	
			V_{CCB} = 3.3 V ± 0.3 V	1.5	29.3	
			V_{CCB} = 5 V ± 0.5 V	1.4	29.2	
t_{PHZ}, t_{PLZ}	$\overline{OE}$	B	V_{CCB} = 1.8 V ± 0.15 V	2.4	32.2	ns
			V_{CCB} = 2.5 V ± 0.2 V	1.9	13.1	
			V_{CCB} = 3.3 V ± 0.3 V	1.7	12	
			V_{CCB} = 5 V ± 0.5 V	1.3	10.3	
t_{PZH}, t_{PZL}	$\overline{OE}$	A	V_{CCB} = 1.8 V ± 0.15 V	0.4	24	ns
			V_{CCB} = 2.5 V ± 0.2 V	0.4	23.8	
			V_{CCB} = 3.3 V ± 0.3 V	0.4	23.7	
			V_{CCB} = 5 V ± 0.5 V	0.4	23.7	
t_{PZH}, t_{PZL}	$\overline{OE}$	B	V_{CCB} = 1.8 V ± 0.15 V	1.8	32	ns
			V_{CCB} = 2.5 V ± 0.2 V	1.5	16	
			V_{CCB} = 3.3 V ± 0.3 V	1.2	12.6	
			V_{CCB} = 5 V ± 0.5 V	0.9	10.8	

6.7 Switching Characteristics: V_{CCA} = 2.5 V ± 0.2 V

over recommended operating free-air temperature range, V_{CCA} = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}, t_{PHL}	A	B	V_{CCB} = 1.8 V ± 0.15 V	1.5	21.4	ns
			V_{CCB} = 2.5 V ± 0.2 V	1.2	9	
			V_{CCB} = 3.3 V ± 0.3 V	0.8	6.2	
			V_{CCB} = 5 V ± 0.5 V	0.6	4.8	
t_{PLH}, t_{PHL}	B	A	V_{CCB} = 1.8 V ± 0.15 V	1.2	9.3	ns
			V_{CCB} = 2.5 V ± 0.2 V	1	9.1	
			V_{CCB} = 3.3 V ± 0.3 V	1	8.9	
			V_{CCB} = 5 V ± 0.5 V	0.9	8.8	
t_{PHZ}, t_{PLZ}	$\overline{OE}$	A	V_{CCB} = 1.8 V ± 0.15 V	1.4	9	ns
			V_{CCB} = 2.5 V ± 0.2 V	1.4	9	
			V_{CCB} = 3.3 V ± 0.3 V	1.4	9	
			V_{CCB} = 5 V ± 0.5 V	1.4	9	
t_{PHZ}, t_{PLZ}	$\overline{OE}$	B	V_{CCB} = 1.8 V ± 0.15 V	2.3	29.6	ns
			V_{CCB} = 2.5 V ± 0.2 V	1.8	11	
			V_{CCB} = 3.3 V ± 0.3 V	1.7	9.3	
			V_{CCB} = 5 V ± 0.5 V	0.9	6.9	
t_{PZH}, t_{PZL}	$\overline{OE}$	A	V_{CCB} = 1.8 V ± 0.15 V	1	10.9	ns
			V_{CCB} = 2.5 V ± 0.2 V	1	10.9	
			V_{CCB} = 3.3 V ± 0.3 V	1	10.9	
			V_{CCB} = 5 V ± 0.5 V	1	10.9	
t_{PZH}, t_{PZL}	$\overline{OE}$	B	V_{CCB} = 1.8 V ± 0.15 V	1.7	28.2	ns
			V_{CCB} = 2.5 V ± 0.2 V	1.5	12.9	
			V_{CCB} = 3.3 V ± 0.3 V	1.2	9.4	
			V_{CCB} = 5 V ± 0.5 V	1	6.9	

6.8 Switching Characteristics: V_{CCA} = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, V_{CCA} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}, t_{PHL}	A	B	V_{CCB} = 1.8 V ± 0.15 V	1.5	21.2	ns
			V_{CCB} = 2.5 V ± 0.2 V	1.1	8.8	
			V_{CCB} = 3.3 V ± 0.3 V	0.8	6.2	
			V_{CCB} = 5 V ± 0.5 V	0.5	4.4	
t_{PLH}, t_{PHL}	B	A	V_{CCB} = 1.8 V ± 0.15 V	0.8	7.2	ns
			V_{CCB} = 2.5 V ± 0.2 V	0.8	6.2	
			V_{CCB} = 3.3 V ± 0.3 V	0.7	6.1	
			V_{CCB} = 5 V ± 0.5 V	0.6	6	
t_{PHZ}, t_{PLZ}	$\overline{OE}$	A	V_{CCB} = 1.8 V ± 0.15 V	1.6	8.2	ns
			V_{CCB} = 2.5 V ± 0.2 V	1.6	8.2	
			V_{CCB} = 3.3 V ± 0.3 V	1.6	8.2	
			V_{CCB} = 5 V ± 0.5 V	1.6	8.2	
t_{PHZ}, t_{PLZ}	$\overline{OE}$	B	V_{CCB} = 1.8 V ± 0.15 V	2.1	29	ns
			V_{CCB} = 2.5 V ± 0.2 V	1.7	10.3	
			V_{CCB} = 3.3 V ± 0.3 V	1.5	8.6	
			V_{CCB} = 5 V ± 0.5 V	0.8	6.3	
t_{PZH}, t_{PZL}	$\overline{OE}$	A	V_{CCB} = 1.8 V ± 0.15 V	0.8	8.1	ns
			V_{CCB} = 2.5 V ± 0.2 V	0.8	8.1	
			V_{CCB} = 3.3 V ± 0.3 V	0.8	8.1	
			V_{CCB} = 5 V ± 0.5 V	0.8	8.1	
t_{PZH}, t_{PZL}	$\overline{OE}$	B	V_{CCB} = 1.8 V ± 0.15 V	1.8	27.7	ns
			V_{CCB} = 2.5 V ± 0.2 V	1.4	12.4	
			V_{CCB} = 3.3 V ± 0.3 V	1.1	8.5	
			V_{CCB} = 5 V ± 0.5 V	0.9	6.4	

6.9 Switching Characteristics: V_{CCA} = 5 V ± 0.5 V

over recommended operating free-air temperature range, V_{CCA} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}, t_{PHL}	A	B	V_{CCB} = 1.8 V ± 0.15 V	1.5	21.4	ns
			V_{CCB} = 2.5 V ± 0.2 V	1	8.8	
			V_{CCB} = 3.3 V ± 0.3 V	0.7	6	
			V_{CCB} = 5 V ± 0.5 V	0.4	4.2	
t_{PLH}, t_{PHL}	B	A	V_{CCB} = 1.8 V ± 0.15 V	0.7	7	ns
			V_{CCB} = 2.5 V ± 0.2 V	0.4	4.8	
			V_{CCB} = 3.3 V ± 0.3 V	0.3	4.5	
			V_{CCB} = 5 V ± 0.5 V	0.3	4.3	
t_{PHZ}, t_{PLZ}	$\overline{OE}$	A	V_{CCB} = 1.8 V ± 0.15 V	0.3	5.4	ns
			V_{CCB} = 2.5 V ± 0.2 V	0.3	5.4	
			V_{CCB} = 3.3 V ± 0.3 V	0.3	5.4	
			V_{CCB} = 5 V ± 0.5 V	0.3	5.4	
t_{PHZ}, t_{PLZ}	$\overline{OE}$	B	V_{CCB} = 1.8 V ± 0.15 V	2	28.7	ns
			V_{CCB} = 2.5 V ± 0.2 V	1.6	9.7	
			V_{CCB} = 3.3 V ± 0.3 V	1.4	8	
			V_{CCB} = 5 V ± 0.5 V	0.7	5.7	
t_{PZH}, t_{PZL}	$\overline{OE}$	A	V_{CCB} = 1.8 V ± 0.15 V	0.7	6.4	ns
			V_{CCB} = 2.5 V ± 0.2 V	0.7	6.4	
			V_{CCB} = 3.3 V ± 0.3 V	0.7	6.4	
			V_{CCB} = 5 V ± 0.5 V	0.7	6.4	
t_{PZH}, t_{PZL}	$\overline{OE}$	B	V_{CCB} = 1.8 V ± 0.15 V	1.5	27.6	ns
			V_{CCB} = 2.5 V ± 0.2 V	1.3	11.4	
			V_{CCB} = 3.3 V ± 0.3 V	1	8.1	
			V_{CCB} = 5 V ± 0.5 V	0.9	6	

6.10 Operating Characteristics

T_A = 25°C

PARAMETER(1)		TEST CONDITIONS		TYP	UNIT
C_{pdA} (2)	A-port input, B-port output	C_L = 0, f = 10 MHz, t_r = t_f = 1 ns	V_{CCA} = V_{CCB} = 1.8 V	2	pF
			V_{CCA} = V_{CCB} = 2.5 V	2	
			V_{CCA} = V_{CCB} = 3.3 V	2	
			V_{CCA} = V_{CCB} = 5 V	3	
	B-port input, A-port output	C_L = 0, f = 10 MHz, t_r = t_f = 1 ns	V_{CCA} = V_{CCB} = 1.8 V	12	
			V_{CCA} = V_{CCB} = 2.5 V	13	
			V_{CCA} = V_{CCB} = 3.3 V	13	
			V_{CCA} = V_{CCB} = 5 V	16	
C_{pdB} (2)	A-port input, B-port output	C_L = 0, f = 10 MHz, t_r = t_f = 1 ns	V_{CCA} = V_{CCB} = 1.8 V	13	pF
			V_{CCA} = V_{CCB} = 2.5 V	13	
			V_{CCA} = V_{CCB} = 3.3 V	14	
			V_{CCA} = V_{CCB} = 5 V	16	
	B-port input, A-port output	C_L = 0, f = 10 MHz, t_r = t_f = 1 ns	V_{CCA} = V_{CCB} = 1.8 V	2	
			V_{CCA} = V_{CCB} = 2.5 V	2	
			V_{CCA} = V_{CCB} = 3.3 V	2	
			V_{CCA} = V_{CCB} = 5 V	3	

(1) See *CMOS Power Consumption and Cpd Calculation*, SCAA035.
(2) Power dissipation capacitance per transceiver.

6.11 Typical Characteristics

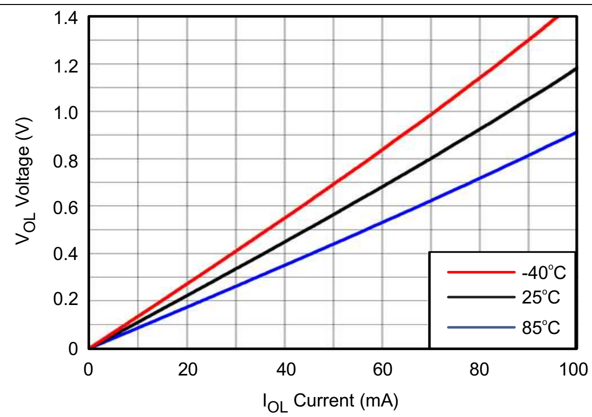


Figure 1. Voltage vs Current

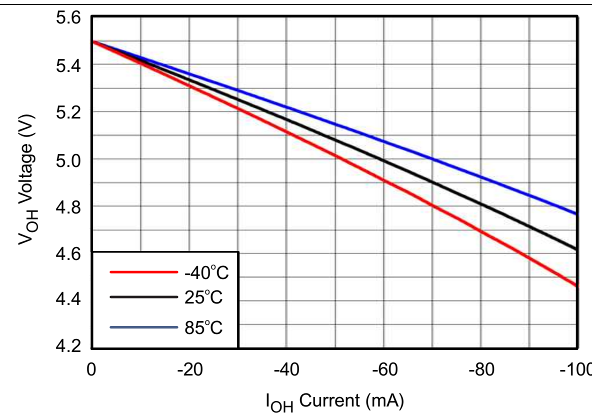
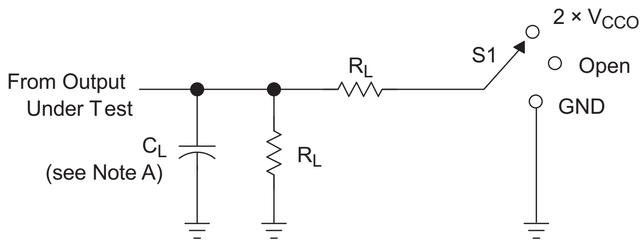


Figure 2. Voltage vs Current

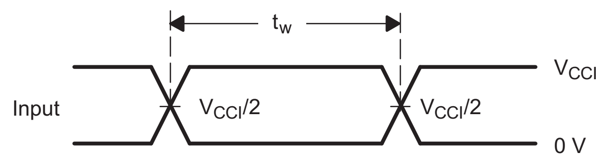
7 Parameter Measurement Information



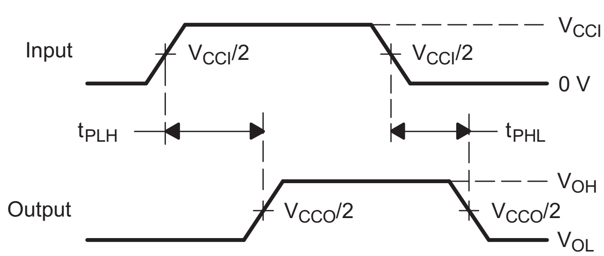
LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 × V_{CCO}
t_{PHZ}/t_{PZH}	GND

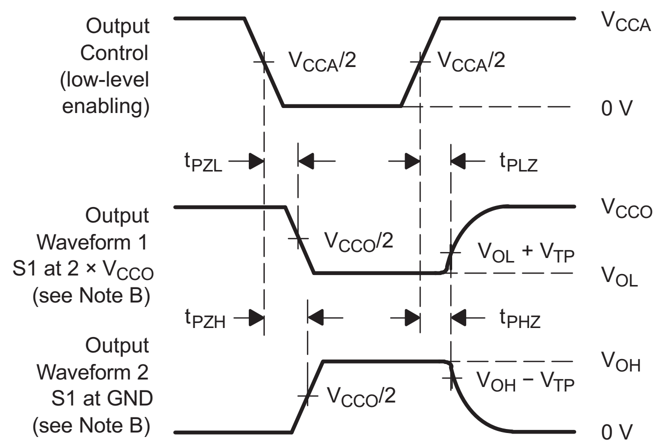
V_{CCO}	C_L	R_L	V_{TP}
1.8 V ± 0.15 V	15 pF	2 kW	0.15 V
2.5 V ± 0.2 V	15 pF	2 kW	0.15 V
3.3 V ± 0.3 V	15 pF	2 kW	0.3 V
5 V ± 0.5 V	15 pF	2 kW	0.3 V



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR   10 MHz, Z_O = 50 W, dv/dt ≥ 1 V/ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- F. t_{PZL} and t_{PZH} are the same as t_{en}.
- G. t_{PLH} and t_{PHL} are the same as t_{pd}.
- H. V_{CCI} is the V_{CC} associated with the input port.
- I. V_{CCO} is the V_{CC} associated with the output port.
- J. All parameters and waveforms are not applicable to all devices.

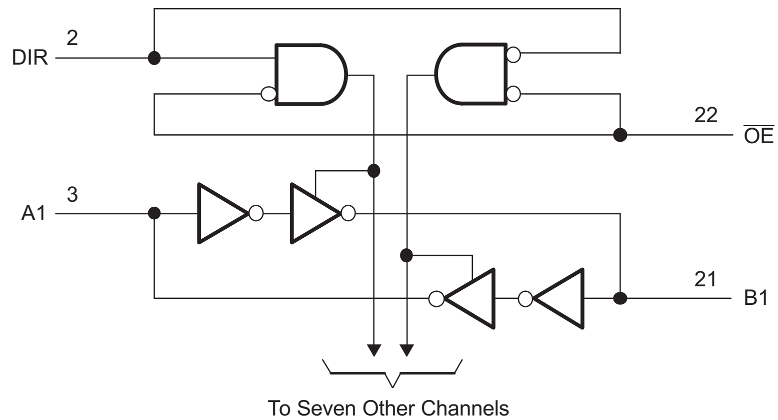
Figure 3. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The SN74LVCH8T245 is an 8-bit, dual supply noninverting voltage level translator. Pins A1 through A4, and the control pins (DIR and $\overline{OE}$) are referenced to V_{CCA}, while pins B1 through B4 are referenced to V_{CCB}. Both the A port and B port can accept I/O voltages ranging from 1.65 V to 5.5 V. The high on DIR allows data transmission from Port A to Port B, and a low on DIR allows data transmission from Port B to Port A. See *AVC Logic Family Technology and Applications* (SCEA006).

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Fully Configurable Dual-Rail Design

Both V_{CCA} and V_{CCB} can be supplied at any voltage from 1.65 V to 5.5 V, making the device suitable for translating between any of the voltage nodes: 1.8 V, 2.5 V, 3.3 V and 5 V.

8.3.2 Partial-Power-Down Mode Operation

I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. This can occur in applications where subsections of a system are powered down (partial power down) to reduce power consumption.

8.3.3 Active Bus Hold Circuitry

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state, which helps with board space savings and reduced component costs. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

8.3.4 Supports High-Speed Translation

The device can support high data rate applications, which can be calculated from the maximum propagation delay. This is also dependant on the output load. For example, for a 3.3-V to 5-V conversion, the maximum frequency is 200 MHz.

8.3.5 V_{CC} Isolation

The V_{CC} isolation feature ensures that if either V_{CCA} or V_{CCB} are at GND (or < 0.4 V), both ports will be in a high-impedance state (I_{OZ} shown in *Electrical Characteristics*). This prevents false logic levels from being presented to either bus.

8.4 Device Functional Modes

Table 1 lists the functional modes of the SN74LVCH8T245.

Table 1. Function Table (Each 8-Bit Section)

CONTROL INPUTS(1)		OUTPUT CIRCUITS		OPERATION
$\overline{OE}$	DIR	A PORT	B PORT	
L	L	Enabled	Hi-Z	B data to A bus
L	H	Hi-Z	Enabled	A data to B bus
H	X	Hi-Z	Hi-Z	Isolation

(1) Input circuits of the data I/Os are always active.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74LVCH8T245 device can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The maximum output current can be up to 32 mA when device is powered by 5 V.

9.2 Typical Application

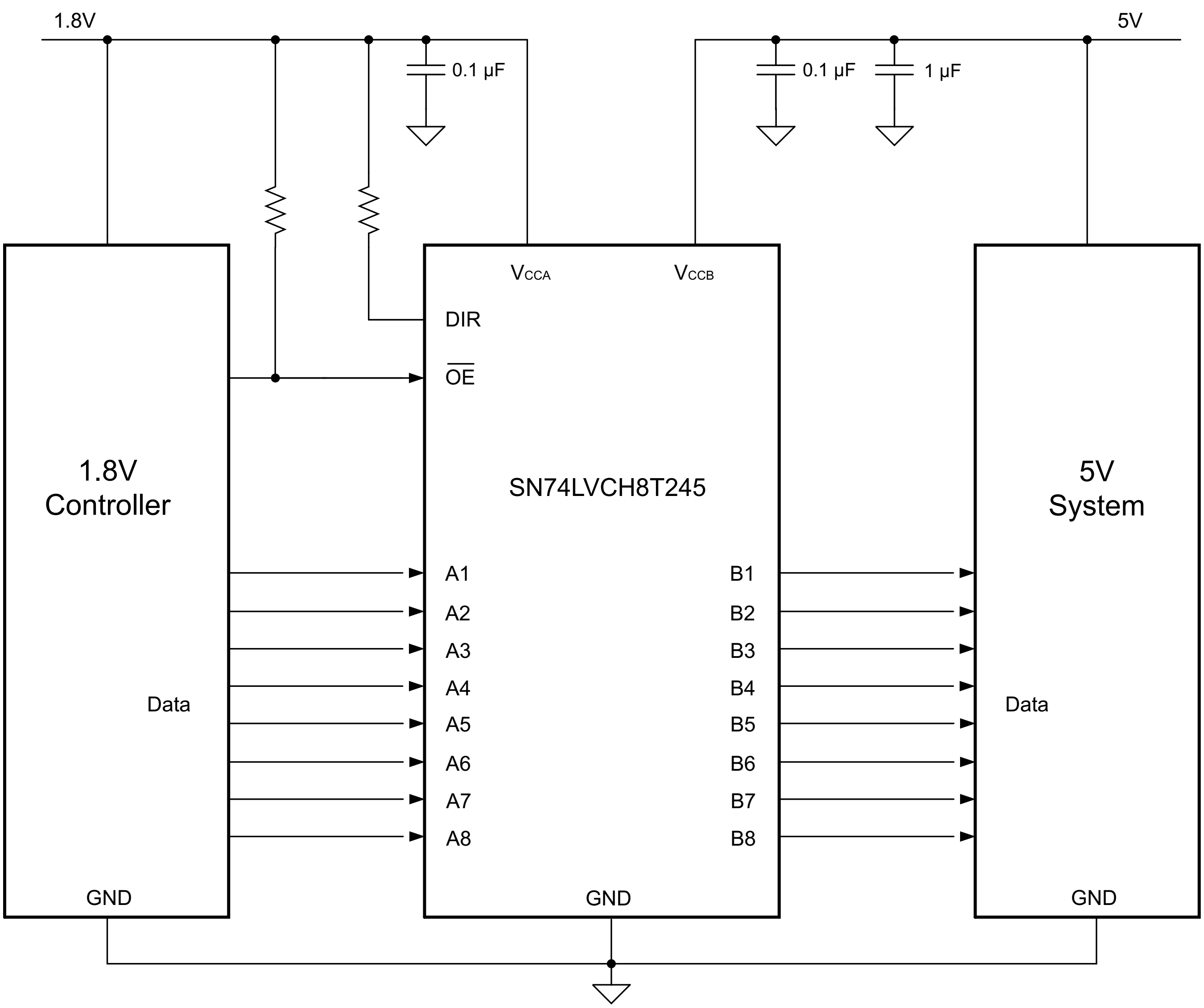


Figure 4. Typical Application Circuit

Typical Application (continued)

9.2.1 Design Requirements

For this design example, use the parameters listed in Table 2.

Table 2. Design Parameters

PARAMETERS	VALUES
Input voltage	1.65 V to 5.5 V
Output voltage	1.65 V to 5.5 V

9.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  – Use the supply voltage of the device that is driving the SN74LVCH8T245 to determine the input voltage range. For a valid logic high, the value must exceed the V_{IH} of the input port. For a valid logic low, the value must be less than the V_{IL} of the input port.
- Output voltage range
  – Use the supply voltage of the device that the SN74LVCH8T245 is driving to determine the output voltage range.

9.2.2.1 Enable Times

Calculate the enable times for the SN74LVCH8T245 using Equation 1, Equation 2, Equation 3, and Equation 4:

$$t_{PZH} \text{ (DIR to A)} = t_{PLZ} \text{ (DIR to B)} + t_{PLH} \text{ (B to A)} \quad (1)$$

$$t_{PZL} \text{ (DIR to A)} = t_{PHZ} \text{ (DIR to B)} + t_{PHL} \text{ (B to A)} \quad (2)$$

$$t_{PZH} \text{ (DIR to B)} = t_{PLZ} \text{ (DIR to A)} + t_{PLH} \text{ (A to B)} \quad (3)$$

$$t_{PZL} \text{ (DIR to B)} = t_{PHZ} \text{ (DIR to A)} + t_{PHL} \text{ (A to B)} \quad (4)$$

In a bidirectional application, these enable times provide the maximum delay from the time the DIR bit is switched until an output is expected. For example, if the device initially is transmitting from A to B, then the DIR bit is switched; the B port of the device must be disabled before presenting it with an input. After the B port has been disabled, an input signal applied to it appears on the corresponding A port after the specified propagation delay.

9.2.3 Application Curve

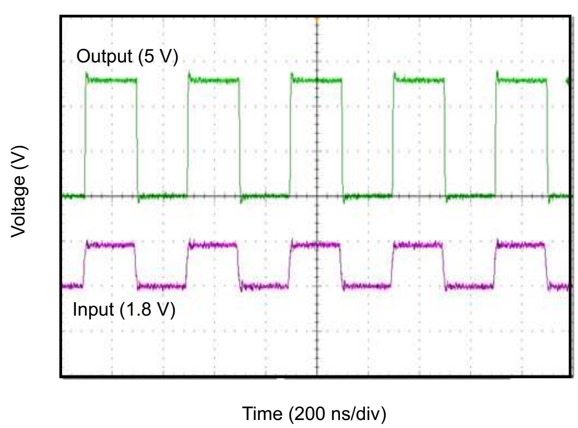


Figure 5. Translation Up (1.8 V to 5 V) at 2.5 MHz

10 Power Supply Recommendations

The output-enable ($\overline{OE}$) input circuit is designed so that it is supplied by V_{CCA} and when the $\overline{OE}$ input is high, all outputs are placed in the high-impedance state. To ensure the high-impedance state of the outputs during power up or power down, the $\overline{OE}$ input pin must be tied to V_{CCA} through a pullup resistor and must not be enabled until V_{CCA} and V_{CCB} are fully ramped and stable. The minimum value of the pullup resistor to V_{CCA} is determined by the current-sinking capability of the driver.

V_{CCA} or V_{CCB} can be powered up first. If the SN74LVCH8T245 is powered up in a permanently enabled state (for example $\overline{OE}$ is always kept low), pullup resistors are recommended at the input. This ensures proper, glitch-free, power-up. See *Designing with SN4LVCXT245 and SN74LVCHXT245 Family of Direction Controlled Voltage Translators/Level-Shifters* (SLVA746). In addition, the $\overline{OE}$ pin may be shorted to GND if the application does not require use of the high-impedance state at any time.

11 Layout

11.1 Layout Guidelines

To ensure reliability of the device, TI recommends the following common printed-circuit board layout guidelines.

- Bypass capacitors should be used on power supplies.
- Short trace lengths should be used to avoid excessive loading.
- Placing pads on the signal paths for loading capacitors or pullup resistors helps adjust rise and fall times of signals depending on the system requirements.

11.2 Layout Example

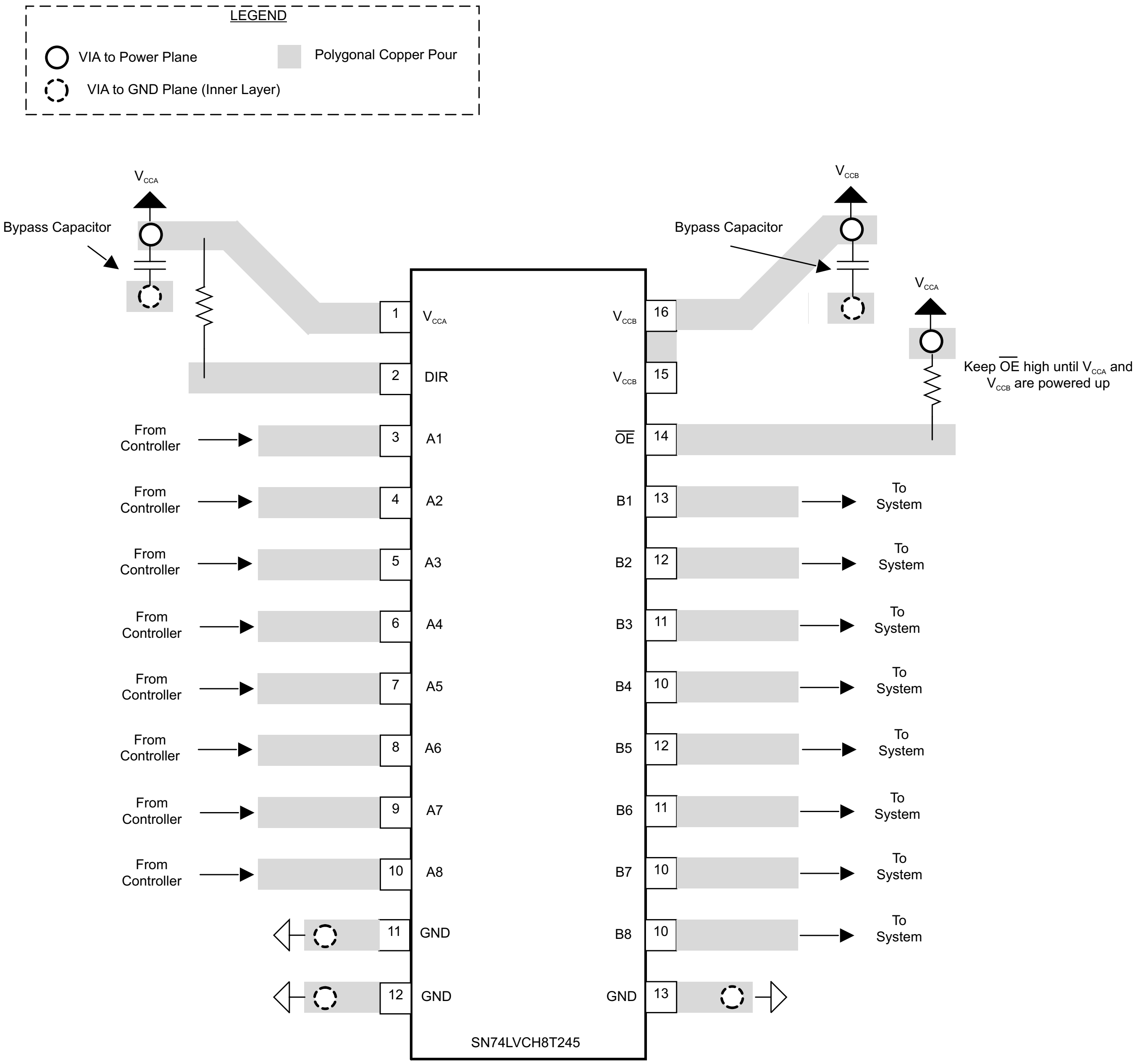


Figure 6. SN74LVCH8T245 Layout

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- *Designing with SN74LVCXT245 and SN74LVCHXT245 Family of Direction Controlled Voltage Translators/Level-Shifters*, SLVA746
- *Bus-Hold Circuit*, SCLA015
- *AVC Logic Family Technology and Applications*, SCEA006
- *CMOS Power Consumption and Cpd Calculation*, SCAA035

12.2 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVCH8T245DBR	ACTIVE	SSOP	DB	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NJ245	Samples
SN74LVCH8T245DGVR	ACTIVE	TVSOP	DGV	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NJ245	Samples
SN74LVCH8T245PW	ACTIVE	TSSOP	PW	24	60	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NJ245	Samples
SN74LVCH8T245PWE4	ACTIVE	TSSOP	PW	24	60	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NJ245	Samples
SN74LVCH8T245PWR	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	NJ245	Samples
SN74LVCH8T245RHLR	ACTIVE	VQFN	RHL	24	1000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	NJ245	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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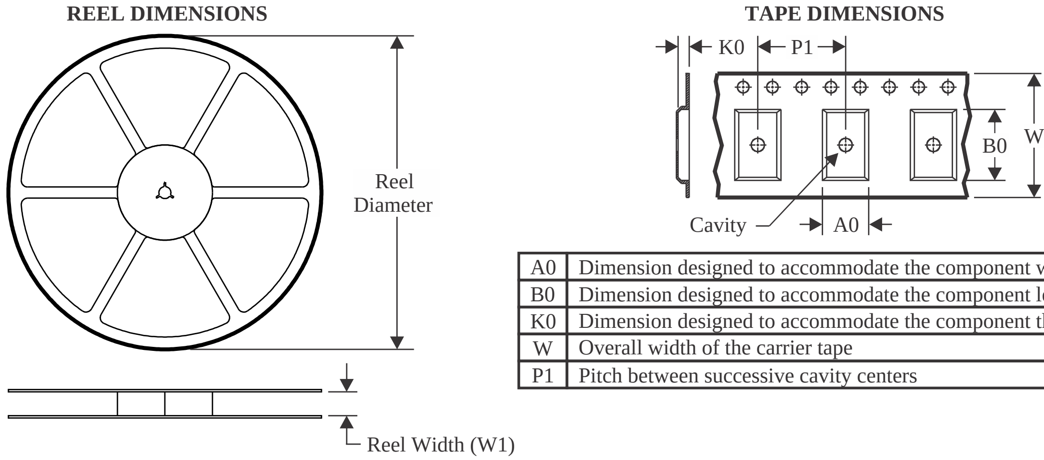
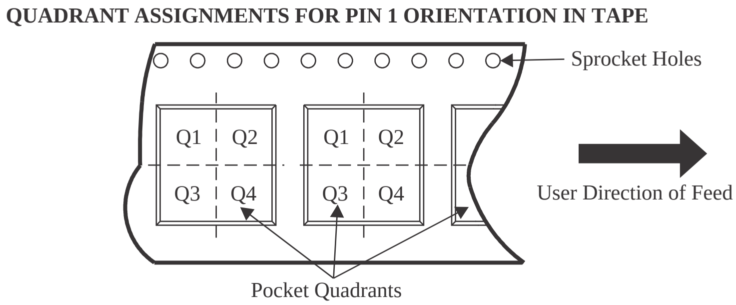
TAPE AND REEL INFORMATION



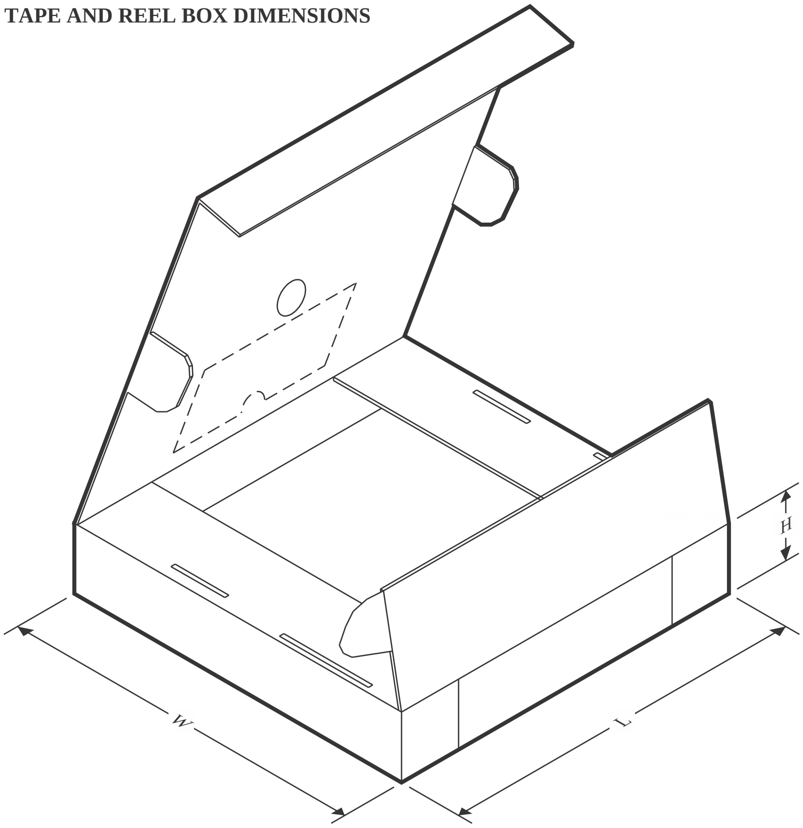
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVCH8T245DBR	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1
SN74LVCH8T245DGVR	TVSOP	DGV	24	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVCH8T245PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
SN74LVCH8T245RHLR	VQFN	RHL	24	1000	180.0	12.4	3.8	5.8	1.2	8.0	12.0	Q1

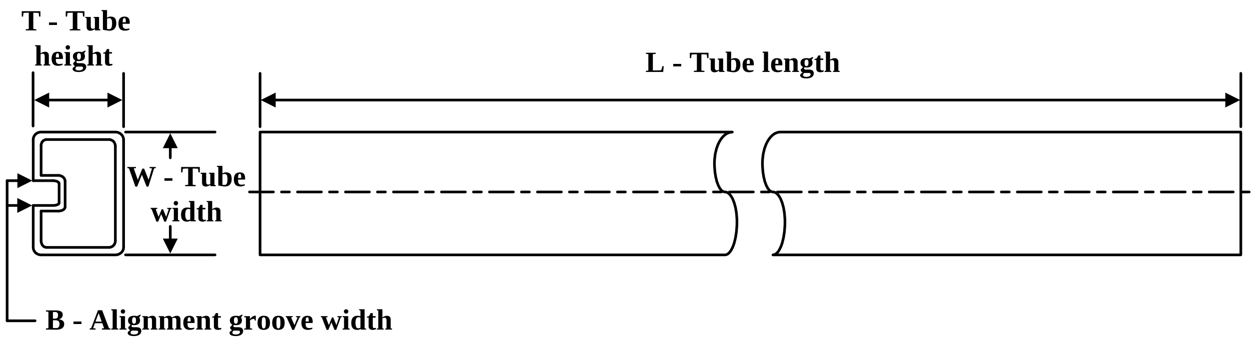
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

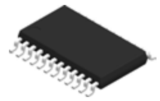
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVCH8T245DBR	SSOP	DB	24	2000	356.0	356.0	35.0
SN74LVCH8T245DGVR	TVSOP	DGV	24	2000	356.0	356.0	35.0
SN74LVCH8T245PWR	TSSOP	PW	24	2000	356.0	356.0	35.0
SN74LVCH8T245RHLR	VQFN	RHL	24	1000	210.0	185.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74LVCH8T245PW	PW	TSSOP	24	60	530	10.2	3600	3.5
SN74LVCH8T245PWE4	PW	TSSOP	24	60	530	10.2	3600	3.5

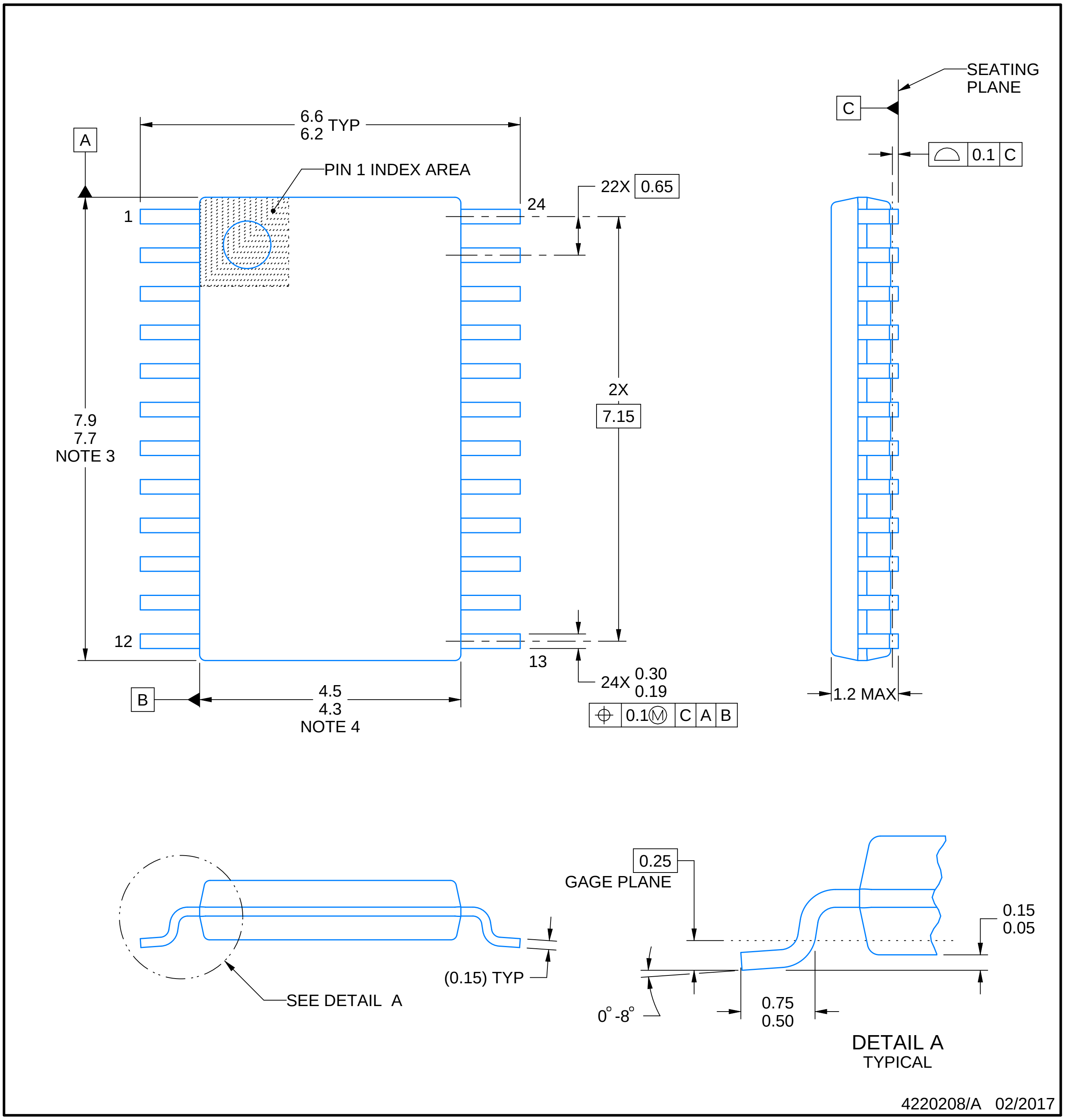


PACKAGE OUTLINE

PW0024A

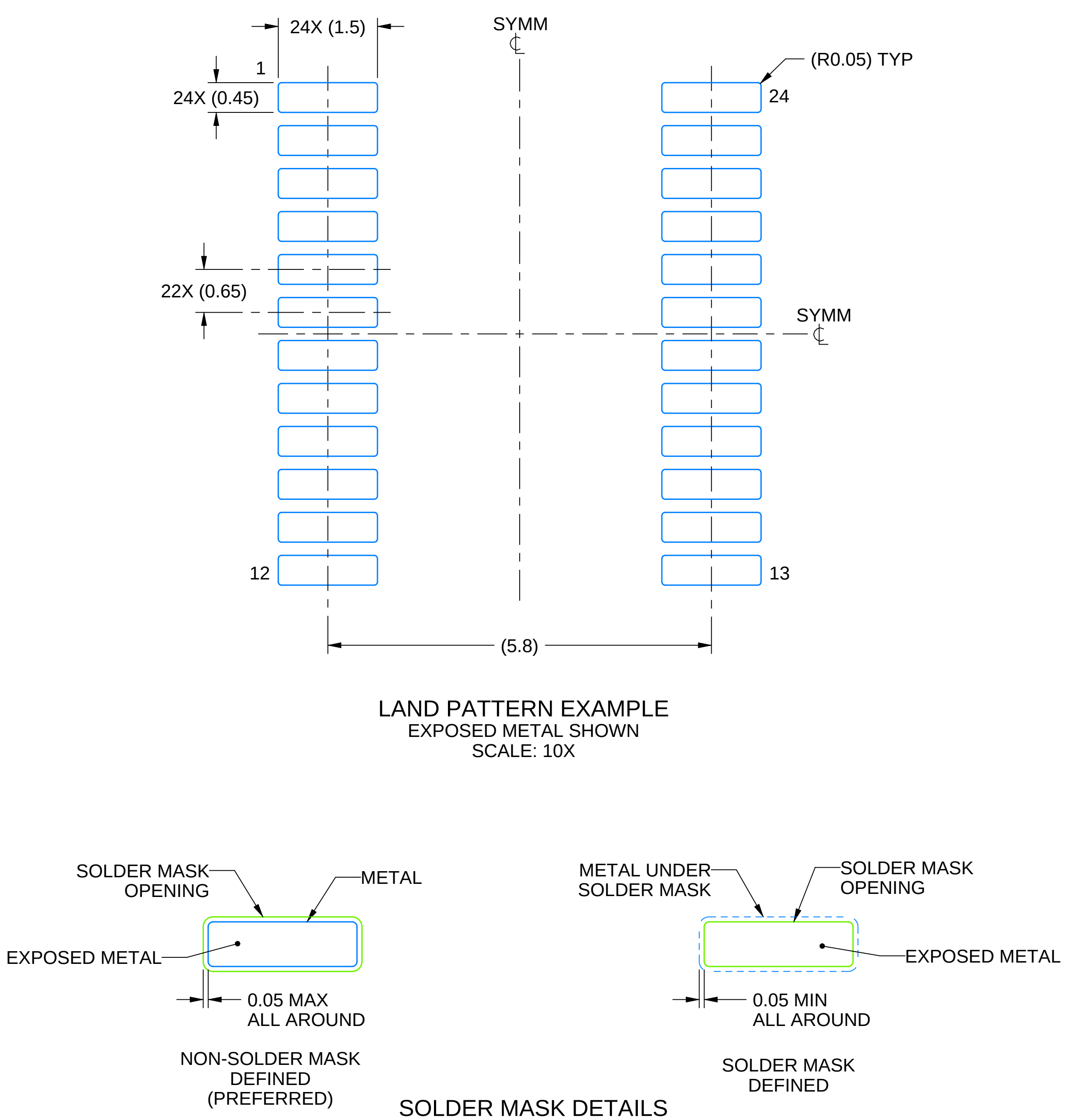
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

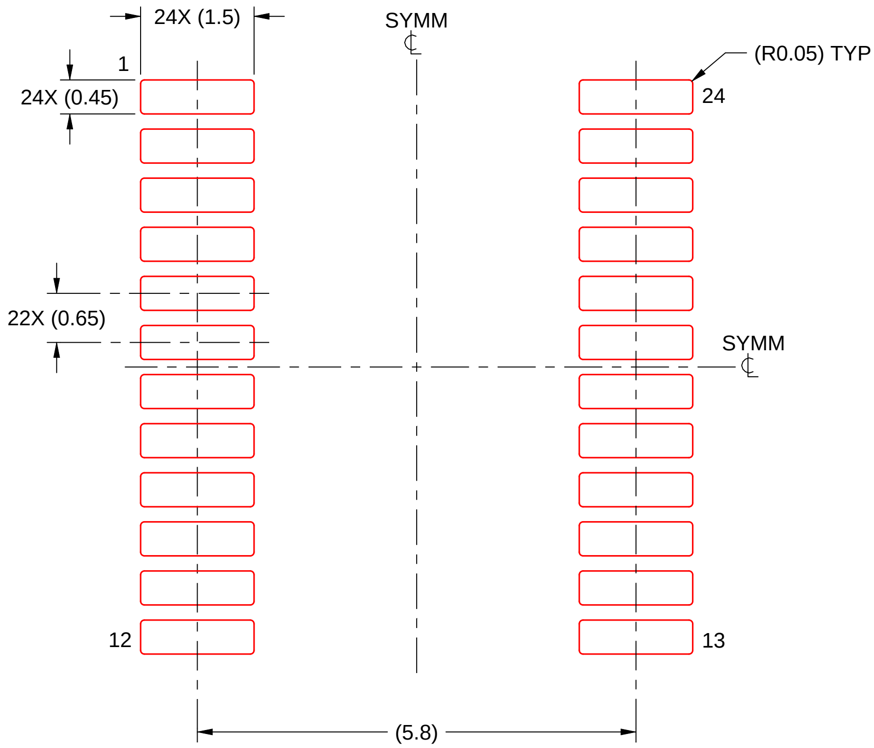
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



4220208/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

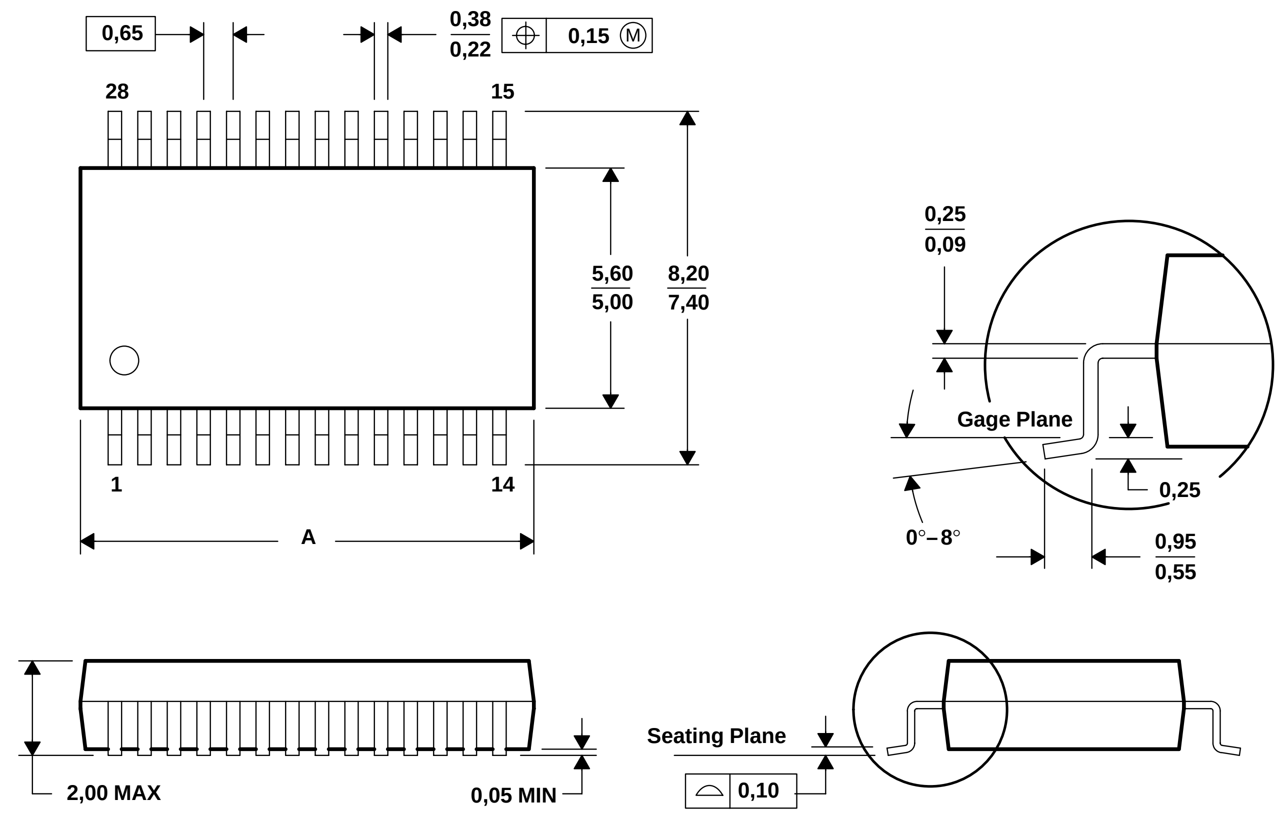
4220208/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

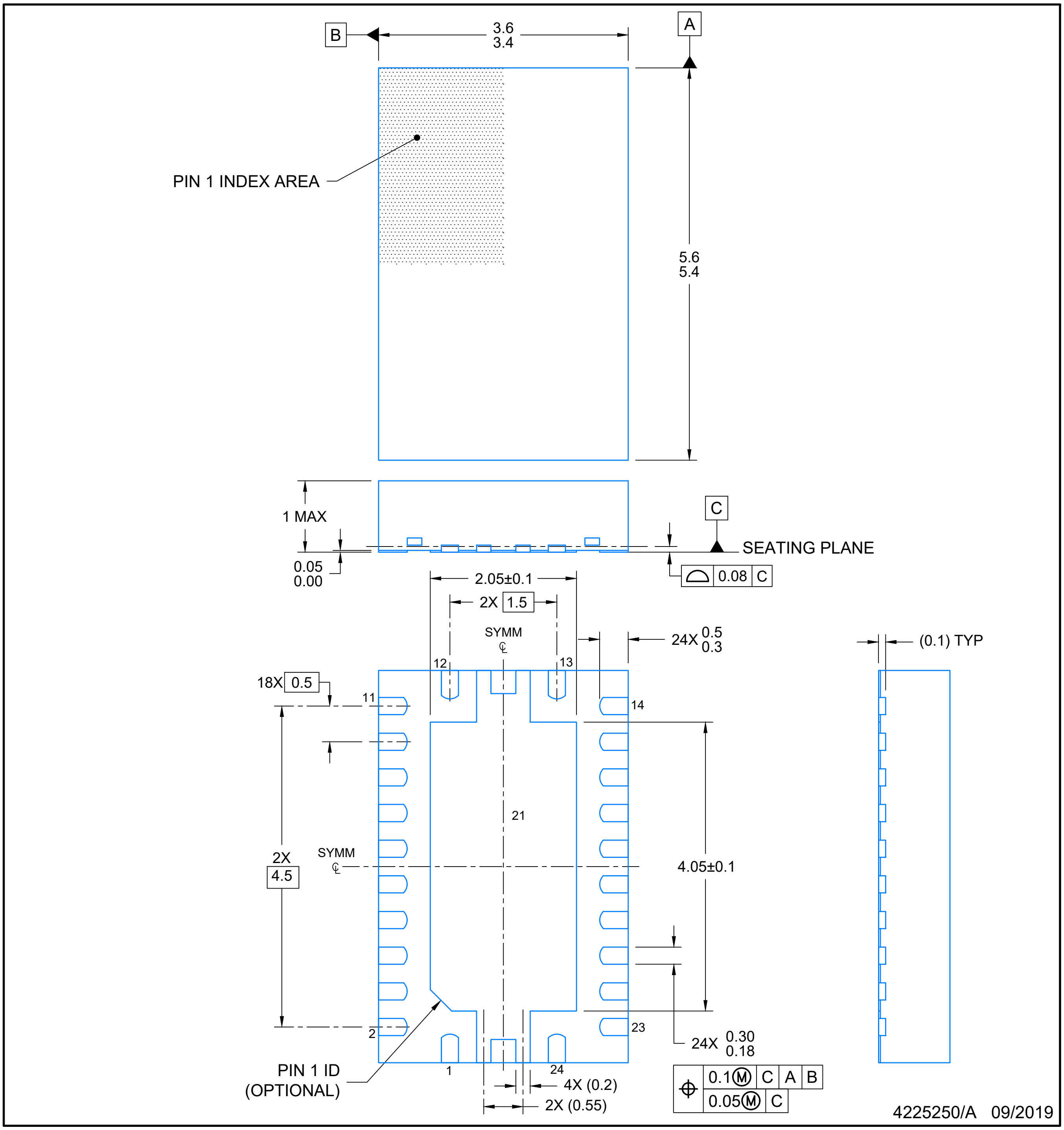
28 PINS SHOWN



PINS ** / DIM	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

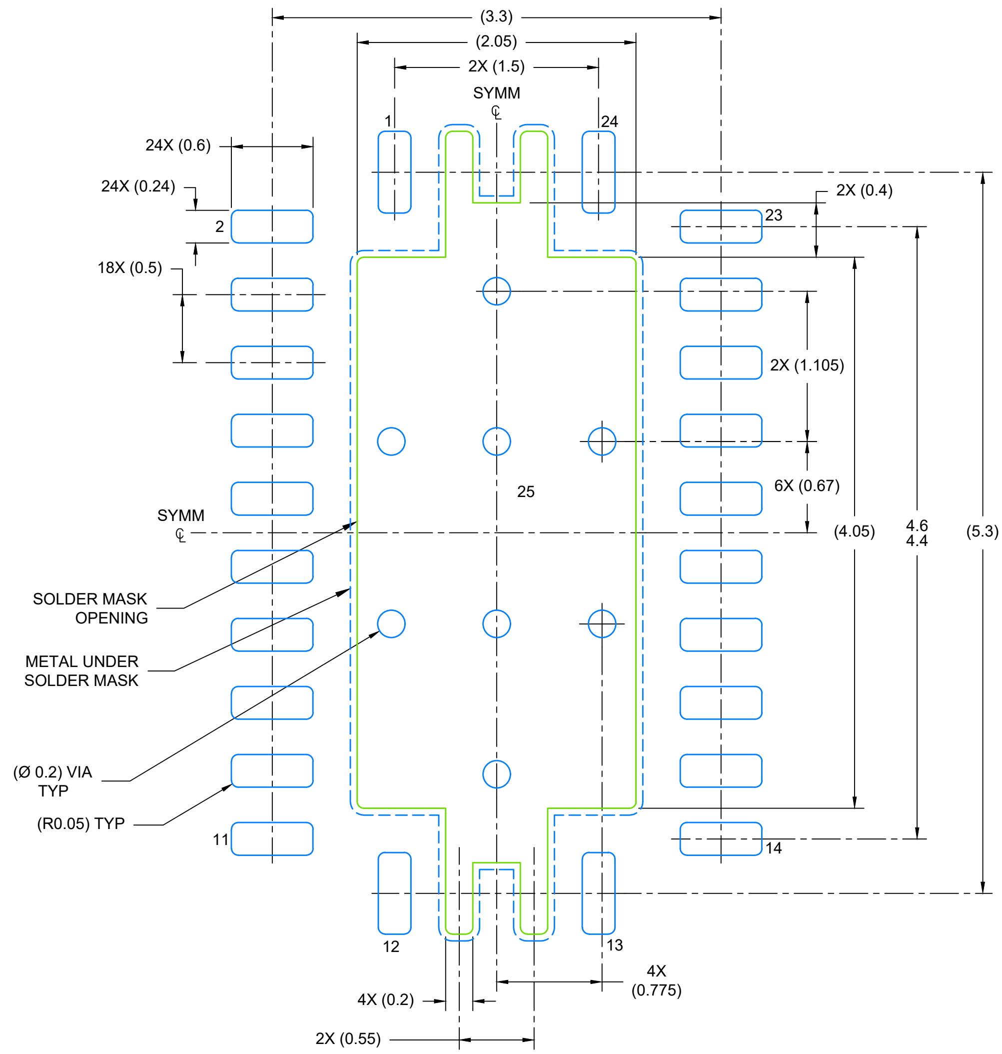
4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

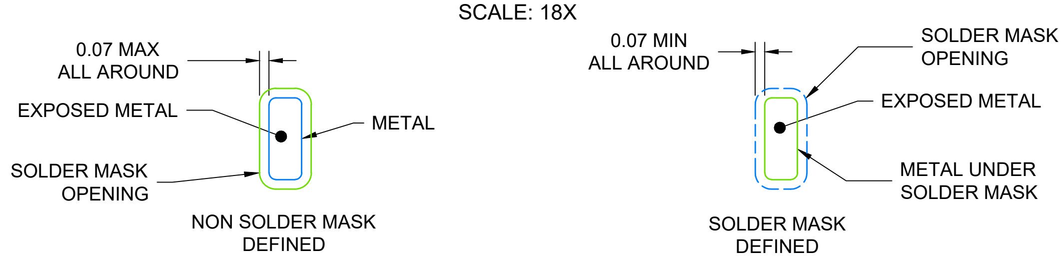


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 18X

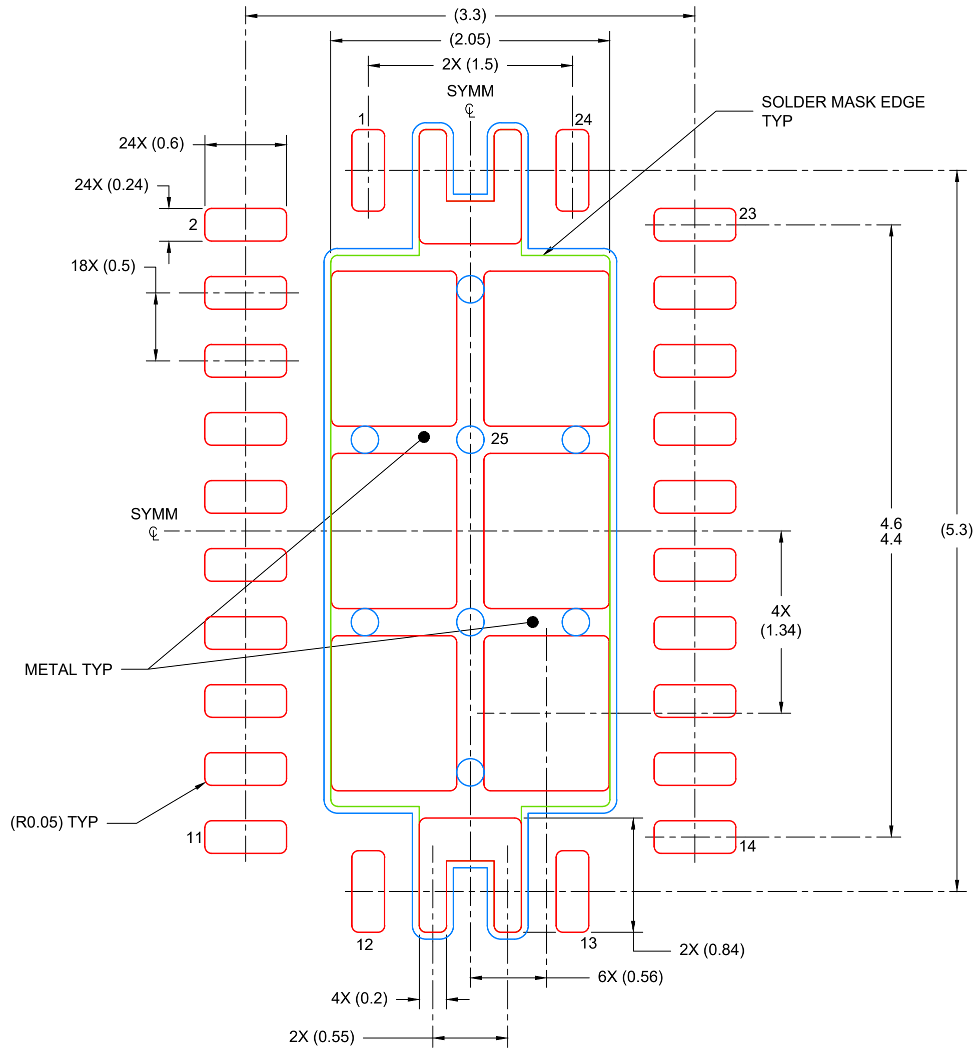


SOLDER MASK DETAILS

4225250/A 09/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
80% PRINTED COVERAGE BY AREA
SCALE: 18X

4225250/A 09/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.