MIC5166

3A High-Speed, Low-V_{IN} DDR Terminator

Features

- Operating Voltage Range:
  - V_{DDQ} Supply: 0.9V to 3.6V
  - Bias Supply: 2.5V to 5.5V
- High Bandwidth: Very Fast Transient Response
- Stable with Two 10 µF Ceramic Output Capacitors
- Two 10 µF Output Capacitors used in Most Applications
- High Output Voltage Accuracy:
  - 0.015% Line Regulation
  - 1.5% Load Regulation
- Logic Level Enable Input
- Power Good (PG)
- Thermally Enhanced 3 mm x 3 mm DFN
- Junction Temperature Range –40°C to +125°C
- This Device Meets DDR4 Requirements

Applications

- Desktop Computers
- Notebook Computers
- Datacom Systems
- Servers
- Video Cards

General Description

The MIC5166 is a 3A, high-speed, linear, low V_{IN}, double data rate (DDR), memory terminator power supply. The part is small and requires small output capacitors, making it a tiny overall solution. This allows it to be conveniently placed close to the DDR memory, minimizing circuit board layout inductance that may cause excessive voltage ripple at the DDR memory.

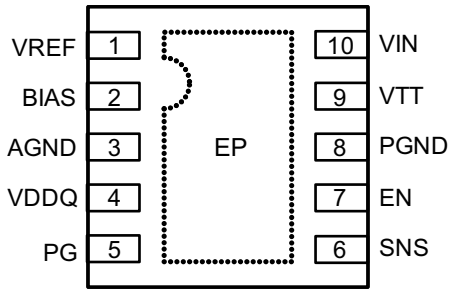
The MIC5166 contains a precision voltage divider network in order to take in the V_{DDQ} voltage as a reference voltage and conveniently output the terminator voltage (V_{TT}) at one half of the V_{DDQ} input voltage.

The MIC5166 is capable of sinking and sourcing up to 3A. It is stable with only two 10 µF ceramic output capacitors. The part is available in a small 3 mm x 3 mm DFN thermally-enhanced package.

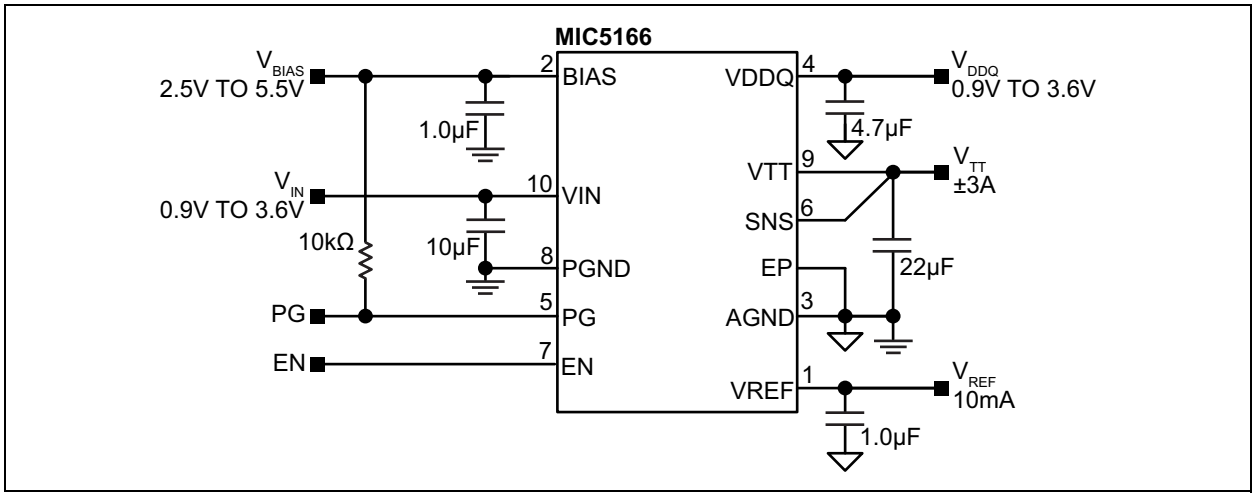
The MIC5166 has a high-side NMOS output stage offering very low output impedance, and very high bandwidth. The NMOS output stage offers a unique ability to respond very quickly to sudden load changes such as is required for DDR memory termination power supply applications.

Package Type

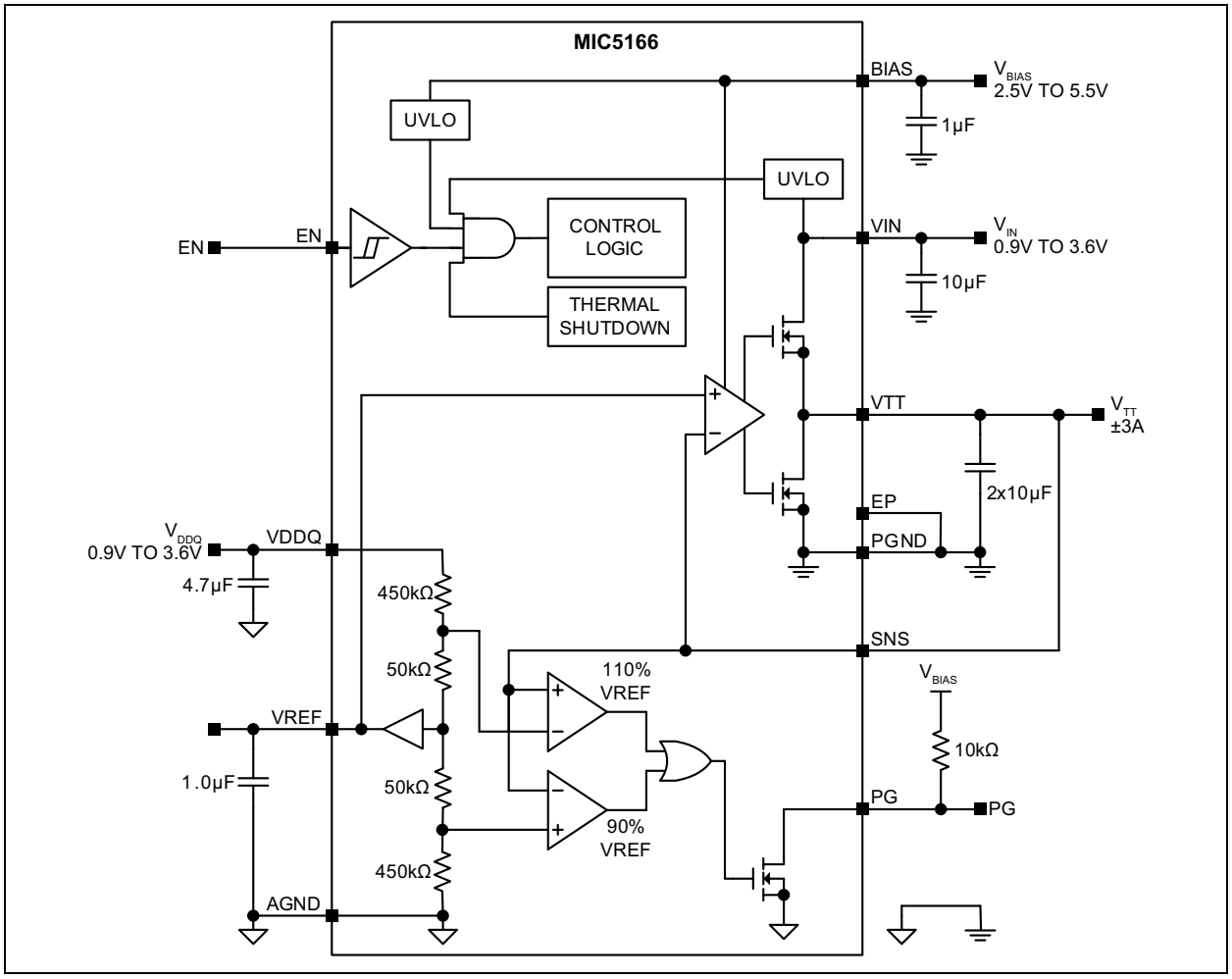
MIC5166
10-Lead 3 mm x 3 mm DFN (ML)
(Top View)



Typical Application Circuit



Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

V_{BIAS} ..... –0.3V to +6V
V_{IN} ..... –0.3V to V_{BIAS}
V_{DDQ} ..... –0.3V to V_{IN}
V_{TT} ..... –0.3V to V_{IN}
V_{EN} ..... –0.3V to V_{BIAS}
V_{PG} ..... –0.3V to V_{BIAS}
PGND to AGND ..... –0.3V to +0.3V
Junction Temperature (T_J) ..... +150°C
Storage Temperature (T_S) ..... –65°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... +260°C
Continuous Power Dissipation (T_A = +25°C; De-Rated 16.4 mW/°C above 25°C) 1.64W
Continuous Power Dissipation (T_A = +85°C) ..... 656 mW
ESD Rating (HBM, Note 1) ..... 2 kV

Operating Ratings ††

Supply Voltage (V_{BIAS}) ..... +2.5V to +5.5V
Supply Voltage (V_{IN}, Note 2) ..... +0.9V to +3.6V
Supply Voltage (V_{DDQ}, Note 3) ..... +0.9V to V_{IN}
Power Good Voltage (V_{PG}) ..... 0V to V_{BIAS}
Enable Input Voltage (V_{EN}) ..... 0V to V_{BIAS}
Junction Temperature Range (T_J) ..... –40°C to +125°C
Package Thermal Resistance
3 mm x 3 mm DFN (θ_{JC}) ..... 28.7°C/W
3 mm x 3 mm DFN (θ_{JA}) ..... 60.7°C/W

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

†† Notice: The device is not guaranteed to function outside its operating ratings.

Note 1: Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5 kΩ in series with 100 pF.

2: If $V_{BIAS} \leq 3.6V$, then $V_{IN(MAX)} = V_{BIAS}$.

3: If $V_{BIAS} \leq 4V$, then $V_{DDQ(MAX)} = 2 \times (V_{BIAS} – 2.2V)$. If $V_{BIAS} > 4V$, then $V_{DDQ(MAX)} = 3.6V$.

ELECTRICAL CHARACTERISTICS

Electrical Characteristics: V_{IN} = 1.5V, V_{BIAS} = 3.3V, V_{DDQ} = 1.5V, T_A = +25°C, unless noted. **Bold** values indicate –40°C ≤ T_J ≤ +125°C. Note 1

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Power Input Supply						
Input Voltage Range	V_{IN}	**0.9**	—	**3.6**	V	—
Undervoltage Lockout Trip Level	—	**0.625**	0.8	**0.9**	V	V_{IN} rising
UVLO Hysteresis	—	—	150	—	mV	—
Quiescent Supply Current	I_{IN}	—	0.1	10	µA	I_{OUT} = 0A
Shutdown Current	I_{SHDN}	—	0.1	5	µA	V_{EN} = 0V
Bias Supply						
Bias Voltage Range	V_{BIAS}	**2.5**	—	**5.5**	V	—
Undervoltage Lockout Trip Level	—	**1.9**	2.23	**2.33**	V	V_{BIAS} rising
UVLO Hysteresis	—	—	70	—	mV	—
Quiescent Supply Current	I_{BIAS}	—	1.6	**3**	mA	I_{OUT} = 1 mA
		—	1.6	**3**		I_{OUT} = 1A
Shutdown Current	I_{SHDN}	—	0.1	5	µA	V_{EN} = 0V
V_{TT} Output						
V_{TT} Accuracy	—	**–25**	—	**25**	mV	Variation from V_{REF}, I_{OUT} = –2A to 2A
Load Regulation	—	—	1.5	**2.1**	%	V_{SNS} = 0.75V, I_{OUT} = +10 mA to +3A
		–1.8	–1.4	—		V_{SNS} = 0.75V, I_{OUT} = –10 mA to –3A
Line Regulation	—	**–0.05**	0.005	**0.05**	%/V	V_{IN} = 1.5V to 3.6V, V_{BIAS} = 5.5V, I_{OUT} = 100 mA
		–0.1	0.015	**0.17**		V_{IN} = 1.5V, V_{BIAS} = 2.5V to 5.5V, I_{OUT} = 100 mA
V_{REF} Output						
V_{REF} Voltage Accuracy	V_{REF}	**–1**	—	**1**	%	Variation from (V_{DDQ}/2), I_{REF} = –10 mA to 10 mA, V_{REF} Output = 0.6V (DDR4), I_{OUT} = 0A.
Bias Supply Dropout Voltage						
Dropout Voltage (V_{BIAS} – V_{TT})	V_{DO}	—	1.15	—	V	I_{OUT} = 100 mA
		—	1.25	—		I_{OUT} = 500 mA
		—	1.65	**2.2**		I_{OUT} = 3A
Enable Control						
EN Logic High Level	V_{IH}	**1.2**	—	—	V	Logic high
EN Logic Low Level	V_{IL}	—	—	**0.2**		Logic low
EN Current	I_{EN}	—	1.0	—	µA	V_{EN} = 0.2V
		—	6.0	—		V_{EN} = 1.2V
Start-Up Time	t_{SU}	—	55	—	µs	From EN pin going high to V_{TT} 90% of V_{REF}

Note 1: Specification for packaged product only.

ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Characteristics: V_{IN} = 1.5V, V_{BIAS} = 3.3V, V_{DDQ} = 1.5V, T_A = +25°C, unless noted. **Bold** values indicate –40°C ≤ T_J ≤ +125°C. Note 1

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Short-Current Protection						
Sourcing Current Limit	I_{LIM}	**3.1**	4.9	**7.8**	A	V_{IN} = 2.7V, V_{TT} = 0V
Sinking Current Limit	I_{LIM}	**–3.1**	–4.9	**–7.8**	A	V_{IN} = 2.7V, V_{TT} = V_{IN}
Internal FETs						
Top MOSFET	$R_{DS(ON)}$	—	130	**190**	mΩ	Source, I_{OUT} = 3A (V_{TT} to PGND)
Bottom MOSFET	$R_{DS(ON)}$	—	130	**190**	mΩ	Sink, I_{OUT} = –3A (V_{IN} to V_{TT})
Power Good (PG)						
PG Window	—	≥90	—	≤110	%	Threshold percent of V_{TT} from V_{REF}
Hysteresis	—	—	2	—	%	—
PG Output Low Voltage	—	—	430	—	mV	I_{PG} = 4 mA (sinking)
PG Leakage Current	—	—	—	**1.0**	µA	V_{PG} = 5.5V, V_{SNS} = V_{REF}
Thermal Protection						
Overtemperature Shutdown	—	—	150	—	°C	T_J rising
Overtemperature Shutdown Hysteresis	—	—	10	—	°C	—

Note 1: Specification for packaged product only.

TEMPERATURE SPECIFICATIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Junction Temperature Range	T_J	–40	—	+125	°C	—
Maximum Junction Temperature	$T_{J(MAX)}$	—	—	+150	°C	—
Lead Temperature	—	—	—	+260	°C	Soldering, 10 sec.
Storage Temperature Range	T_S	–65	—	+150	°C	—
Package Thermal Resistances						
Thermal Resistance, 3x3 DFN 10-Ld	θ_{JC}	—	28.7	—	°C/W	—
Thermal Resistance, 3x3 DFN 10-Ld	θ_{JA}	—	60.7	—	°C/W	—

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperatures above +125°C can impact the device reliability.

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

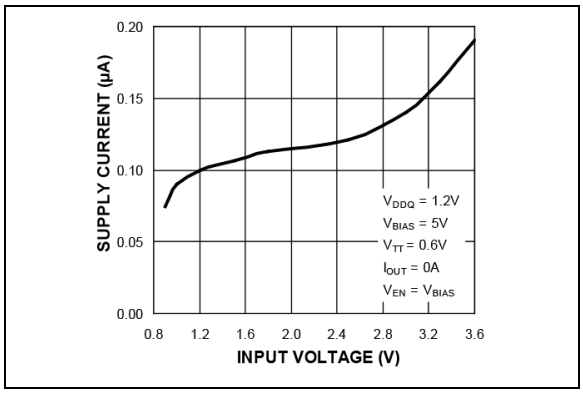


FIGURE 2-1: *V_{IN} Operating Supply Current vs. Input Voltage.*

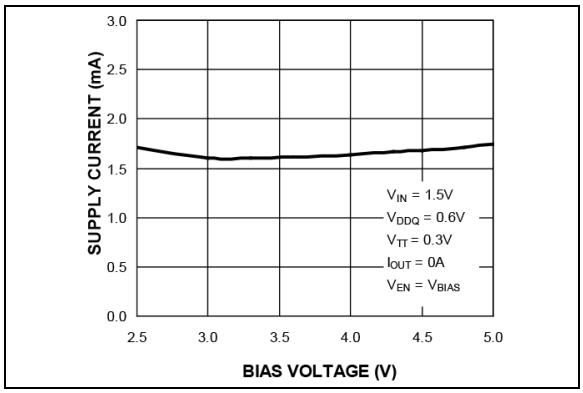


FIGURE 2-4: *V_{BIAS} Operating Supply Current vs. BIAS Voltage.*

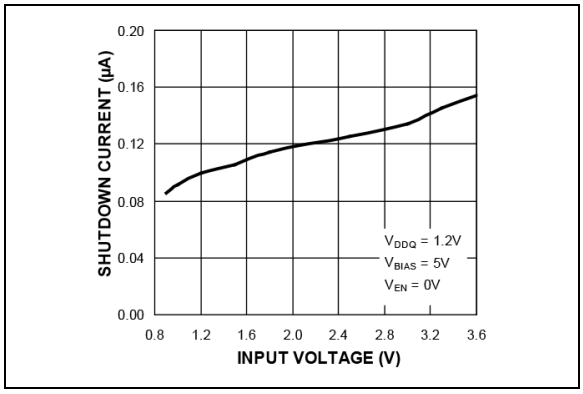


FIGURE 2-2: *V_{IN} Shutdown Current vs. Input Voltage.*

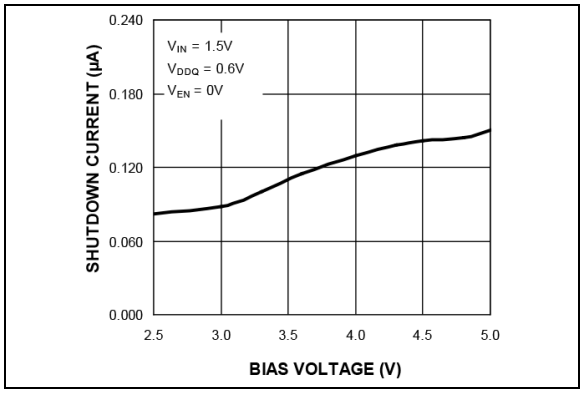


FIGURE 2-5: *V_{BIAS} Shutdown Current vs. BIAS Voltage.*

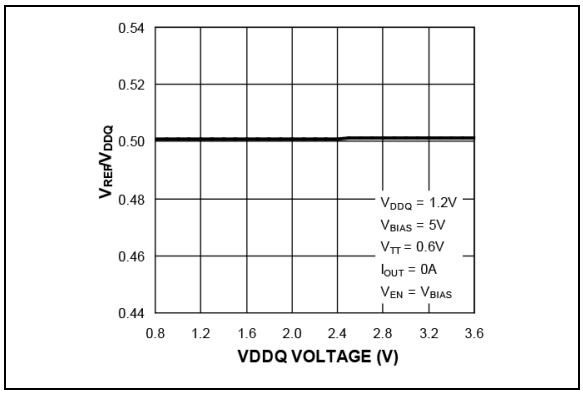


FIGURE 2-3: *V_{REF}/V_{DDQ} Tracking Ratio vs. V_{DDQ} Voltage.*

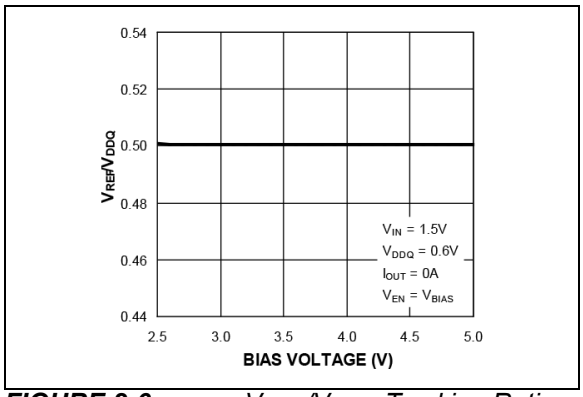


FIGURE 2-6: *V_{REF}/V_{DDQ} Tracking Ratio vs. BIAS Voltage.*

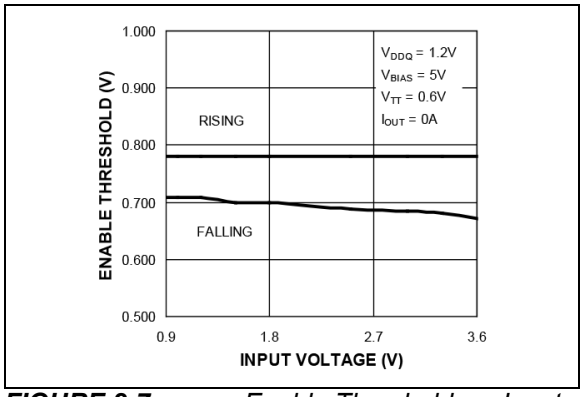


FIGURE 2-7: *Enable Threshold vs. Input Voltage.*

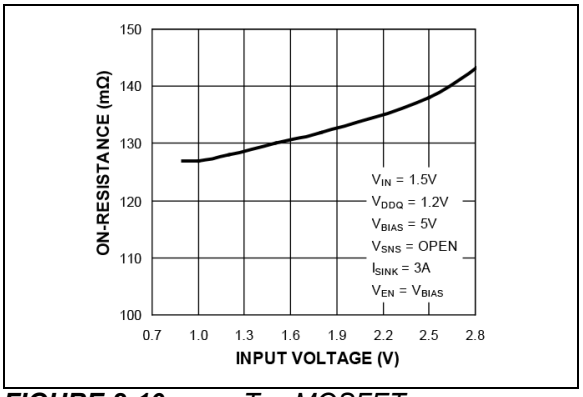


FIGURE 2-10: *Top MOSFET On-Resistance vs. Input Voltage.*

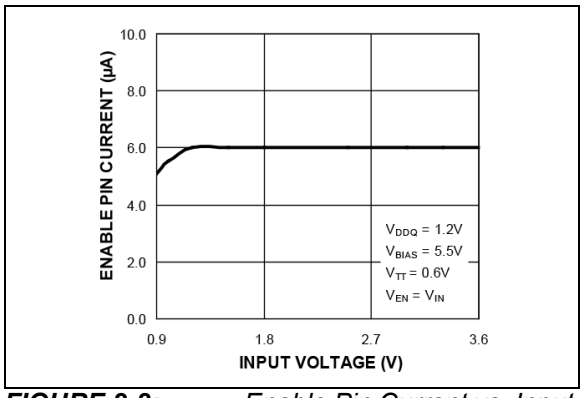


FIGURE 2-8: *Enable Pin Current vs. Input Voltage.*

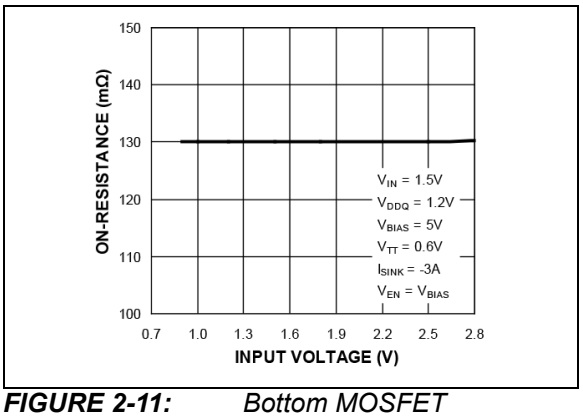


FIGURE 2-11: *Bottom MOSFET On-Resistance vs. Input Voltage.*

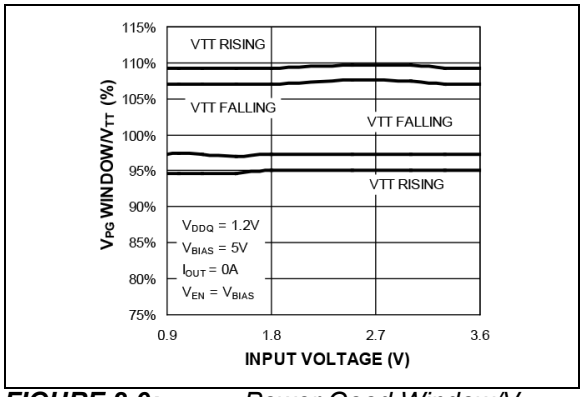


FIGURE 2-9: *Power Good Window/V_{TT} Ratio vs. Input Voltage.*

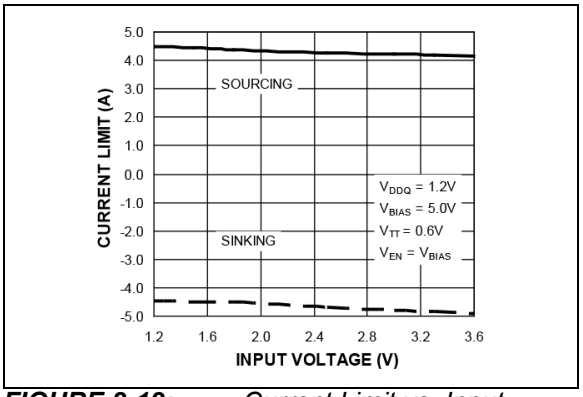


FIGURE 2-12: *Current Limit vs. Input Voltage.*

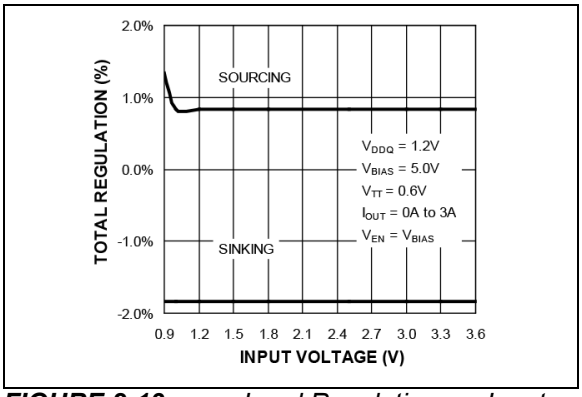


FIGURE 2-13: *Load Regulation vs. Input Voltage.*

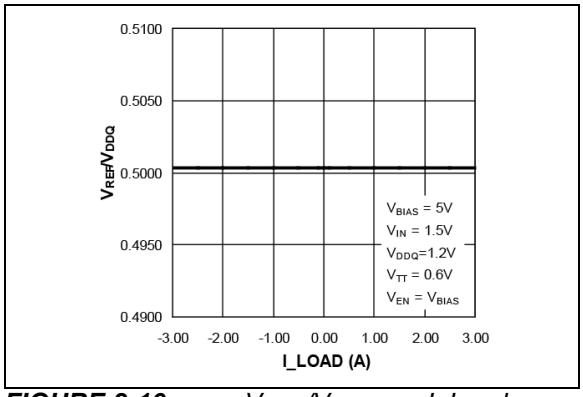


FIGURE 2-16: *V_{REF}/V_{DDQ} vs. I_Load.*

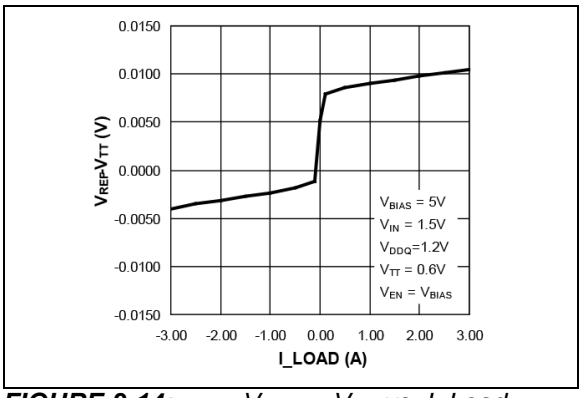


FIGURE 2-14: *$V_{REF} – V_{TT}$ vs. I_Load.*

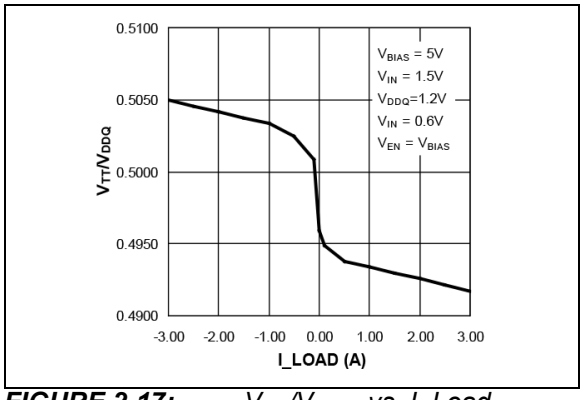


FIGURE 2-17: *V_{TT}/V_{DDQ} vs. I_Load.*

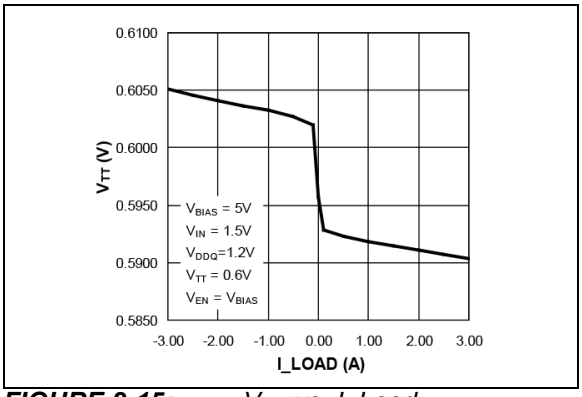


FIGURE 2-15: *V_{TT} vs. I_Load.*

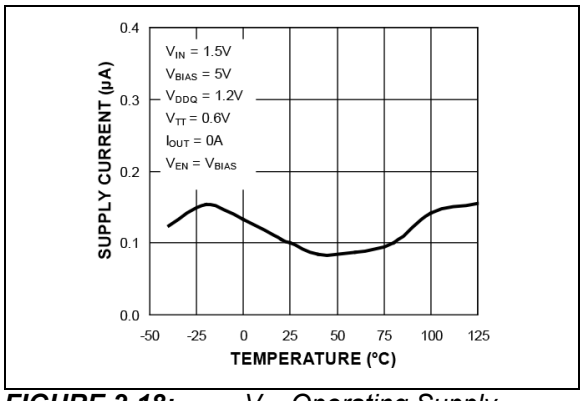


FIGURE 2-18: *V_{IN} Operating Supply Current vs. Temperature.*

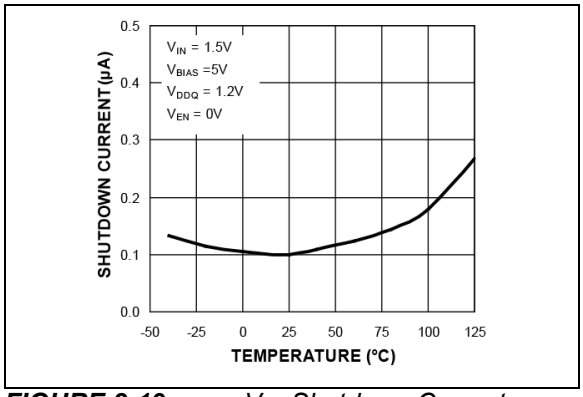


FIGURE 2-19: *V_{IN} Shutdown Current vs. Temperature.*

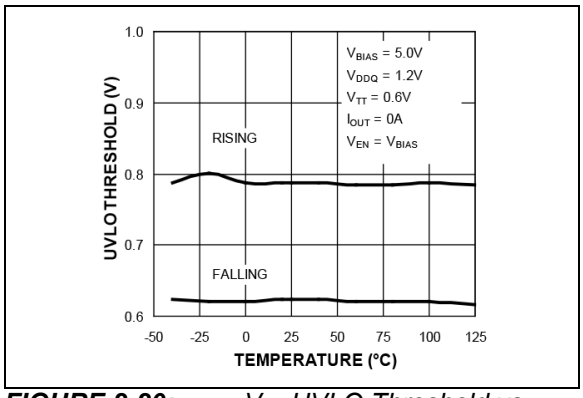


FIGURE 2-20: *V_{IN} UVLO Threshold vs. Temperature.*

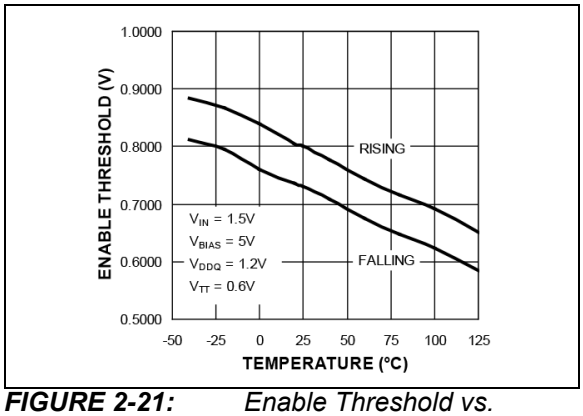


FIGURE 2-21: *Enable Threshold vs. Temperature.*

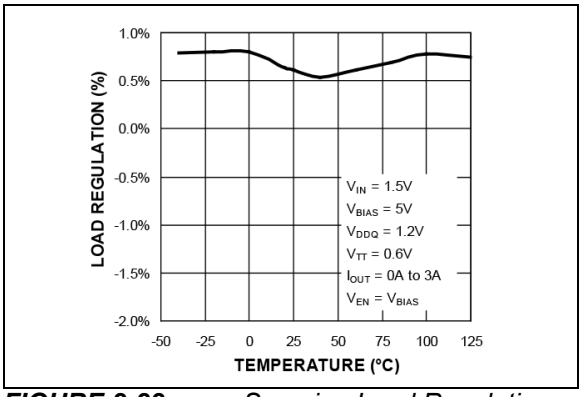


FIGURE 2-22: *Sourcing Load Regulation vs. Temperature.*

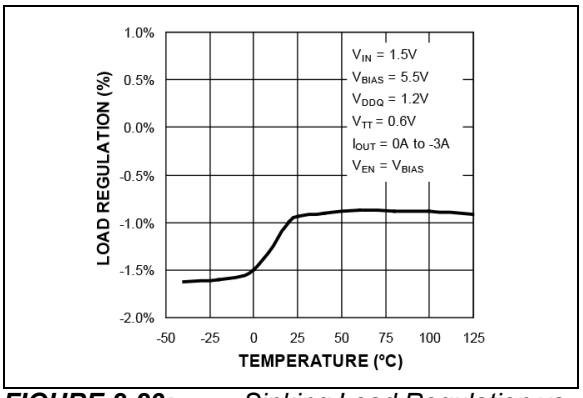


FIGURE 2-23: *Sinking Load Regulation vs. Temperature.*

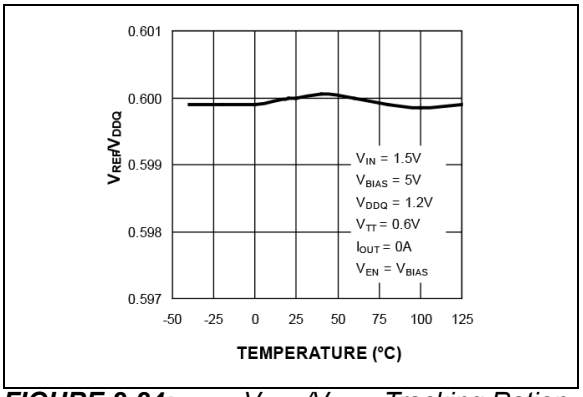


FIGURE 2-24: *V_{REF}/V_{DDQ} Tracking Ration vs. Temperature.*

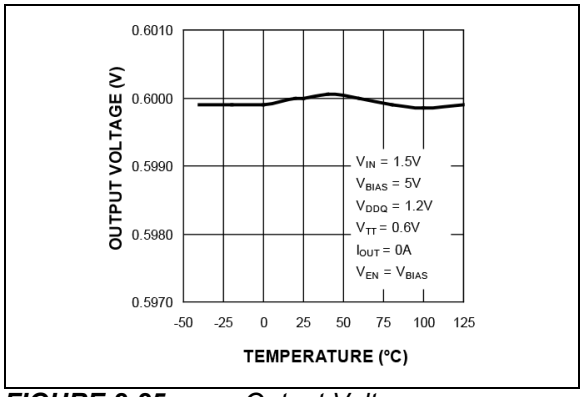


FIGURE 2-25: *Output Voltage vs. Temperature.*

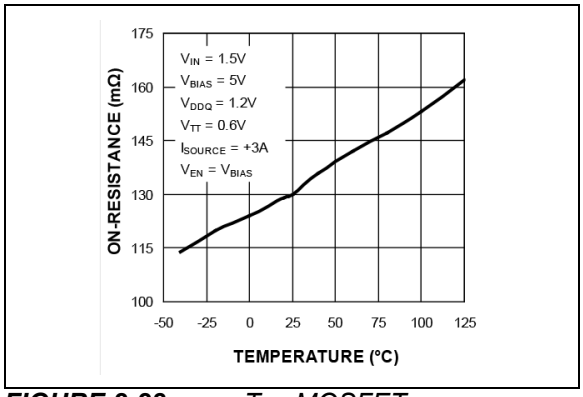


FIGURE 2-28: *Top MOSFET On-Resistance vs. Temperature.*

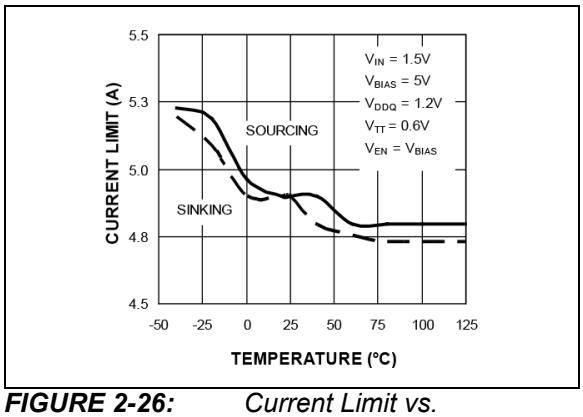


FIGURE 2-26: *Current Limit vs. Temperature.*

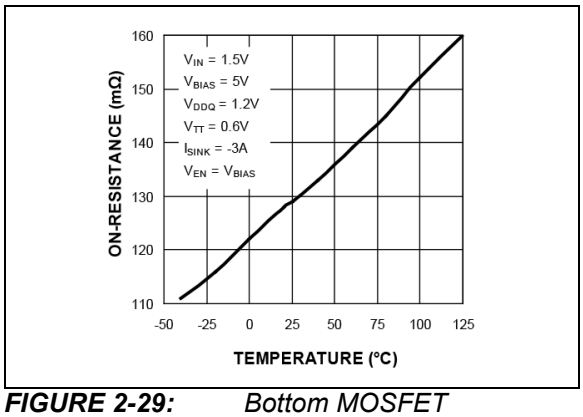


FIGURE 2-29: *Bottom MOSFET On-Resistance vs. Temperature.*

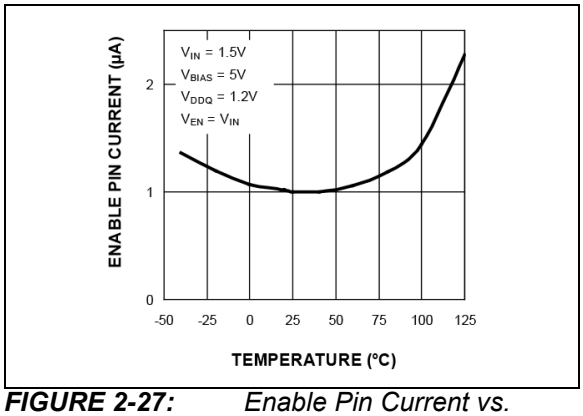


FIGURE 2-27: *Enable Pin Current vs. Temperature.*

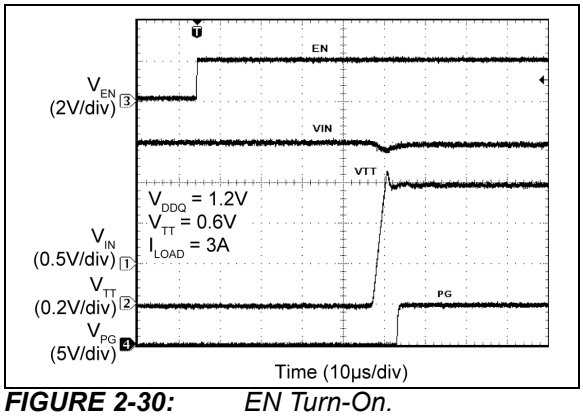


FIGURE 2-30: *EN Turn-On.*

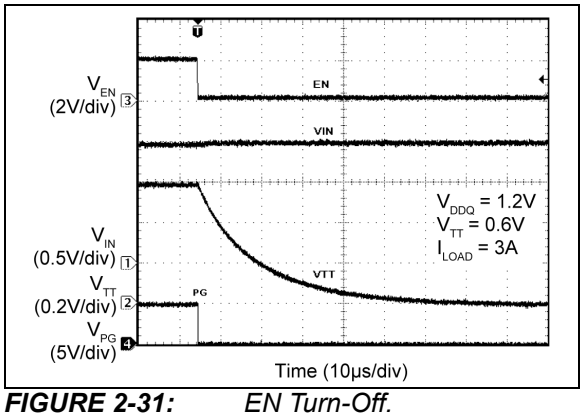


FIGURE 2-31: *EN Turn-Off.*

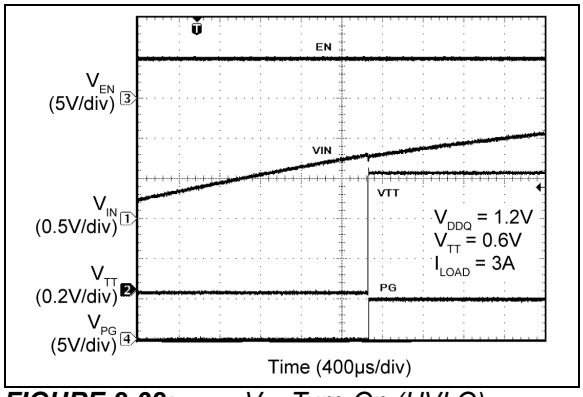


FIGURE 2-32: *V_{IN} Turn-On (UVLO).*

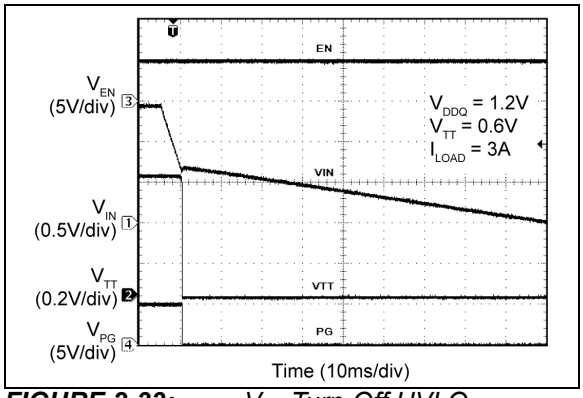


FIGURE 2-33: *V_{IN} Turn-Off UVLO.*

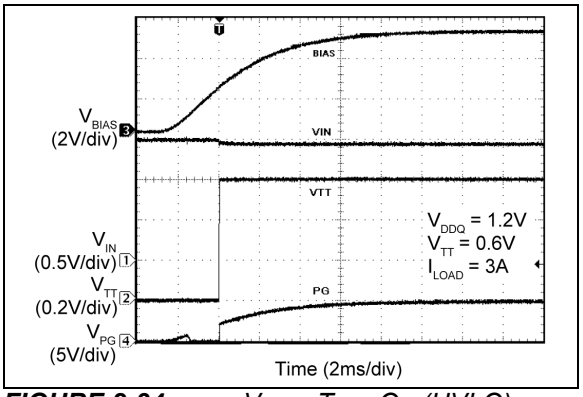


FIGURE 2-34: *V_{BIAS} Turn-On (UVLO).*

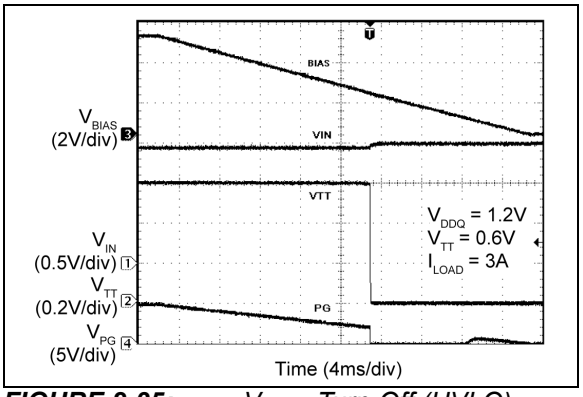


FIGURE 2-35: *V_{BIAS} Turn-Off (UVLO).*

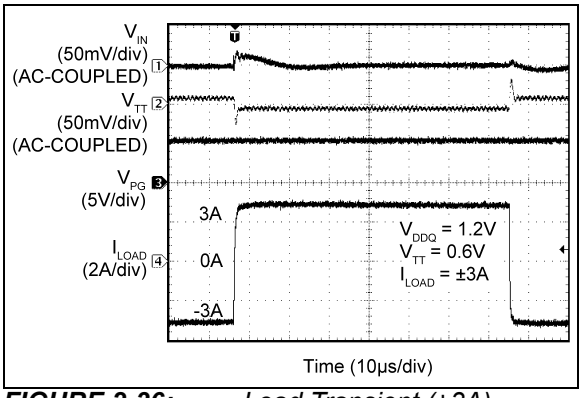


FIGURE 2-36: *Load Transient (±3A).*

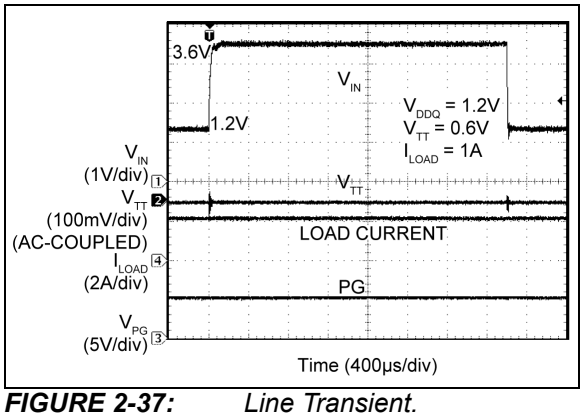


FIGURE 2-37: *Line Transient.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	VREF	Reference Voltage. This output provides an output of the internal reference voltage $V_{DDQ}/2$. The V_{REF} output is used to provide the reference voltage for the memory chip. Connect a 1.0 µF capacitor to ground at this pin. This pin can sink and source 10 mA.
2	BIAS	BIAS Supply Voltage. The BIAS supply is the power MOSFET gate drive supply voltage and the supply bus for the IC. The BIAS voltage must be greater than (V_{TT} + 2.2V). A 1.0 µF ceramic capacitor from the BIAS pin to PGND must be placed next to the IC.
3	AGND	Analog Ground. Internal signal ground for all low-power circuits.
4	VDDQ	Input Supply. VDDQ is connected to an internal precision divider that provides the V_{REF}. Connect a 4.7 µF capacitor to ground at this pin.
5	PG	Power Good. This is an open-drain output that indicates when the output voltage is within ±10% of the reference voltage. The PG flag is asserted typically with 65 µs delay when the enable is set low or when the output goes outside ±10% the window threshold.
6	SNS	Feedback. Input to the error amplifier.
7	EN	Enable. Logic level control of the output. Logic high enables the MIC5166 and a logic low shuts down the MIC5166. In the off state, supply current of the device is greatly reduced (typically 0.2 µA). The EN pin should not be left open.
8	PGND	Power Ground. Internal ground connection to the source of the internal, low-side drive, N-channel MOSFET.
9	VTT	Power Output. This is the connection to the source of the internal high-side N-channel MOSFET and drain of the low-side N-channel MOSFET. This is a high-frequency, high-power connection, therefore two 10 µF output capacitors must be placed as close to the IC as possible.
10	VIN	High-Side N-Channel MOSFET Drain Connection. The V_{IN} operating voltage range is from 0.9V to 3.6V. An input capacitor between the VIN pin and the PGND is required as close to the chip as possible.
EP	ePAD	Exposed Pad. Must be connected to a GND plane for best thermal performance.

4.0 FUNCTIONAL DIAGRAM

DDR memory requires two power supplies: one for the memory chip, referred to as V_{DDQ}, and the other for a termination supply, V_{TT}, which is one-half V_{DDQ}. With memory speeds in excess of 300 MHz, the memory system bus must be treated as a transmission line. To maintain good signal integrity the memory bus must be terminated to minimize signal reflections. Figure 4-1 shows the simplified termination circuit. Each control, address and data lines have these termination resistors R_S and R_T connected to them.

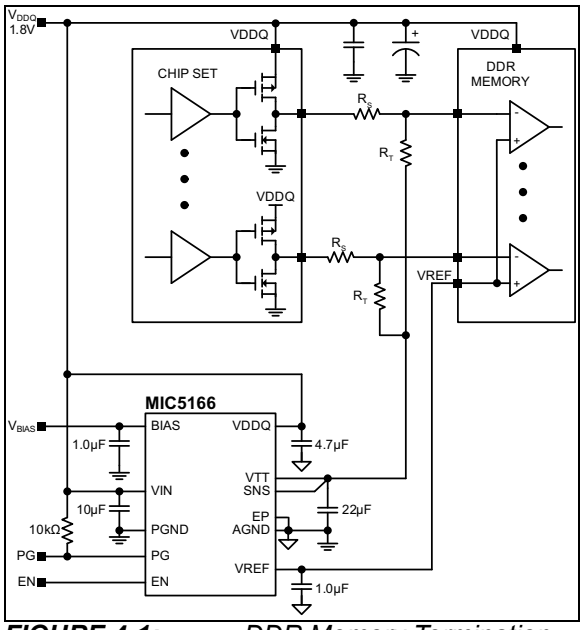


FIGURE 4-1: *DDR Memory Termination Circuit.*

Bus termination provides a means to increase signaling speed while maintaining good signal integrity. The termination network consists of a series resistor (R_S) and a terminating resistor (R_T). Values of R_S range between 10Ω to 30Ω with a typical of 22Ω, while R_T ranges from 22Ω to 28Ω with a typical value of 25Ω. V_{REF} must maintain half V_{DDQ} with a ±1% tolerance, while V_{TT} will dynamically sink and source current to maintain a termination voltage of ±40 mV from the V_{REF} line under all conditions. This method of bus termination reduces common-mode noise, settling time, voltage swings, EMI/RFI, and improves slew rates.

V_{DDQ} powers all the memory ICs, memory drivers and receivers for all the memory bits in the DDR memory system. The MIC5166 regulates V_{TT} to $V_{DDQ}/2$ during sourcing or sinking current.

The memory bits are not usually all at a logic high or logic low at the same time, so the V_{TT} supply is usually not sinking or sourcing –3A or +3A current continuously.

4.1 V_{TT}

V_{TT} is regulated to V_{REF}. Due to high-speed signaling, the load current seen by V_{TT} is constantly changing. To maintain adequate transient response, two 10 µF ceramic capacitors are required. The proper placement of ceramic capacitors is important to reduce both ESR and ESL such that high-current and high-speed transients do not exceed the dynamic voltage tolerance requirement of V_{TT}. The ceramic capacitors provide current during the fast edges of the bus transition. Using several smaller ceramic capacitors distributed near the termination resistors is important to reduce the effects of PCB trace inductance.

4.2 V_{DDQ}

The V_{DDQ} input on the MIC5166 is used to create the internal reference voltage for V_{TT}. The reference voltage is generated from an internal resistor divider network of two 500 kΩ resistors, generating a reference voltage V_{REF} that is $V_{DDQ}/2$. The V_{DDQ} input should be Kelvin connected as close as possible to the memory supply voltage.

Because the reference is simply $V_{DDQ}/2$, any perturbations on V_{DDQ} will also appear at half the amplitude on the reference. For this reason, a 4.7 µF ceramic capacitor is required on the V_{DDQ} supply. This will aid performance by improving the source impedance over a wide frequency range.

4.3 Sense

The sense (SNS) pin provides the path for the error amplifier to regulate V_{TT}. The SNS input must also be Kelvin connected to the V_{TT} bypass capacitors. If the SNS input is connected too close to the MIC5166, the IR drop of the PCB trace can cause the V_{TT} voltage at the memory chip to be too low. Placing the MIC5166 as close as possible to the DDR memory will improve the load regulation performance.

4.4 Enable

The MIC5166 features an active-high enable input (EN) that allows on-off control of the regulator. The current through the device reduces to near “zero” when the device is shutdown, with only <0.2 µA of leakage current. The EN input may be directly tied to V_{BIAS}. The active-high enable pin uses CMOS technology and the enable pin cannot be left floating. A floating enable pin may cause an indeterminate state on the output.

4.5 Power Good (PG)

The power good (PG) output provides an undervoltage and overvoltage fault flag for the V_{TT} output. The PG output remains high as long as V_{TT} is within ±10% range of V_{REF} and goes low if the output moves beyond this range.

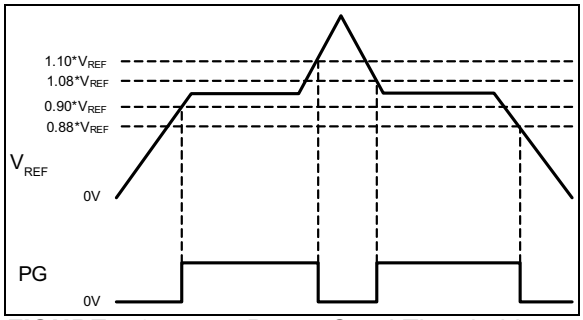


FIGURE 4-2: *Power Good Threshold.*

The PG has an open-drain output. A pull-up resistor must be connected to V_{BIAS}, V_{IN}, or an external source. The external source voltage must not exceed the maximum rating of the pin. The PG pin can be connected to another regulator's enable pin for sequencing of the outputs.

4.6 V_{BIAS} Requirement

A 1 µF ceramic input capacitor is required on the V_{BIAS} pin. To achieve the ultra-fast transient response, the MIC5166 uses an all N-channel power output stage as shown in the Functional Block Diagram. The high-side N-channel MOSFET requires the V_{BIAS} voltage to be 2.2V higher than the V_{TT} to be able to fully enhance the high-side MOSFET.

4.7 V_{IN} Requirement

V_{IN} is used to supply the rail voltage for the high-side N-channel power output stage. It is normally connected to V_{DDQ}, but it can be connected to a lower voltage to reduce power dissipation. In this case, the input voltage must be higher than the V_{TT} voltage to ensure that the output stage is not operating in dropout.

5.0 COMPONENT SELECTION

5.1 Input Capacitor

A 10 µF ceramic input capacitor is all that is required for most applications if it is close to a bulk capacitance.

The input capacitor must be placed on the same side of the board and next to the MIC5166 to minimize the dropout voltage and voltage ringing during transient and short-circuit conditions. It is also recommended that each capacitor to be connected to the PGND directly, not through vias. X7R or X5R dielectric ceramic capacitors are recommended because of their temperature performance. X7R-type capacitors change capacitance by 15% over their operating temperature range and are the most stable type of ceramic capacitors. Z5U and Y5V dielectric capacitors change value by as much as 50% and 60% respectively over their operating temperature ranges. To use a ceramic chip capacitor with Y5V dielectric, the value must be much higher than an X7R ceramic.

5.2 Output Capacitor

As part of the frequency compensation, the MIC5166 requires two 10 µF ceramic output capacitors for best transient performance. To improve transient response, any other type of capacitor can be placed in parallel as long as the two 10 µF ceramic output capacitors are placed next to the MIC5166.

The output capacitor type and placement criteria are the same as the input capacitor. See the Input Capacitor section for a detailed description.

5.3 Thermal Considerations

The MIC5166 is packaged in the 3 mm x 3 mm DFN, a package that has excellent thermal performance. This maximizes heat transfer from the junction to the exposed pad (ePAD) that connects to the ground plane. The size of the ground plane attached to the exposed pad determines the overall thermal resistance from the junction to the ambient air surrounding the printed circuit board.

5.4 Thermal Design

The most complicated design parameters to consider are thermal characteristics. Thermal design requires the following application-specific parameters:

- Maximum ambient temperature (T_A)
- Output current (I_{OUT})
- Output voltage (V_{OUT})
- Input voltage (V_{IN})
- Ground current (I_{GND})

First, calculate the power dissipation of the regulator from these numbers and the device parameters from this data sheet.

EQUATION 5-1:

$$P_D = (V_{IN} - V_{TT}) \times I_{OUT} + (V_{BIAS} \times I_{GND})$$

Where:
I_{OUT} = Approximated by using numbers from the Electrical Characteristics or Typical Performance Curves.

For example, given an expected maximum ambient temperature (T_A) of 70°C with V_{IN} = 1.2V, V_{BIAS} = 3.3V, V_{TT} = 0.9V, and I_{OUT} = 3A, first calculate the expected P_D using Equation 5-1:

EQUATION 5-2:

$$P_D = (1.2V - 0.9V) \times 3A + 3.3V \times 0.0016A = 0.90528W$$

Next, determine the junction temperature for the expected power dissipation above using the thermal resistance (θ_{JA}) of the 10-pin 3 mm x 3 mm DFN (YML) adhering to the following criteria for the PCB design (1oz. copper and 100 mm^2 copper area for the MIC5166):

EQUATION 5-3:

$$T_J = (\theta_{JA} \times P_D) + T_A$$

$$T_J = (60.7°C/W \times 0.90528W) + 70°C$$

$$T_J = 124.95°C$$

To determine the maximum power dissipation allowed that would not exceed the IC's maximum junction temperature (125°C) when operating at a maximum ambient temperature of 70°C:

EQUATION 5-4:

$$P_{D(MAX)} = (T_{J(MAX)} - T_A)/\theta_{JA}$$

$$P_{D(MAX)} = (125°C - 70°C)/(60.7°C/W) = 0.9061W$$

5.5 Thermal Measurements

It is always wise to measure the IC's case temperature to make sure that it is within its operating limits. Although this might seem like a very elementary task, it is very easy to get erroneous results. The most common mistake is to use the standard thermocouple that comes with the thermal voltage meter. This thermocouple wire gauge is large, typically 22 gauge, and behaves like a heat sink, resulting in a lower case measurement.

There are two suggested methods for measuring the IC case temperature: a thermocouple or an infrared thermometer. If a thermocouple is used, it must be constructed of 36 gauge wire or higher to minimize the wire heat sinking effect. In addition, the thermocouple tip must be covered in either thermal grease or thermal glue to make sure that the thermocouple junction makes good contact to the case of the IC. This thermocouple from Omega (5SC-TT-K-36-36) is adequate for most applications.

To avoid this messy thermocouple grease or glue, an infrared thermometer is recommended. Most infrared thermometers' spot size is too large for an accurate reading on small form factor ICs. However, an IR thermometer from Optris has a 1 mm spot size, which makes it ideal for the 3 mm x 3 mm DFN package.

5.6 Sequencing

The following diagrams illustrate methods for connecting MIC5166s to achieve sequencing requirements:

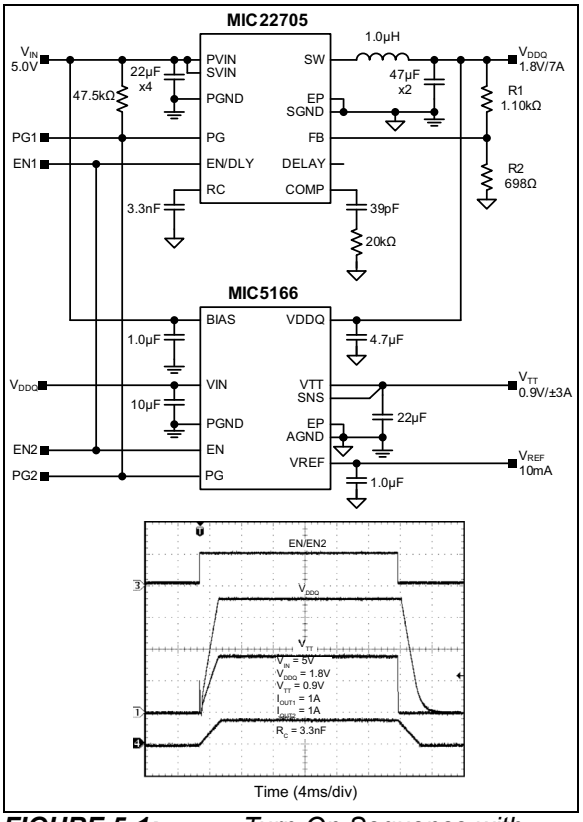


FIGURE 5-1: *Turn-On Sequence with Soft-Start (R_C = 3.3 nF).*

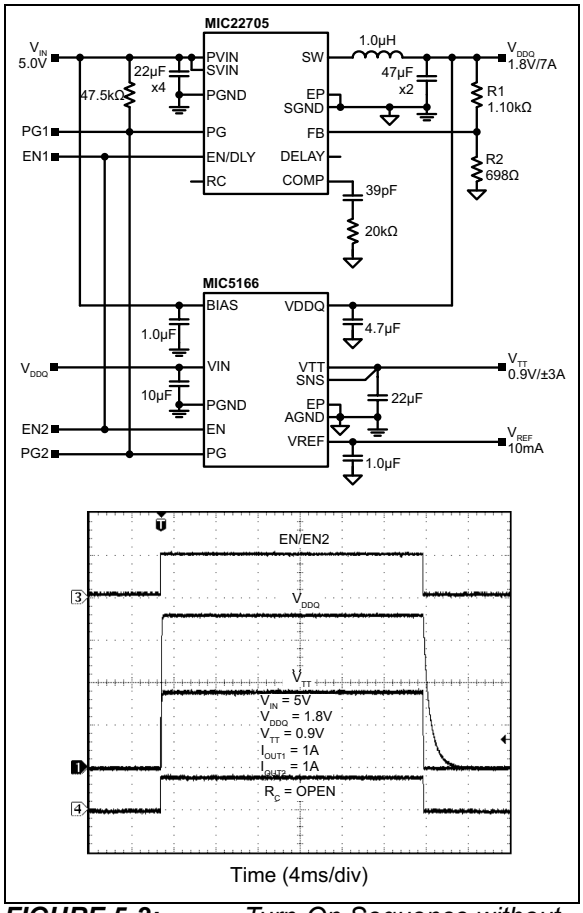


FIGURE 5-2: *Turn-On Sequence without Soft-Start (R_C = Open).*

6.0 PCB LAYOUT GUIDELINES

To minimize EMI and output noise, follow these layout recommendations.

PCB layout is critical to achieve reliable, stable, and efficient performance. A ground plane is required to control EMI and minimize the inductance in power, signal, and return paths.

The following guidelines should be followed to ensure proper operation of the MIC5166 converter.

6.1 IC

- The 10 µF ceramic capacitor, which is connected to the VIN pin, must be located right at the IC. The VDDQ pin is very noise sensitive and placement of the capacitor is very critical. Use wide traces to connect to the VDDQ and AGND pins.
- The signal ground pin (AGND) must be connected directly to the ground planes. Do not route the AGND pin to the PGND Pad on the top layer.
- Place the IC close to the point-of-load (POL).
- Use wide traces to route the input and output power lines.
- Signal and power grounds should be kept separate and connected at only one location.

6.2 Input Capacitor

- A 10 µF X5R or X7R dielectric ceramic capacitor is recommended on each of the VIN pins for bypassing.
- Place the input capacitors on the same side of the board and as close to the IC as possible.
- Keep both the VIN pin and PGND connections short.
- Place several vias to the ground plane close to the input capacitor ground terminal.
- Use either X7R or X5R dielectric input capacitors. Do not use Y5V or Z5U type capacitors.
- Do not replace the ceramic input capacitor with any other type of capacitor. Any type of capacitor can be placed in parallel with the input capacitor.
- If a Tantalum input capacitor is placed in parallel with the input capacitor, it must be recommended for switching regulator applications and the operating voltage must be derated by 50%.
- In hot-plug applications, a Tantalum or Electrolytic bypass capacitor must be used to limit the overvoltage spike seen on the input supply with power is suddenly applied.

6.3 Output Capacitor

- Use a wide trace to connect the output capacitor ground terminal to the input capacitor ground terminal.
- Phase margin will change as the output capacitor value and ESR changes. Contact the factory if the output capacitor is different from what is shown in the BOM.
- The feedback divider network must be place close to the IC with the bottom of R2 connected to AGND.
- The feedback trace should be separate from the power trace and connected as close as possible to the output capacitor. Sensing a long high current load trace can degrade the DC load regulation.

7.0 EVALUATION BOARD SCHEMATICS

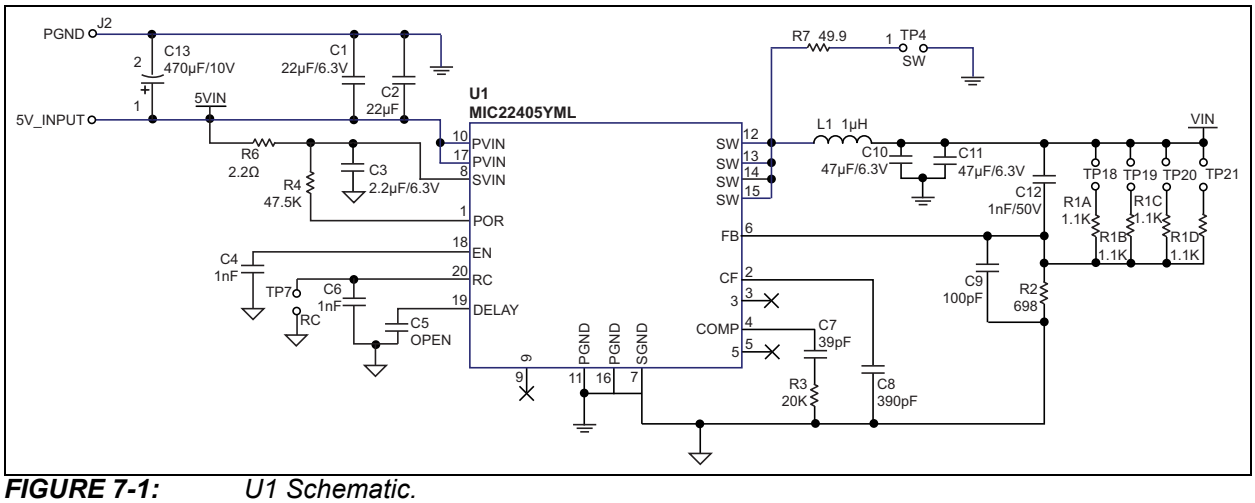


FIGURE 7-1: *U1 Schematic.*

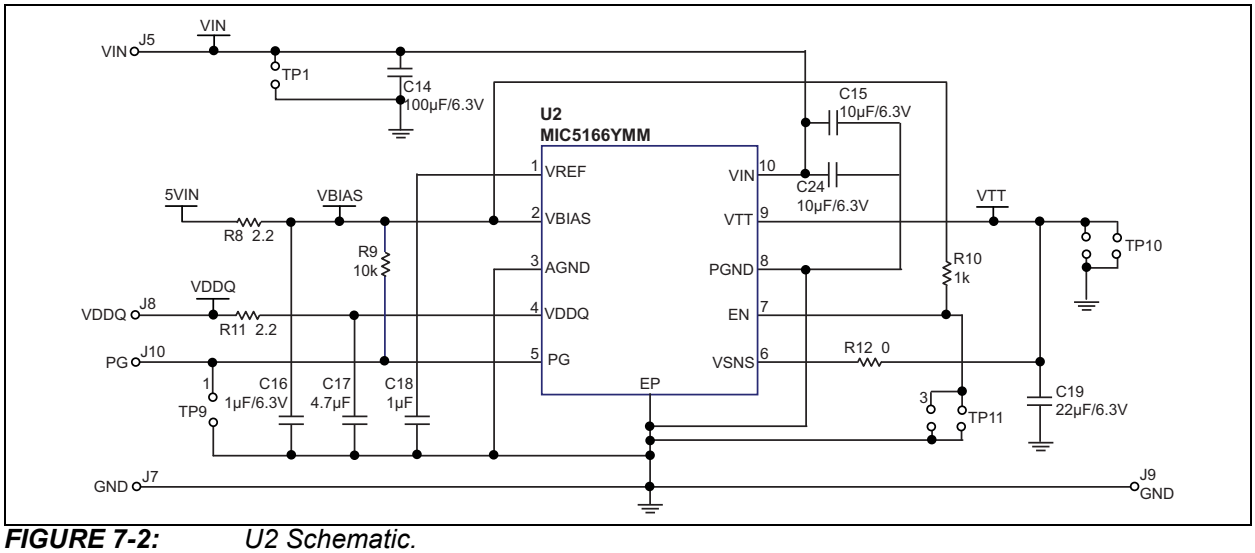


FIGURE 7-2: *U2 Schematic.*

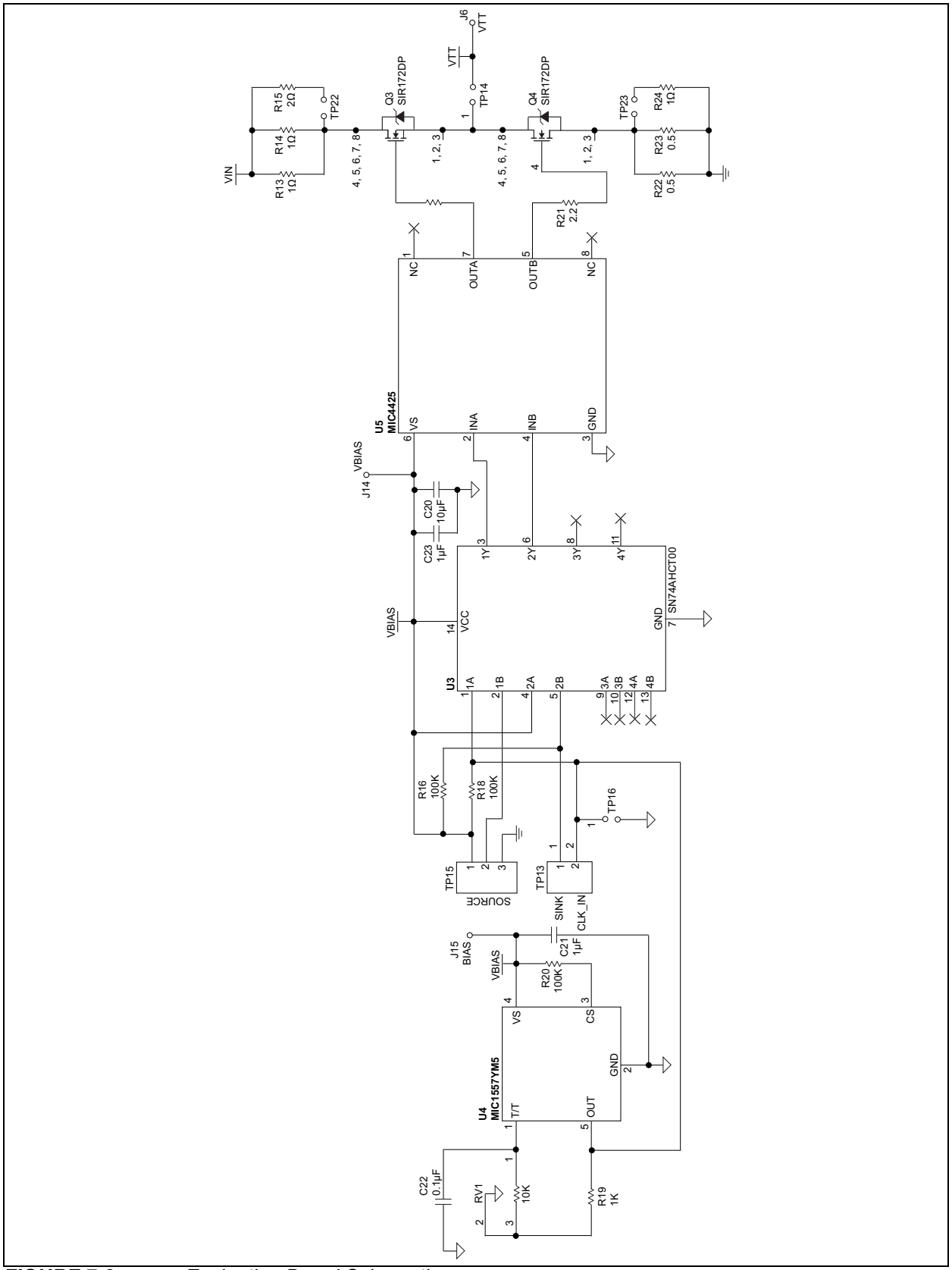


FIGURE 7-3: *Evaluation Board Schematic.*

TABLE 7-1: BILL OF MATERIALS

Item	Part Number	Manufacturer	Description	Qty.
C1, C2, C19	08056D226MAT	AVX	22 µF, 6.3V, ceramic capacitor, X5R, 0805	3
	C2012X5R0J226K	TDK		
	GRM21BR60J226ME39L	Murata		
C3	08056D225KAT2A	AVX	2.2µF, 6.3V, ceramic capacitor, X5R, 0805	1
	C2012X5R0J225K	TDK		
	GRM21BR60J225KA01L	Murata		
C4, C6, C12	06035C102KAT	AVX	1 nF, 50V, ceramic capacitor, X7R, 0603	3
	C1608X7R1H102K	TDK		
	GRM188R71H102KA01D	Murata		
C7	06035A390JAT2A	AVX	39 pF, 50V, ceramic capacitor, NPO, 0603	1
	C1608C0G1H390J	TDK		
	GRM1885C1H390JA01D	Murata		
C8	06035A391JAT2A	AVX	390 pF, 50V, ceramic capacitor, NPO, 0603	1
	C1608C0G1H391J	TDK		
	GRM188R71H391KA01D	Murata		
C9	06035A101JAT2A	AVX	100 pF, 50V, ceramic capacitor, NPO, 0603	1
	C1608C0G1H101J	TDK		
	GRM1885C1H101JA01D	Murata		
C10, C11	12066D476MAT2A	AVX	47µF, 6.3V, ceramic capacitor, X5R,1206	2
	C3216X5R0J476M	TDK		
	GRM31CR60J476ME19L	Murata		
C14	12106D107MAT2A	AVX	100 µF, 6.3V, ceramic capacitor, X5R, 1210	1
	C3225X5R0J107M	TDK		
	GRM32ER60J107ME20L	Murata		
C15, C20, C24	06036D106MAT	AVX	10 µF, 6.3V, ceramic capacitor, X5R, 0603	3
	FP3-1R0-R	TDK		
	GRM188R60J106ME47D	Murata		
C16, C18, C21, C23	06036D105KAT2A	AVX	1 µF, 6.3V, ceramic capacitor, X5R, 0603	4
	C1608X5R0J105K	TDK		
	GRM188R60J105KA01D	Murata		
C17	06036D475KAT2A	AVX	4.7 µF, 6.3V, ceramic capacitor, X5R, 0603	1
	C1608X5R0J475M	TDK		
	C1608X5R0J475M	Murata		
C5	—	—	N.U. 0603 ceramic capacitor	1
C22	06035C104KAT2A	AVX	0.1 µF, 50V, ceramic capacitor, X7R, 0603	1
	C1608X7R1H104K	TDK		
	GRM188R71H104KA93D	Murata		
C13	EEU-FC1A471	Panasonic	470 µF/10V, Elect., 20%, 8x11.5, Radial	1
L1	FP3-1R0-R	Cooper	1 µH,6.26A Inductor	1
Q3, Q4	NDS8425	Fairchild	MOSFET, N-CH 20V 7.4A 8-SOIC	2
R1A	CRCW0603300RFKEA	Vishay Dale	300Ω, resistor, 1%, 0603	1
R1B	CRCW06031101FKEA	Vishay Dale	510Ω, resistor, 1%, 0603	1
R1C	CRCW0603806RFKEA	Vishay Dale	806Ω, resistor, 1%, 0603	1
R1D	CRCW06031K10FKEA	Vishay Dale	1.1 kΩ, resistor, 1%, 0603	1

TABLE 7-1: BILL OF MATERIALS (CONTINUED)

Item	Part Number	Manufacturer	Description	Qty.
R2	CRCW0603698RFKEA	Vishay Dale	698Ω, resistor, 1%, 0603	1
R3	CRCW06032002FKEA	Vishay Dale	20 kΩ, resistor, 1%, 0603	1
R4	CRCW06034752FKEA	Vishay Dale	47.5 kΩ, resistor, 1%, 0603	1
R6, R8, R11, R17, R21	CRCW06032R20RFKEA	Vishay Dale	2.2Ω, resistor, 1%, 0603	5
R7	CRCW060349R9RFKEA	Vishay Dale	49.9Ω, resistor, 1%, 0603	1
R9	CRCW06031002FKEA	Vishay Dale	10 kΩ, resistor, 1%, 0603	1
R10, R19	CRCW06031K00FKEA	Vishay Dale	1 kΩ, resistor, 1%, 0603	2
R12	CRCW0603000RFKEA	Vishay Dale	0Ω, resistor, 1%, 0603	1
R13, R14, R24	CRCW25121R00FKEGHP	Vishay Dale	1Ω, resistor, 1.5W, 1%, 2512	3
R15	CRCW25122R00JNEG	Vishay Dale	2Ω, resistor, 1.5W, 1%, 2512	1
R16, R18, R20	CRCW06031003FKEA	Vishay Dale	100 kΩ, resistor, 1%, 0603	3
R22, R23	LR2512-R50FW	Vishay Dale	0.5Ω, resistor, 1.5W, 1%, 2512	2
RV1	PV36W103C01B00	Murata	Pot, 10 kΩ, 0.5W, 9.6x5x10	1
U1	MIC22405YML	Microchip	4A, Synchronous Buck Regulator	1
U2	MIC5166YMM	Microchip	3A High-Speed Low V_{IN} DDR Terminator	1
U3	SN74AHCT00RGYR	TI	Quad, 2IN Pos-NAND Gate, 14-pin, QFN	1
U4	MIC1557YM5	Microchip	5 MHz RC Timer Oscillator	1
U5	MIC4425	Microchip	3A Dual Inverting and Non-Inverting MOSFET Driver	1

7.1 PCB Layout Recommendations

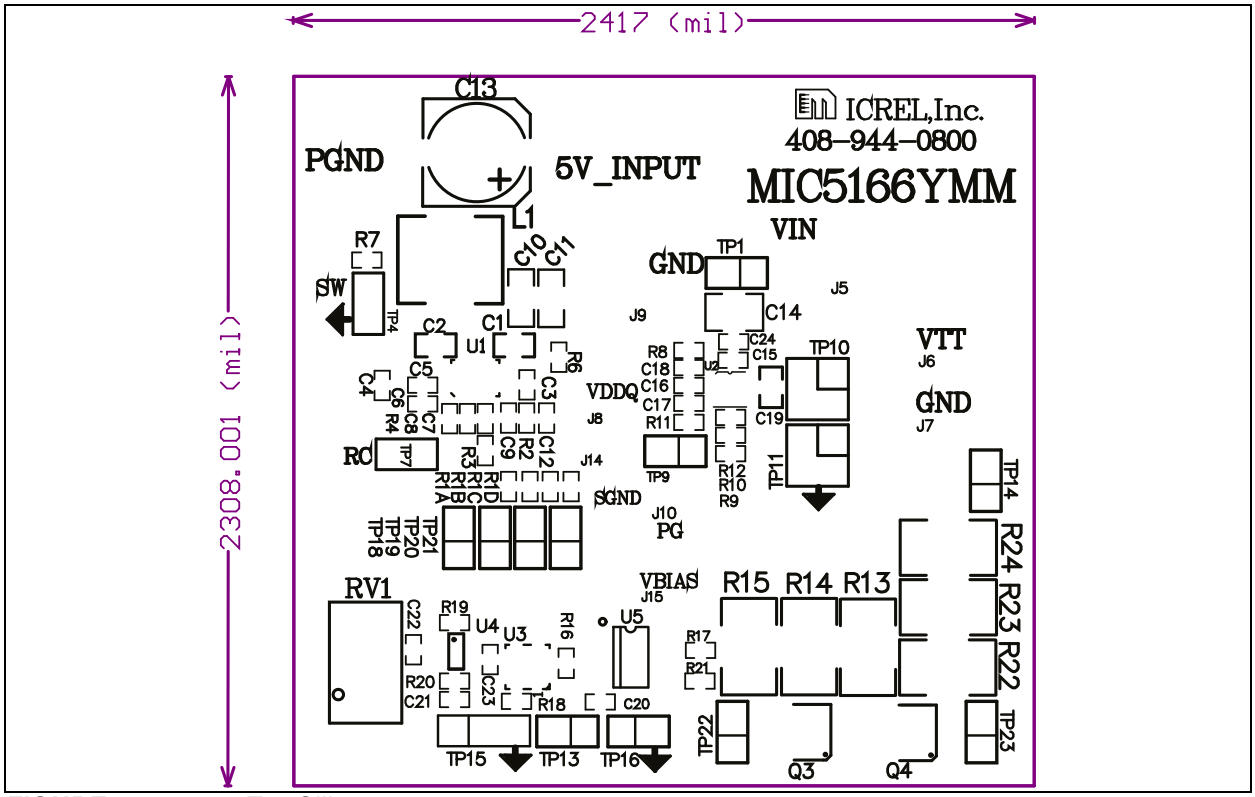


FIGURE 7-4: *Top Silk.*

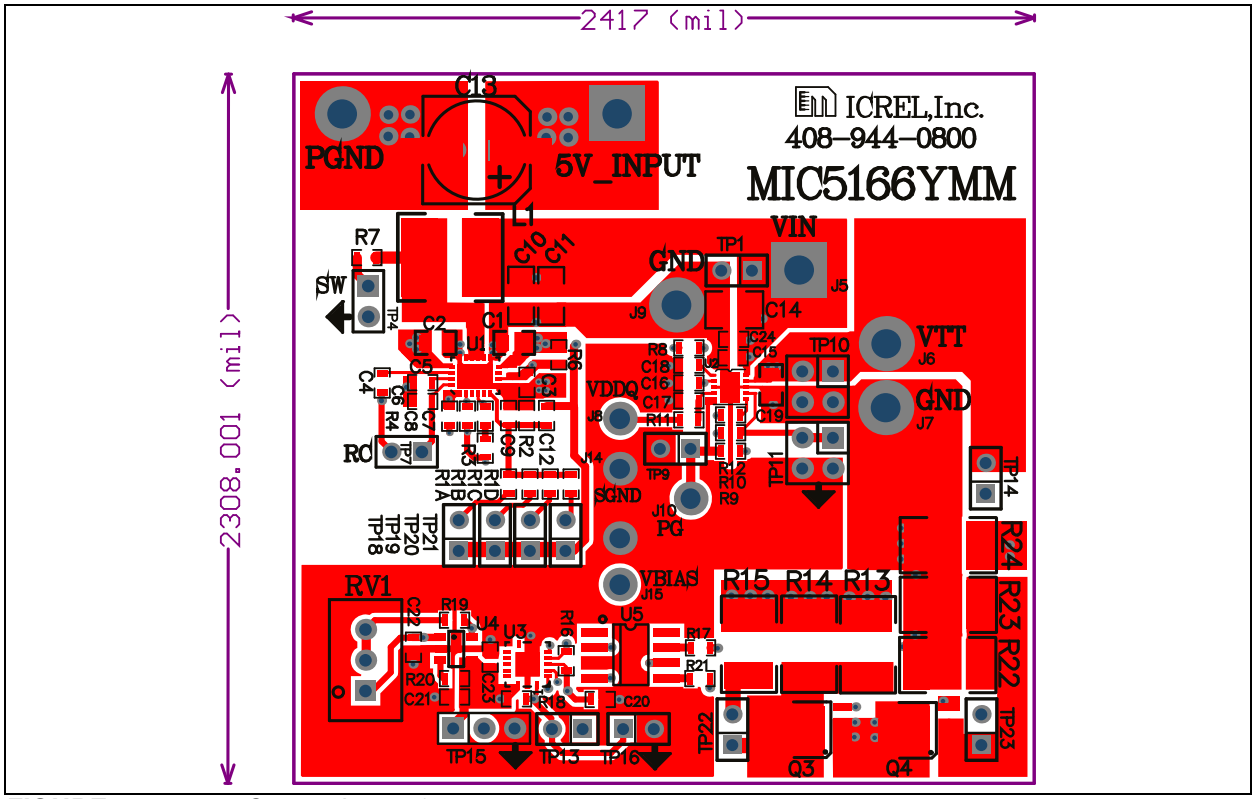


FIGURE 7-5: *Copper Layer 1.*

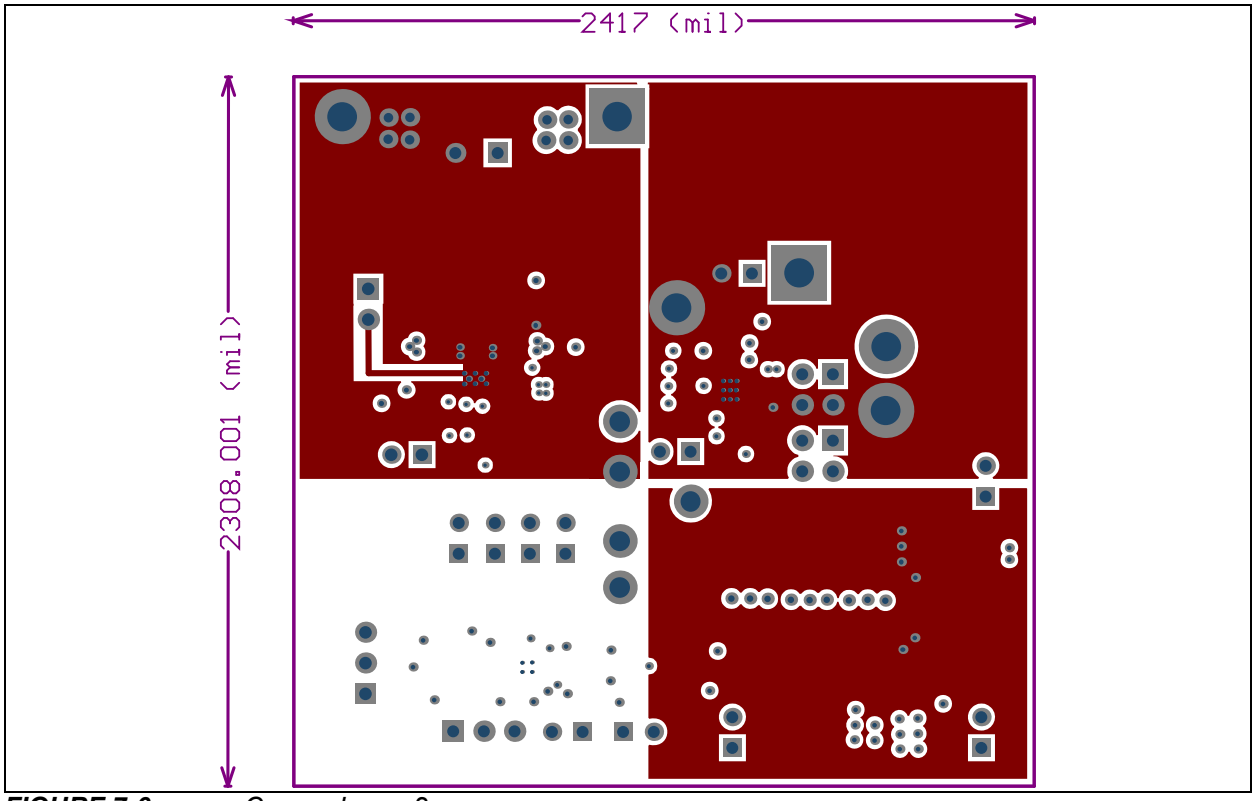


FIGURE 7-6: *Copper Layer 2.*

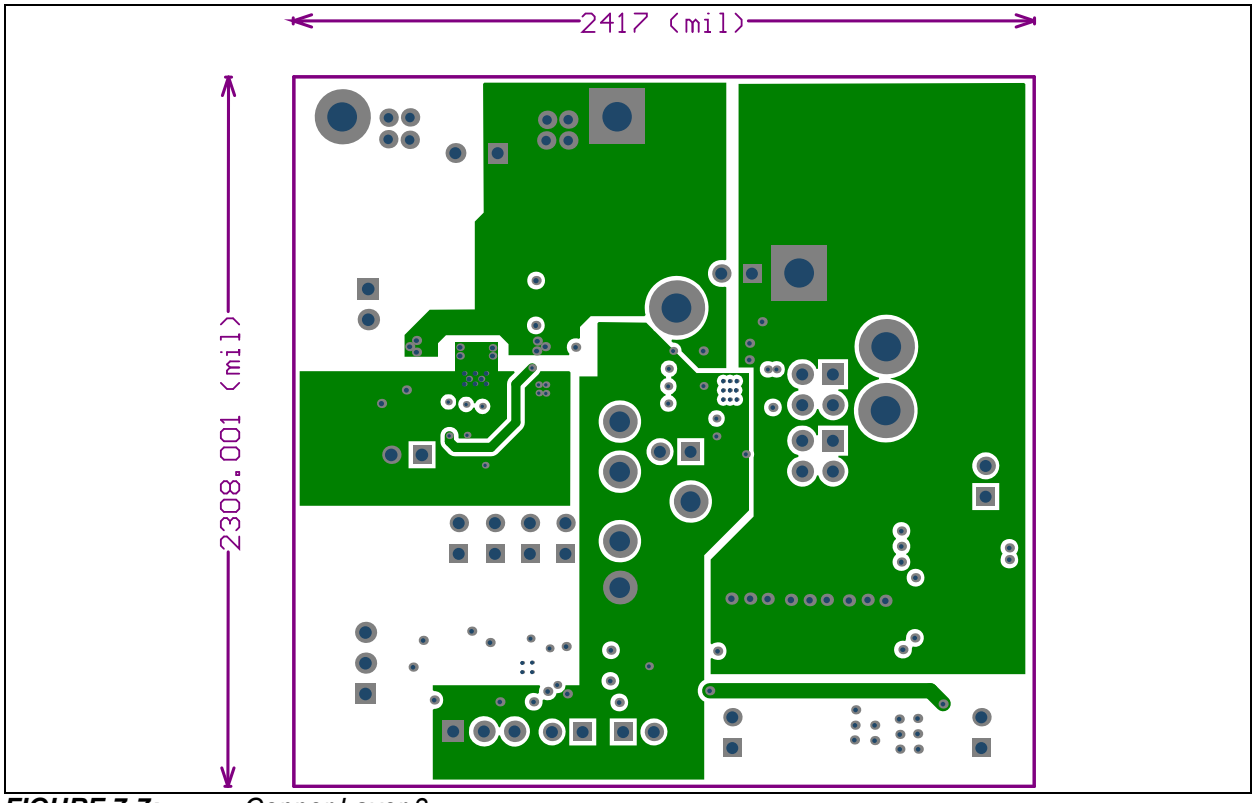


FIGURE 7-7: *Copper Layer 3.*

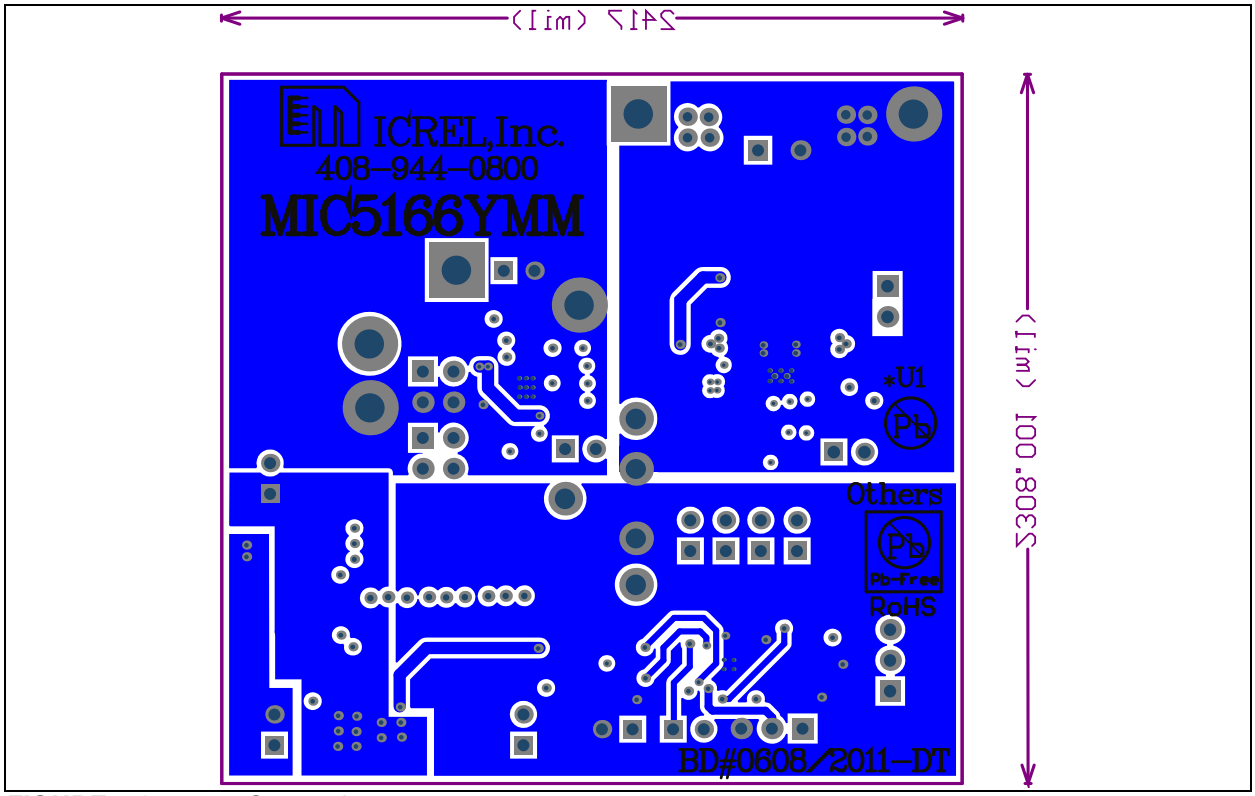


FIGURE 7-8: *Copper Layer 4.*

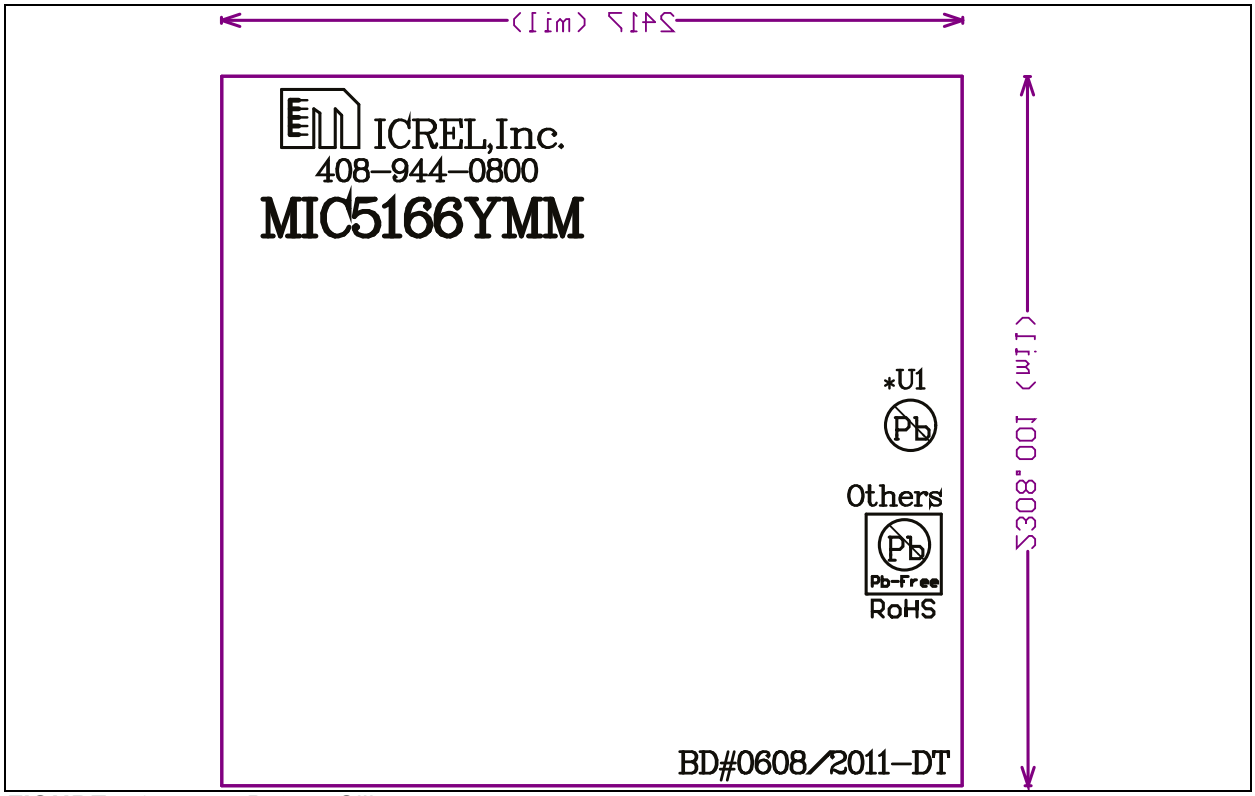
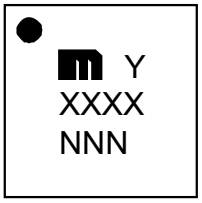


FIGURE 7-9: *Bottom Silk.*

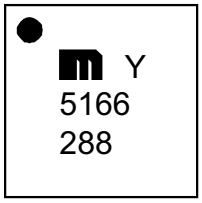
8.0 PACKAGING INFORMATION

8.1 Package Marking Information

10-Lead DFN*



Example

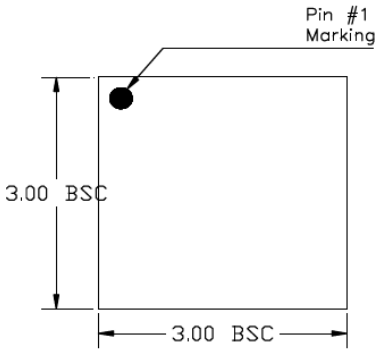


Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.	
	Underbar (_) and/or Overbar (¯) symbol may not be to scale.	

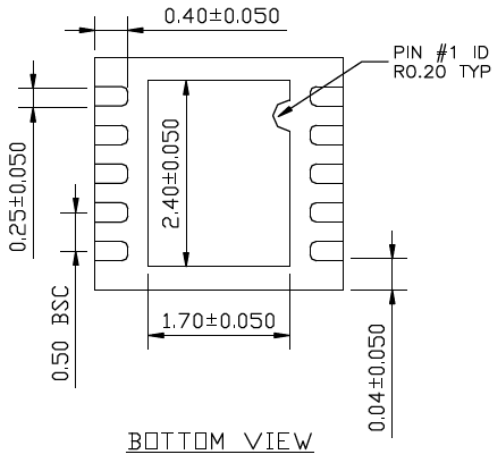
10-Lead 3 mm x 3 mm DFN Package Outline & Recommended Land Pattern

TITLE
10 LEAD DFN 3x3mm PACKAGE OUTLINE & RECOMMENDED LAND PATTERN

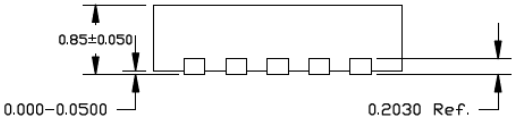
DRAWING #	DFN33-10LD-PL-1	**UNIT**	MM



TOP VIEW
NOTE: 1, 2, 3



BOTTOM VIEW
NOTE: 1, 2, 3

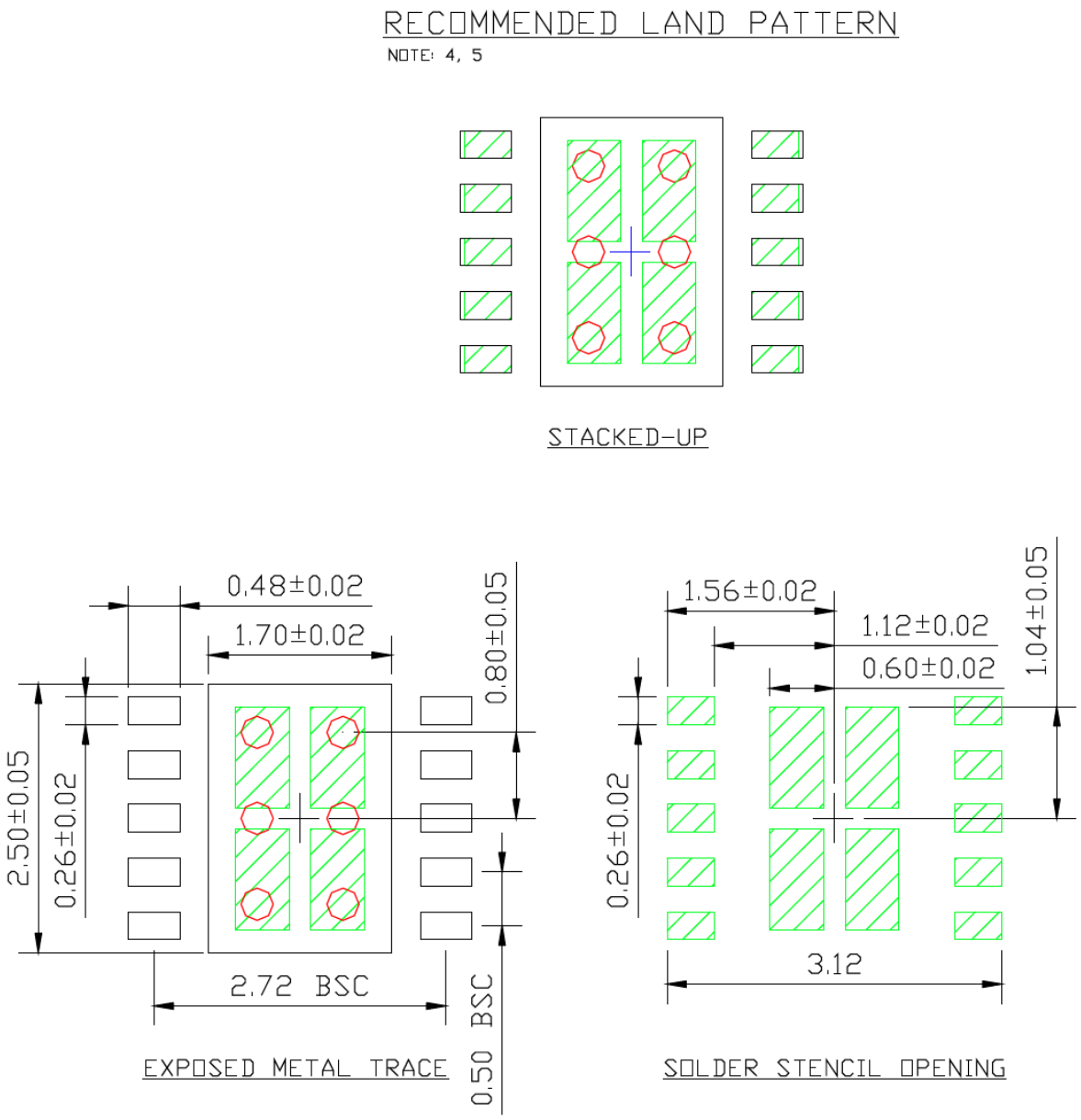


SIDE VIEW
NOTE: 1, 2, 3

NOTE:
1. MAX PACKAGE WARPAGE IS 0.05 MM
2. MAX ALLOWABLE BURR IS 0.076MM IN ALL DIRECTIONS
3. PIN #1 IS ON TOP WILL BE LASER MARKED
4. RED CIRCLE IN LAND PATTERN INDICATE THERMAL VIA. SIZE SHOULD BE 0.30-0.35 MM IN DIAMETER AND SHOULD BE CONNECTED TO GND FOR MAX THERMAL PERFORMANCE
5. GREEN RECTANGLES (SHADED AREA) indicate SOLDER STENCIL OPENING ON EXPOSED PAD AREA. SIZE SHOULD BE 0.50x0.95 MM IN SIZE, 0.20 MM SPACING.

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

POD-Land Pattern drawing #DFN33-10LD-PL-1



Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging.

APPENDIX A: REVISION HISTORY

Revision A (October 2018)

- Converted Micrel document MIC5166 to Microchip data sheet template DS20006085A.
- Minor grammatical text changes throughout.

Revision B (March 2019)

- EN and PG pin names/numbers corrected in Typical Application Circuit and Figure 7-2.
- Updated V_{TT} Accuracy values in the Electrical Characteristics table.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

Device	X	XX	-XX
Part No.	Junction Temp. Range	Package	Media Type

Device:	MIC5166:	3A High-Speed, Low V_{IN} DDR Terminator	
Junction Temperature Range:	Y	=	–40°C to +125°C, RoHS-Compliant
Package:	ML	=	10-Lead 3 mm x 3 mm x 0.9 mm DFN
Media Type:	TR	=	5,000/Reel

Note: DFN is a green, RoHS-compliant package. Lead finish is NiPdAu. Mold compound is Halogen free.

Examples:

a) MIC5166YML-TR: MIC5166, –40°C to +125°C Temperature Range, 10-Lead 3 mm x 3 mm DFN, 5,000/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
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- Microchip is willing to work with the customer who is concerned about the integrity of their code.
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Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

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