ISL99125B, ISL99135B

25A/35A DrMOS Module with Diode Emulation and PS4

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The ISL99125B and ISL99135B are high-performance DrMOS power modules designed for high-frequency power conversion. By combining a high-performance FET driver and MOSFETs in an advanced package, high-density DC/DC converters may be created. Combined with an Intersil PWM controller, a complete voltage regulator solution can be created with reduced external components and minimum overall PCB real estate.

The ISL99125B and ISL99135B feature a three-state PWM input that, working together with Intersil's 5V PWM controllers (such as ISL6398, ISL9585x, ISL637x, ISL633x, ISL636x, and ISL68201), will provide a robust solution in the event of abnormal operating conditions.

The ISL99125B, ISL99135B support high-efficiency operations not only at heavy loads, but also at light loads via its diode emulation capability. Diode emulation can be disabled for those applications where variable frequency operation is not desired at light loads.

ISL99125B, ISL99135B also feature very low shutdown supply current (3µA) to ensure the low power consumption, especially designed for IMVP8 PS4 shutdown operation.

Related Literature

- For a full list of related documents, visit our website
  - ISL99125B and ISL99135B product pages

Features

- V_{IN} range: 0V to 25V
- Current capability: 25A (ISL99125B), 35A (ISL99135B)
- Supports three-state 5.0V PWM input
- 0.5Ω ON-resistance and 4A sink current capability
- Diode emulation for enhanced light-load efficiency
- Ultra low shutdown supply current (3µA) for PS4 operation
- Low three-state hold-off time
- Adaptive shoot-through protection
- Integrated high-side gate-to-source resistor to prevent self turn-on due to high input bus dv/dt
- V_{CC} undervoltage lockout
- Switching frequencies up to 2MHz
- Pb-free (RoHS compliant)
- 3.5x5 QFN 24 Ld package

Applications

- High-efficiency and high-density VRM and VRD
- Core, graphic, and memory regulators for microprocessors
- High-density VR for server, networking, and cloud computing
- POL DC/DC converters and video gaming consoles

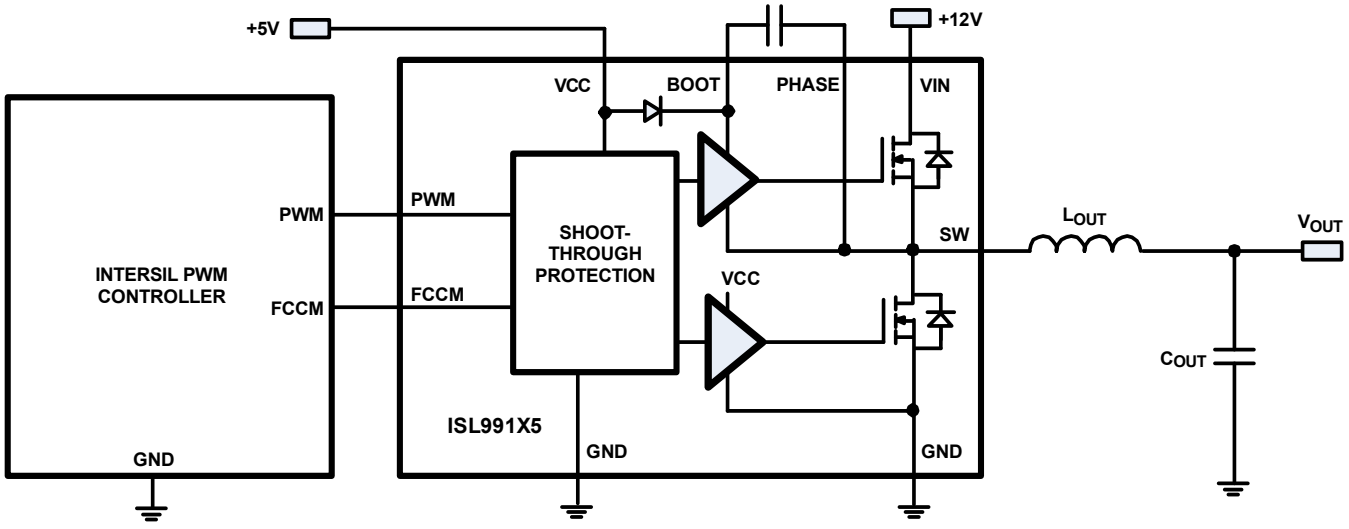


FIGURE 1. SIMPLIFIED APPLICATION BLOCK DIAGRAM

Functional Block Diagram

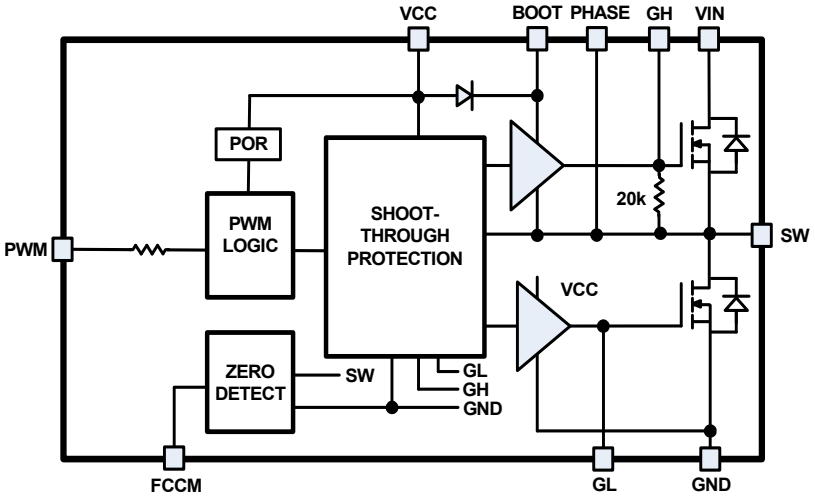


FIGURE 2. FUNCTIONAL BLOCK DIAGRAM

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP RANGE (°C)	CURRENT RATING (A)	PWM INPUT (V)	TAPE AND REEL (UNITS)	PACKAGE (RoHS COMPLIANT)	PKG. DWG. #
ISL99125BDRZ-T	125BDRZ	-40 to +85	25	5.0	3k	24 Ld Exposed Pad 3.5x5 QFN	L24.3.5x5W
ISL99135BDRZ-T	135BDRZ	-40 to +85	35	5.0	3k	24 Ld Exposed Pad 3.5x5 QFN	L24.3.5x5W
ISL68201-99125DEMO1Z	3.3V at 16A design with ISL99125B and the ISL68201 digital hybrid PWM Controller						
ISL68201-99135DEMO1Z	1.0V at 20A design with ISL99135B and the ISL68201 digital hybrid PWM Controller						

NOTES:

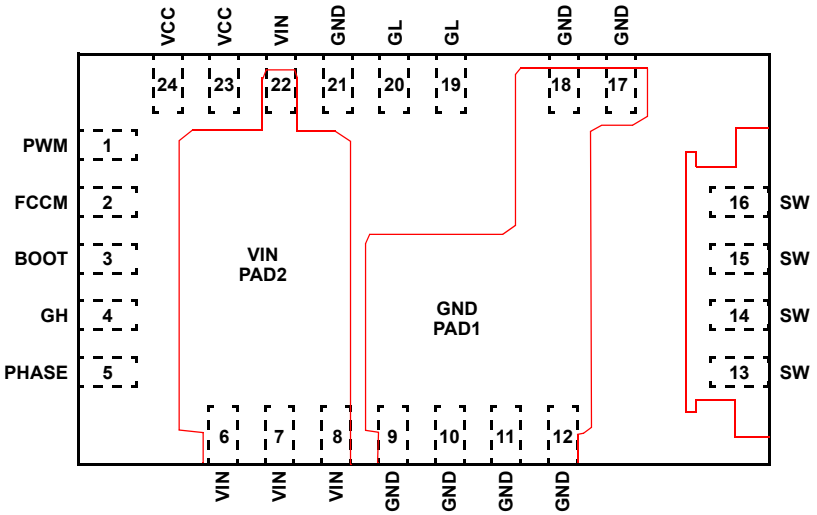
1. Refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), see product information pages for ISL99125B, ISL99135B. For more information on MSL, see tech brief TB363.

TABLE 1. KEY DIFFERENCES BETWEEN FAMILY OF PARTS

PART #	CURRENT RATING (A)	PWM (V)	THERMAL FLAG	OCP FLAG	IMON	TMON	PACKAGE	P2P COMPATIBLE	USED WITH
5.0V PWM POWER STAGE FAMILY									
ISL99125B	25	5.0	No	No	No	No	24 Ld 3.5x5 QFN	ISL99135B	Analog Controllers: ISL633x, ISL636x, ISL637x, ISL95829, ISL9585x Digital Hybrid Controllers: ISL68201, ISL6388/98 Full Digital Controller: ZL8802 Phase Doublers: ISL6617, ISL6617A
ISL99135B	35	5.0	No	No	No	No	24 Ld 3.5x5 QFN	ISL99125B	
ISL99227B	60	5.0	Yes	Yes	Yes	Yes	32 Ld 5x5 PQFN	ISL99226B	
3.3V PWM POWER STAGE FAMILY									
ISL99140	40	3.3	Yes	No	No	No	40 Ld 6x6 QFN	N/A	Full Digital Controllers: ISL68/69xxx, ZL8802 Digital Hybrid Controllers: ISL68201, ISL6388/98 (3.3V PWM Setting)
ISL99227	60	3.3	Yes	Yes	Yes	Yes	32 Ld 5x5 PQFN	ISL99226A	

Pin Configuration

ISL99125B, ISL99135B
(24 LD QFN)
TOP VIEW



Pin Descriptions

PIN #	PIN NAME	DESCRIPTION
1	PWM	PWM input of gate driver. The PWM signal can enter three distinct states during operation. Connect this pin to the PWM output of the controller.
2	FCCM	Input pin to enable or disable diode emulation. When FCCM is LOW, diode emulation is allowed. When FCCM is HIGH, continuous conduction mode is forced. High impedance on the input (floating FCCM) or keeping the pin at mid-level of VCC will shut down the device into ultra-low current mode (5V, 3µA).
3	BOOT	Floating bootstrap supply pin for the upper gate drive. Place a high quality low ESR ceramic capacitor (~0.1µF to 0.22µF/X7R) in close proximity across the BOOT and PHASE pins.
4	GH	High-side gate drive output for monitoring/testing. No circuit connection needed.
5	PHASE	Return of bootstrap capacitor. Internally connected to SW node. External connection is not needed.
6, 7, 8, 22, PAD2	VIN	Input of power stage. Place a couple of high quality, low ESR ceramic capacitors (10µF or higher, X5R or X7R) in close proximity across the VIN and GND planes.
9, 10, 11, 12, 17, 18, 21, PAD1	GND	Power stage and logic bias supply return. Connect directly to system ground plane.
13, 14, 15, 16	SW	Switching junction node between low-side and high-side MOSFETs. Connect directly to output inductor.
19, 20	GL	Low-side gate drive output for monitoring/testing. No circuit connection needed.
23, 24	VCC	+5V driver bias supply. Place a high quality, low ESR ceramic capacitor (~1µF/ X5R~X7R) in close proximity from this pin to system ground plane.

Typical Applications Circuits with ISL68201

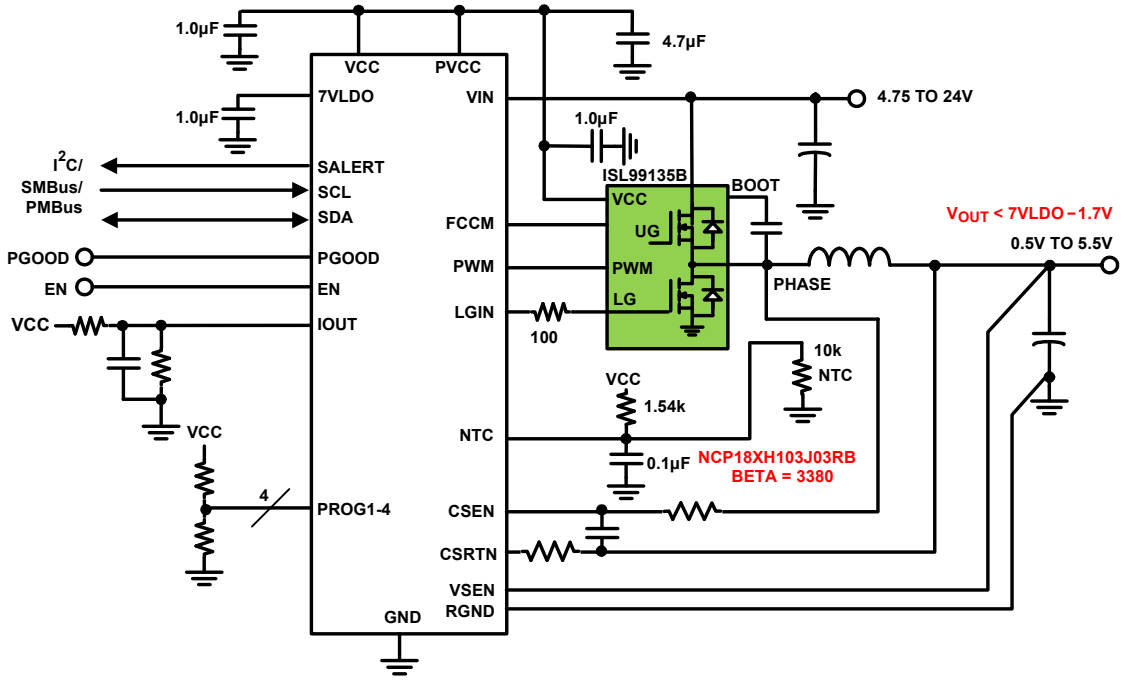


FIGURE 3. WIDE RANGE INPUT AND OUTPUT APPLICATIONS

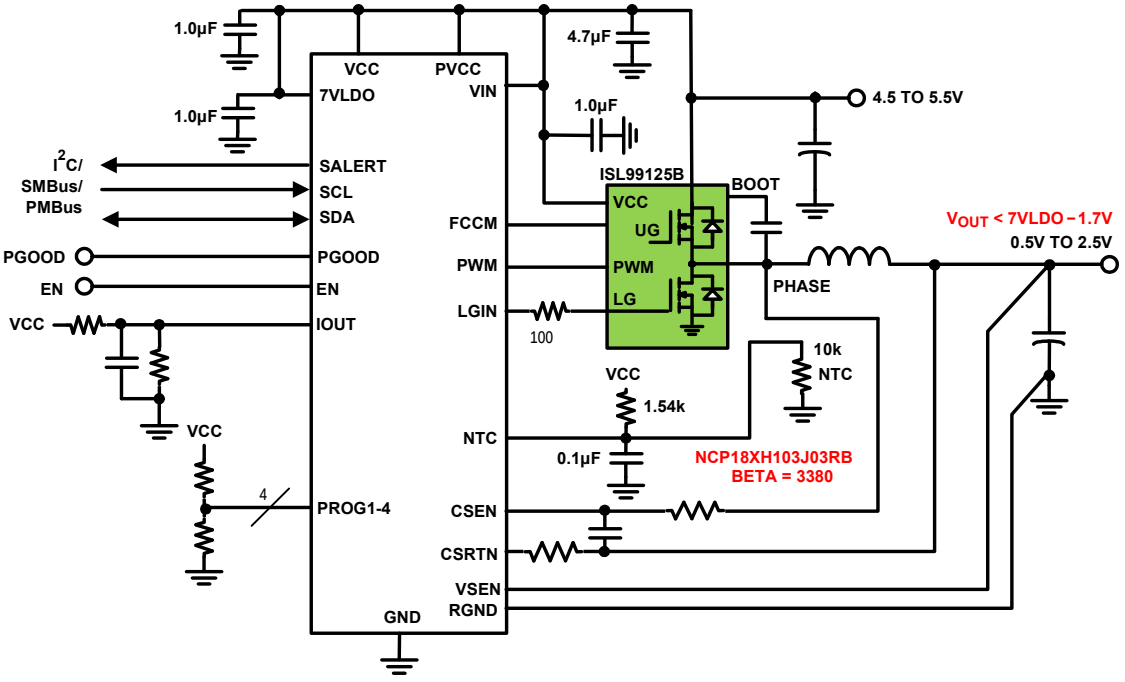


FIGURE 4. 5V INPUT APPLICATION

Typical Application Circuit with ISL95855

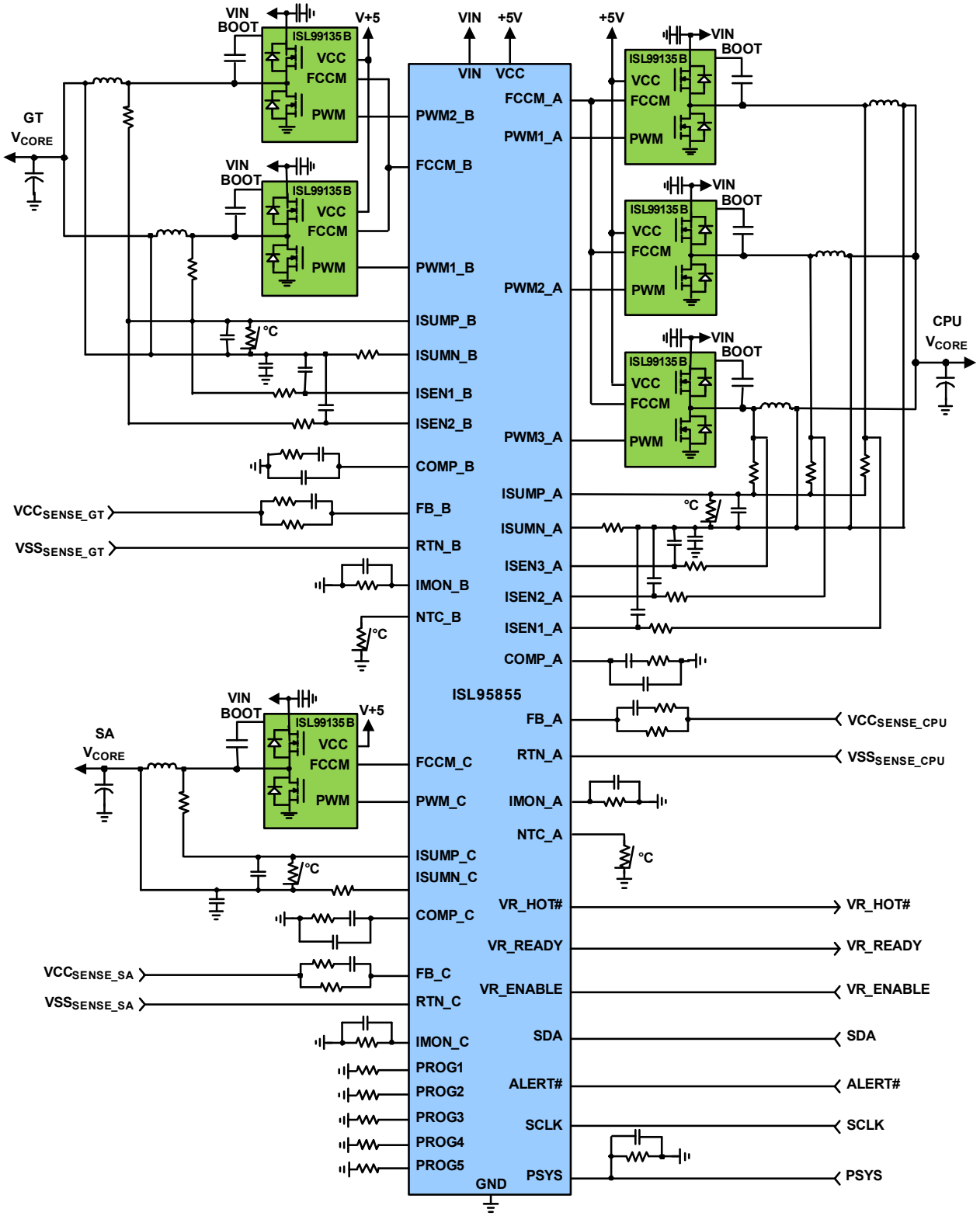


FIGURE 5. TYPICAL APPLICATION CIRCUIT WITH ISL95855

Absolute Maximum Ratings

VIN ..... -0.3V to 30V
Supply Voltage (VCC) ..... -0.3V to 7V
I/O Voltage (V_{PWM}, V_{FCCM}) ..... -0.3V to VCC + 0.3V
BOOT Voltage ($V_{BOOT-GND}$) ..... -0.3V to 33V (DC) or 36V (<20ns)
BOOT to PHASE Voltage ($V_{BOOT-PHASE}$) ..... -0.3V to 7V (DC)
-0.3V to 9V (<10ns)
PHASE Voltage ..... (GND - 0.3V) to 30V
GND - 10V (<20ns Pulse Width, 10µJ)
ESD Rating
Human Body Model (Tested per JESD22-A114F) 2kV
Charged Device Model (Tested per JESD22-C101C) 1kV
Latch-Up (Tested per JESD78C, Class II, Level A) 100mA

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
24 Ld QFN Package (Notes 4, 5)	10	3

Maximum Junction Temperature (Plastic Package) ..... +150°C
Maximum Storage Temperature Range ..... -65°C to +150°C
Pb-Free Reflow Profile ..... see TB493

Recommended Operating Conditions

Ambient Temperature Range ..... -40°C to +85°C
Maximum Operating Junction Temperature ..... +125°C
Supply Voltage, V_{CC}, PVCC ..... 5V ±5%
Input Supply Voltage, V_{IN} ..... 0V to 25V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.

Electrical Specifications

T_A = +25°C; V_{IN} = 12V, V_{CC} = 5V unless otherwise noted. **Boldface limits apply across the recommended operating temperature range, -40°C to +85°C.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
V_{CC} SUPPLY CURRENT						
Standby Bias Supply Current	I_{VCCSD}	PWM and FCCM pin floating		3.3	**4**	µA
		PWM pin floating, V_{FCCM} = 5V		80		µA
		PWM pin floating, V_{FCCM} = 0V		120		µA
ISL99125B Bias Supply Current	I_{VCC}	FCCM = 5V, V_{PWM} = 300kHz, 10% duty cycle		12		mA
ISL99135B Bias Supply Current		FCCM = 5V, V_{PWM} = 300kHz, 10% duty cycle		10		mA
ISL99125B Bias Supply Current		FCCM = 5V, V_{PWM} = 1MHz, 10% duty cycle		40		mA
ISL99135B Bias Supply Current		FCCM = 5V, V_{PWM} = 1MHz, 10% duty cycle		34		mA
POWER-ON RESET AND ENABLE						
POR Rising Threshold	V_{PORR}			3.4	**3.9**	V
POR Falling Threshold	V_{PORF}		**2.3**	2.9		V
POR Hysteresis	V_{PORH}			500		mV
PWM INPUT						
Input Current	I_{PWM}	V_{PWM} = 5V		250		µA
		V_{PWM} = 0V		-250		µA
PWM Rising Threshold	V_{PWMH}	V_{CC} = 5V	**3.5**	3.8	**4.1**	V
PWM Falling Threshold	V_{PWML}	V_{CC} = 5V	**0.7**	1.0	**1.3**	V
Tri-State Shutdown Window		V_{CC} = 5V	**1.3**		**3.5**	V
FCCM INPUT						
Input Current	I_{FCCM}	V_{FCCM} = 5V		50		µA
		V_{FCCM} = 0V		50		µA
FCCM High Rising Threshold		V_{CC} = 5V	**2.8**		**3.6**	V
FCCM Low Falling Threshold		V_{CC} = 5V	**1.4**		**2.2**	V

Electrical Specifications T_A = +25°C; V_{IN} = 12V, V_{VCC} = 5V unless otherwise noted. **Boldface limits apply across the recommended operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 6)	TYP	MAX (Note 6)	UNIT
Tri-State Shutdown Window		V_{VCC} = 5V	**2.2**		**2.8**	V
PS4 Exit Latency	$t_{PS4EXIT}$	V_{VCC} = 5V			**15**	µs
SWITCHING TIME						
GH Turn-On Propagation Delay	t_{PDHU}	V_{VCC} = 5V, see Figure 6 (GL Low to GH High)		20		ns
GH Turn-Off Propagation Delay	t_{PDLU}	V_{VCC} = 5V, see Figure 6 (PWM Low to GH Low)		18		ns
GL Turn-On Propagation Delay	t_{PDHL}	V_{VCC} = 5V, see Figure 6 (GH Low to GL High)		20		ns
GL Turn-Off Propagation Delay	t_{PDLL}	V_{VCC} = 5V, see Figure 6 (PWM High to GL Low)		25		ns
GH/GL Exit Tri-State Propagation Delay	t_{PDTS}	V_{VCC} = 5V, see Figure 6 (tri-state to GH/GL High)		35		ns
PWM Tri-State Shutdown Hold-Off Time	t_{TSSHD}	V_{CC} = 5V	**100**	175	**250**	ns
Minimum GL On-Time in DCM	t_{LGMIN}	V_{VCC} = 5V		350		ns
BOOTSTRAP DIODE						
Forward Voltage		V_{VCC} = 5V, forward bias current = 2mA	**0.43**	0.55	**0.65**	V

NOTES:

6. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.

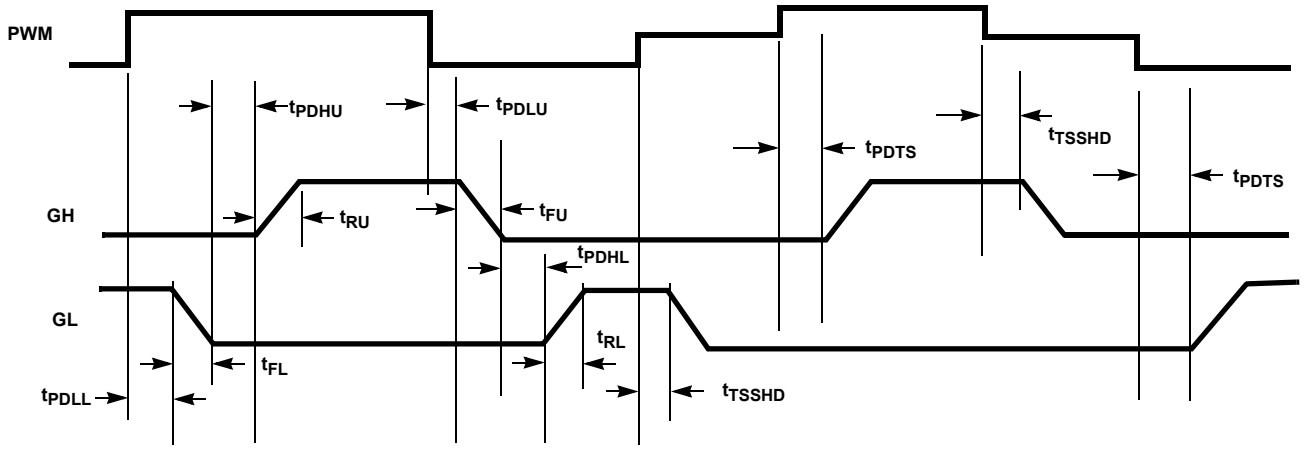


FIGURE 6. TIMING DIAGRAM

TABLE 2. GATE DRIVE TRUTH TABLE

FCCM	PWM	GL	GH
Tri-State	X	L	L
L	L	H (Note 7)	L
L	H	L	H
H	L	H	L
H	H	L	H

NOTE:

7. The LG stays high until inductor current drops to zero.

Typical Performance Characteristics V_{CC} = 5V, T_A = +25°C, unless otherwise noted

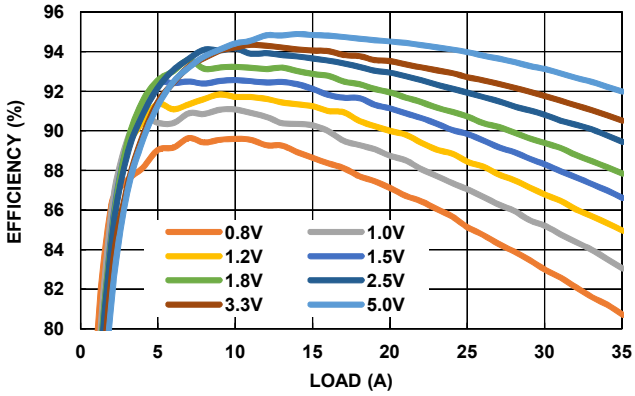


FIGURE 7. V_{OUT} POWER STAGE EFFICIENCY (V_{IN} = 12V; 500kHz; L_{OUT} = 0.18µH/0.17mΩ/FP1008-180-R; INCLUDE INDUCTOR AND ISL99135B LOSSES)

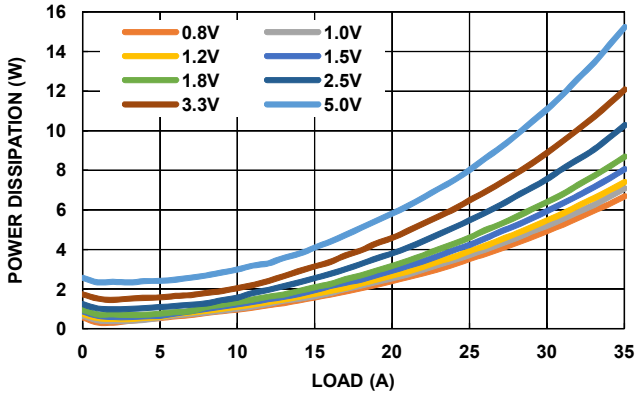


FIGURE 8. V_{OUT} POWER STAGE DISSIPATION (V_{IN} = 12V; 500kHz; L_{OUT} = 0.18µH/0.17mΩ/FP1008-180-R; INCLUDE INDUCTOR AND ISL99135B LOSSES)

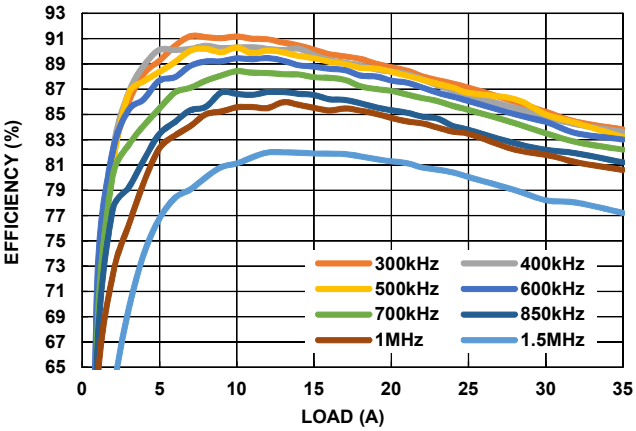


FIGURE 9. V_{OUT} POWER STAGE EFFICIENCY (V_{IN} = 12V; V_{OUT} = 1.0V L_{OUT} = 0.18µH/0.17mΩ/FP1008-180-R; INCLUDE INDUCTOR AND ISL99135B LOSSES)

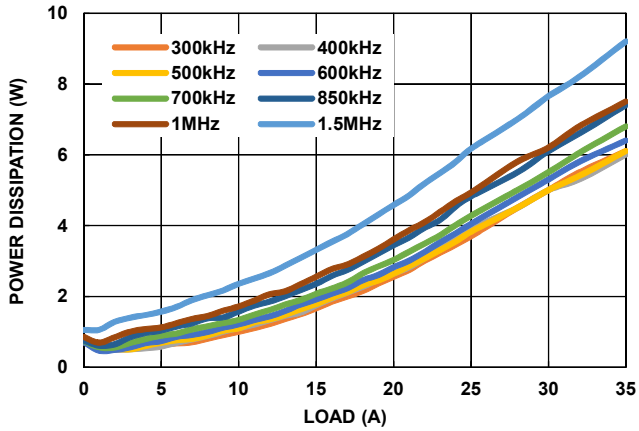


FIGURE 10. V_{OUT} POWER STAGE DISSIPATION (V_{IN} = 12V; V_{OUT} = 1.0V L_{OUT} = 0.18µH/0.17mΩ/FP1008-180-R; INCLUDE INDUCTOR AND ISL99135B LOSSES)

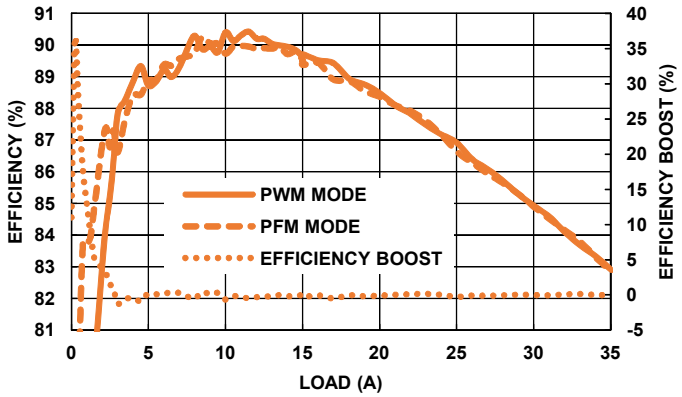


FIGURE 11. EFFICIENCY COMPARISON OF PWM MODE AND PFM ENABLED MODE (V_{IN} = 12V, V_{OUT} = 1.0V, L_{OUT} = 0.18µH/0.17mΩ/FP1008-180-R; INCLUDE INDUCTOR AND ISL99135B LOSSES)

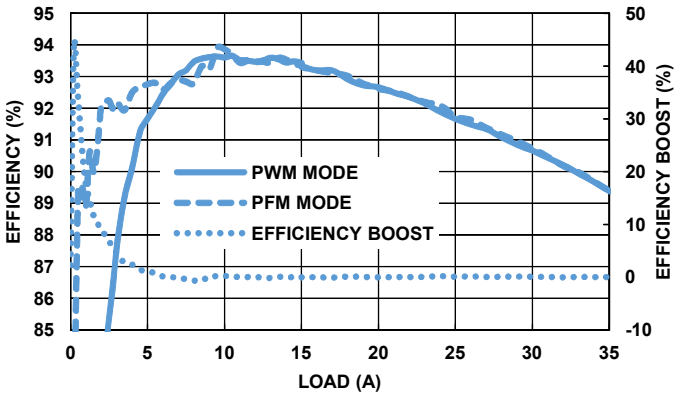


FIGURE 12. EFFICIENCY COMPARISON OF PWM MODE AND PFM ENABLED MODE (V_{IN} = 12V, V_{OUT} = 2.5V, L_{OUT} = 0.18µH/0.17mΩ/FP1008-180-R; INCLUDE INDUCTOR AND ISL99135B LOSSES)

Typical Performance Characteristics V_{CC} = 5V, T_A = +25°C, unless otherwise noted (Continued)

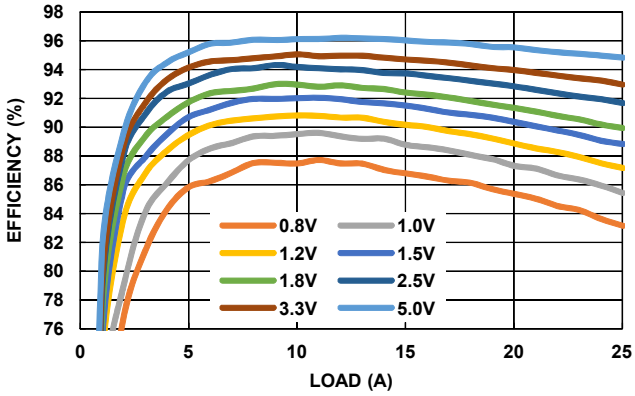


FIGURE 13. POWER STAGE EFFICIENCY (V_{IN} = 12V; 400kHz L_{OUT} = 0.47µH/0.32mΩ/WE 744-301-047; INCLUDE INDUCTOR AND ISL99125B LOSSES)

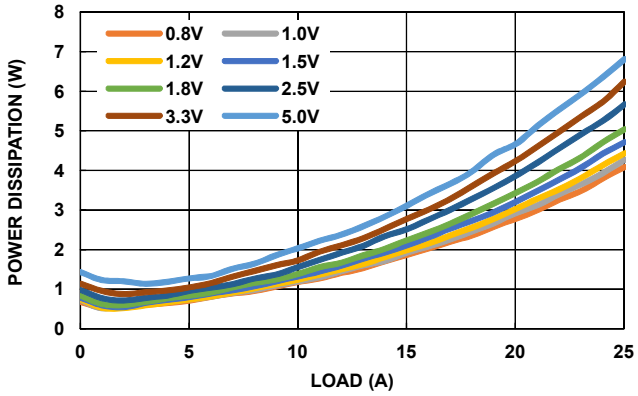


FIGURE 14. POWER STAGE DISSIPATION (V_{IN} = 12V; 400kHz L_{OUT} = 0.47µH/0.32mΩ/WE 744-301-047; INCLUDE INDUCTOR AND ISL99125B LOSSES)

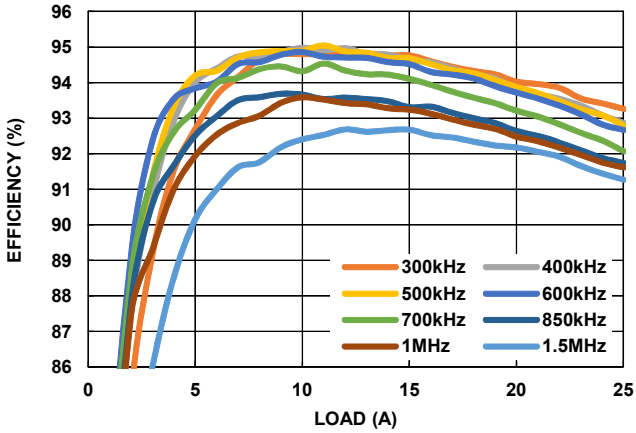


FIGURE 15. POWER STAGE EFFICIENCY (V_{IN} = 12V; V_{OUT} = 3.3V L_{OUT} = 0.47µH/0.32mΩ/WE 744-301-047; INCLUDE INDUCTOR AND ISL99125B LOSSES)

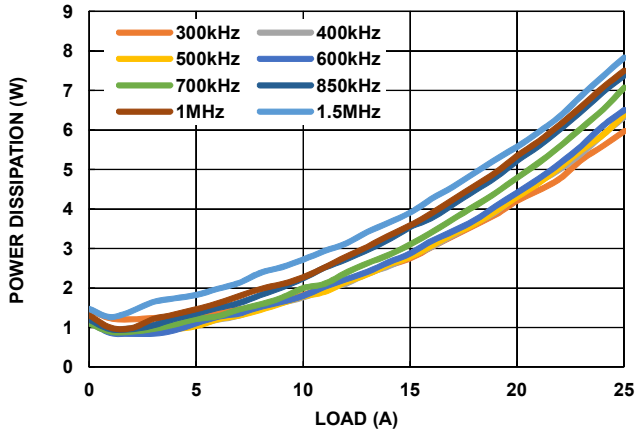


FIGURE 16. POWER STAGE DISSIPATION (V_{IN} = 12V; V_{OUT} = 3.3V L_{OUT} = 0.47µH/0.32mΩ/WE 744-301-047; INCLUDE INDUCTOR AND ISL99125B LOSSES)

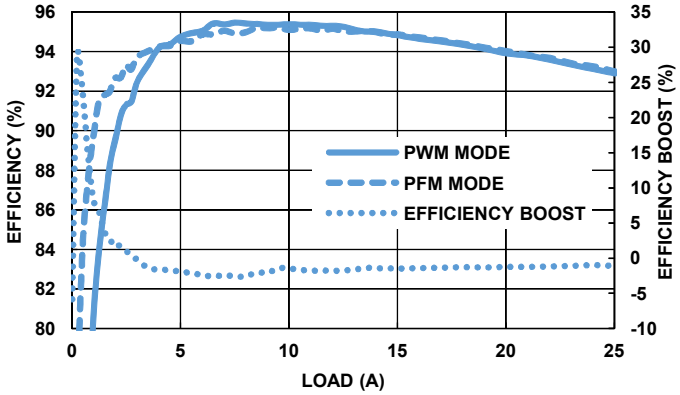


FIGURE 17. EFFICIENCY COMPARISON OF PWM MODE AND PFM ENABLED MODE (V_{IN} = 12V, V_{OUT} = 3.3V, L_{OUT} = 0.47µH/0.32mΩ/WE 744-301-047; INCLUDE INDUCTOR AND ISL99125B LOSSES)

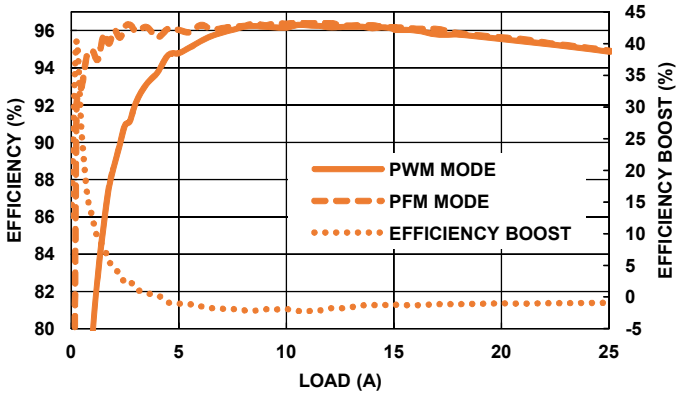


FIGURE 18. EFFICIENCY COMPARISON OF PWM MODE AND PFM ENABLED MODE (V_{IN} = 12V, V_{OUT} = 5.0V, L_{OUT} = 0.47µH/0.32mΩ/WE 744-301-047; INCLUDE INDUCTOR AND ISL99125B LOSSES))

Operation

The ISL99125B, ISL99135B are optimized driver and power stage solutions for high-density synchronous DC/DC power conversion. The ISL99125B and ISL99135B include a high-performance driver, integrated Schottky bootstrap diode, and MOSFET pair optimized for high switching frequency buck voltage regulators. The ISL99125B, ISL99135B include a driver with advanced power management features that allow direct control of the lower MOSFET and diode emulation as well as IMVP8 PS4 shutdown mode.

Power-On Reset (POR)

During initial start-up, the V_{CC} voltage rise is monitored. Once the rising V_{CC} voltage exceeds 3.5V (typically), normal operation of the driver is enabled. If V_{CC} drops below the falling threshold of 2.95V (typically), operation of the driver is disabled.

Shoot-Through Protection

Prior to V_{CC} exceeding its POR level, the undervoltage protection function is activated and both GH and GL are held active low (off). Once the V_{CC} voltage surpasses the Rising Threshold (see "Electrical Specifications" on page 6) the PWM and FCCM signals are used to control both high-side and low-side MOSFETs.

The rising edge on PWM initiates the turn-off of the lower MOSFET. Adaptive shoot-through circuitry monitors the GL voltage and determines a safe time for the upper MOSFET to turn-on. This prevents the MOSFETs from conducting simultaneously.

The falling PWM transition causes the upper FET to turn off and the lower FET to turn on. Adaptive shoot-through circuitry monitors the GH to SW voltage to determine a safe time for the low-side MOSFET turn-on. This prevents the MOSFETs from conducting simultaneously.

Should the driver have no bias voltage applied and be unable to actively hold the MOSFETs off, an integrated 20kΩ resistor from the upper MOSFET gate-to-source will aid in keeping the device in its off state. This can be especially critical in applications where the input voltage rises prior to the ISL99125B and ISL99135B V_{CC} supply.

Tri-State PWM Input

The ISL99125B and ISL99135B supports a tri-level input on the PWM pin. Should the pin be pulled into and remain in the tri-state window for a set hold-off time, the driver will force both MOSFETs to their off states. When the PWM signal moves outside the shutdown window, the driver immediately resumes driving the MOSFETs according to the PWM commands.

This feature is utilized by Intersil PWM controllers as a method of forcing both MOSFETs off. Should the PWM input be left floating, the pin will be pulled into the tri-state window internally and force both MOSFETs to a safe off state. The ISL99125B and ISL99135B's tri-state levels are compatible with 5.0V PWM logic.

FCCM Operation

Diode emulation allows for higher converter efficiency under light load situations. With diode emulation active (FCCM pulled low), the ISL99125B and ISL99135B will detect the zero current crossing of the output inductor and turn off the low-side gate after the minimum LGATE ON-time of 350ns expires. This ensures that Discontinuous Conduction Mode (DCM) is achieved to minimize losses. Diode emulation is asynchronous to the PWM signal. Therefore, the ISL99125B and ISL99135B will respond to the FCCM input immediately after it changes state. This operation is compatible with the ISL95825 VR12.5/12.6 controller for diode emulation operation and the ISL68201 digital hybrid controller for PFM operation, significantly improving light-load efficiency.

Furthermore, compared to conventional drivers with FCCM input, the ISL99125B and ISL99135B enters shutdown operation of both the high-side and low-side MOSFET when the FCCM pin enters its tri-state window. This mode reduces the total bias current to 3µA and significantly reduces the power consumption at standby mode, which is required to support Intel IMVP8 PS4 shutdown operation and compatible with ISL95855, ISL95857, ISL95859, and ISL95829 IMVP8 controllers.

For incompatible controllers without the FCCM output pin such as ISL6398, ISL637x, ISL633x, and ISL636x, the ISL99125B and ISL99135B's FCCM pin should be pulled to V_{CC}.

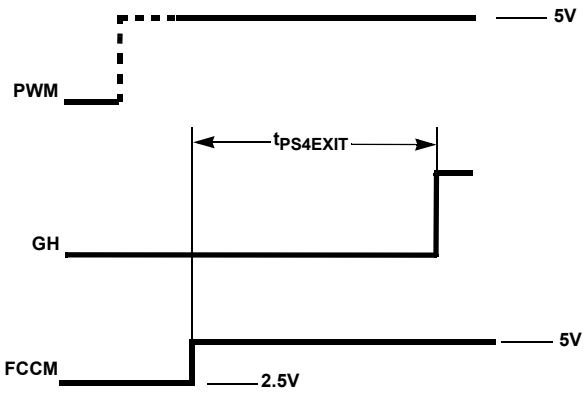


FIGURE 19. PS4 EXIT TIMING DIAGRAM

Bootstrap Function

The ISL99125B and ISL99135B features an internal bootstrap Schottky diode. A high quality ceramic capacitor should be placed in close proximity across BOOT and PHASE pins. The bootstrap capacitor can range between 0.1µF~0.22µF/X5R~X7R for normal buck switching applications.

PCB Layout Considerations

Proper PCB layout will reduce noise coupling to other circuits, improve thermal performance and maximize the efficiency. The following is meant to lead to an optimized layout:

- Place multiple 10µF or greater ceramic capacitors directly at the device between VIN and PGND as indicated in Figure 20. This is the most critical decoupling and reduced parasitic inductance in the power switching loop. This will reduce overall electrical stress on the device as well as reduce coupling to

other circuits. Best practice is to place the decoupling capacitors on the same PCB side as the device.

- Connect GND to the system ground plane with a large via array as close to the GND pins as the design rules allow. This improves thermal and electrical performance.
- Place VCC and BOOT-PHASE decoupling capacitors at the IC pins as shown in Figure 20.
- Note that the SW plane connecting the ISL99125B, ISL99135B, and inductor must carry a full load current and will create resistive loss if not sized properly. However, it is also a very noisy node that should not be oversized or routed close to any sensitive signals. Best practice is to place the inductor as close to the device as possible and thus, minimizing the required area for the SW connection. If one must choose a long route of either the V_{OUT} side of the inductor or the SW side, choose the quiet V_{OUT} side. Best practice is to locate the ISL99125B, ISL99135B as close to the final load as possible and thus avoid noisy or lossy routes to the load.

TABLE 3. AVAILABLE EVALUATION BOARDS

EVALUATION BOARDS	DESCRIPTION	SMBus/ PMBus/I^2C
ISL68201-99125DEM01Z	3.3V at 16A design with ISL99125B and the ISL68201 digital hybrid PWM controller.	Yes
ISL68201-99135DEM01Z	1.0V at 20A design with ISL99135B and the ISL68201 digital hybrid PWM controller.	Yes

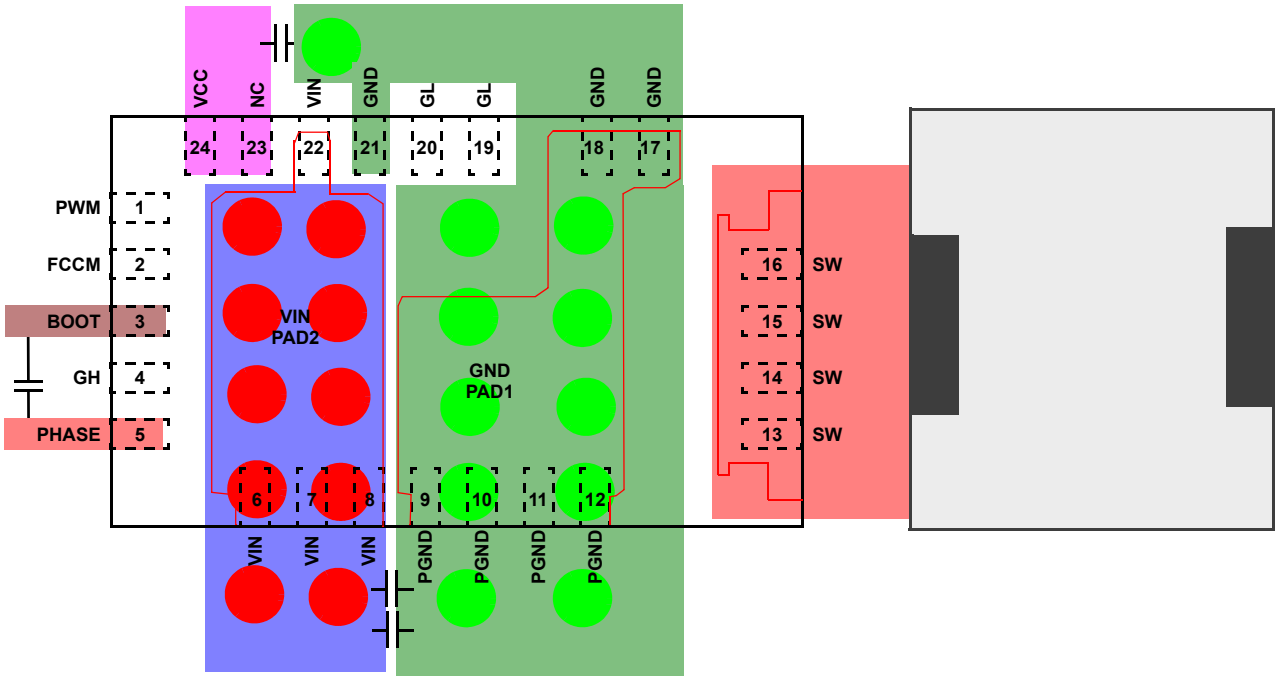


FIGURE 20. PCB LAYOUT FOR MINIMIZING CURRENT LOOPS

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure that you have the latest revision.

DATE	REVISION	CHANGE
January 24, 2017	FN8848.4	Changed temperature range from: -10°C to +85°C to: -40°C to +85°C, in Ordering Information table on page 2 and in Recommended Operating Conditions and Electrical Specifications table on page 6.
January 12, 2017	FN8848.3	Frst bullet in Features on page 1 and in Recommended Operating Conditions on page 6: Changed "4.5V to 25V" to "0V to 25V".
October 14, 2016	FN8848.2	Updated Figure 5 on page 5.
October 3, 2016	FN8848.1	Updated the Related Literature section on page 1. In “Absolute Maximum Ratings” on page 6, updated BOOT Voltage from “-0.3V to 33V” to “-0.3V to 33V (DC) or 36V (20ns)”.
August 26, 2016	FN8848.0	Initial Release

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing, and high-end consumer markets.

For the most updated datasheet, application notes, related documentation, and related parts, please see the respective product information page found at www.intersil.com.

For a listing of definitions and abbreviations of common terms used in our documents, visit: www.intersil.com/glossary.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

Reliability reports are also available from our website at www.intersil.com/support.

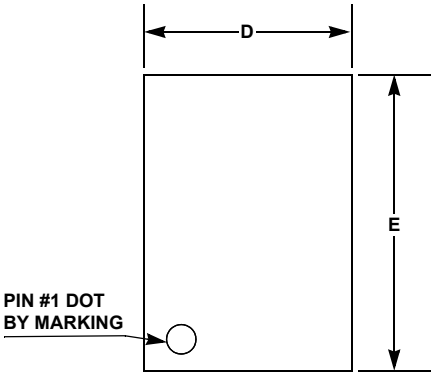
Package Outline Drawing

For the most recent package outline drawing, see L24.3.5x5W.

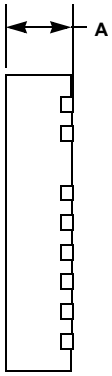
L24.3.5x5W

24 LEAD POWER QUAD FLAT NO-LEAD PLASTIC PACKAGE

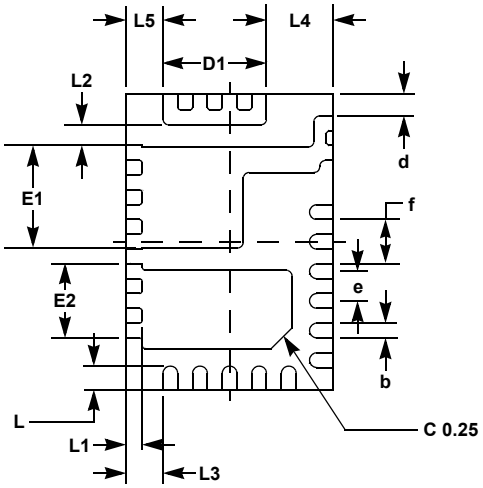
Rev 0, 4/16



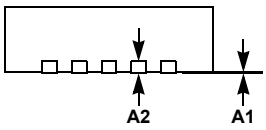
TOP VIEW



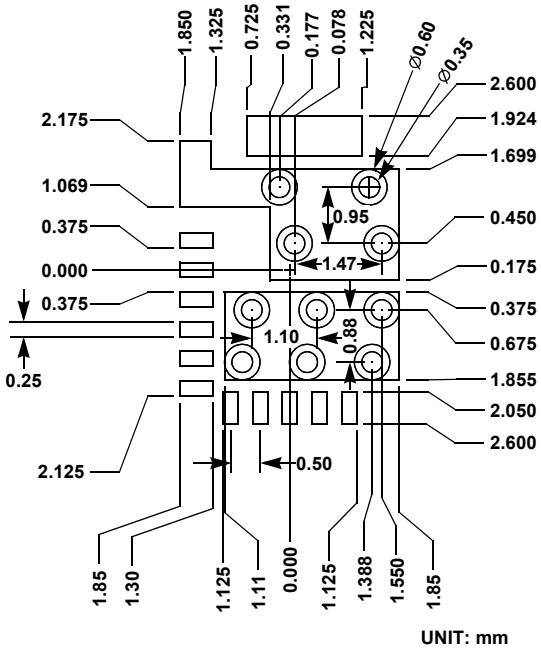
SIDE VIEW



BOTTOM VIEW



SIDE VIEW



UNIT: mm

RECOMMENDED LAND PATTERN

SYMBOLS	MILLIMETER		
	MIN	TYP	MAX
A	1.00	1.10	1.20
A1	0.00	-	0.05
A2		0.20 Ref.	
E	4.90	5.00	5.10
E1	1.63	1.73	1.83
E2	1.15	1.25	1.35
D1	1.65	1.75	1.85
D	3.40	3.50	3.60
L	0.35	0.40	0.45
L1	0.22	0.27	0.32
L2	0.30	0.35	0.40
L3	0.58	0.63	0.68
L4	1.02	1.12	1.22
L5	0.58	0.63	0.68
b	0.20	0.25	0.30
d	0.33	0.38	0.43
f	0.70	0.75	0.80
e		0.50 BSC	

NOTES:

1. Controlling dimension is millimeter.
2. Converted inch dimensions are not necessarily exact.