



PCN Number: SM082119 Chgnot.doc rev 13 1/14

Product/Process	Change Notification (PCN)
Customer: Digi-Key	Date: 08/21/19
Customer Part # and/or Lot# affected:	A4915METTR-T and A4915MLPTR-T
Originator: Scott Mitti	Phone: 508-854-5899
<b>Duration of Change:</b>	Permanent X Temporary (explain)
Summary description of change: Part C	hange: X Other:
Semiconductor LLC (PSL), Bloomington, M to PSL, Allegro will be manufacturing the	METTR-T and A4915MLPTR-T at wafer fab, Polar MN, USA, utilizing 8" ABCD5 technology. In addition A4915METTR-T and A4915MLPTR-T at United shu, Taiwan wafer fab utilizing the 8" ABCD5
What is the part or process changing for	rom (provide details)?

Allegro currently manufactures the A4915METTR-T and A4915MLPTR-T at wafer fab, Polar Semiconductor LLC (PSL), Bloomington, MN, USA, utilizing 8" ABCD5 technology

What is the part or process changing to (describe the anticipated impact of this change on form, fit and/or function)?

In addition to PSL, Allegro will be manufacturing the A4915METTR-T and A4915MLPTR-T at United Microelectronics Corporation (UMC), Hsinshu, Taiwan. afer fab utilizing the 8" ABCD5 technology wafer line.

Note: Validation of equivalence within a specific application is at the discretion of the Customer





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Is a PPAP update required?	Yes	No X
Is reliability testing required? (If Yes, refer to attached plan)	Yes X	No (explain)



## **Reliability Qualification Results**

 Device:
 A4915 (949151)
 Package:
 WLP (eTSSOP)

 Assy Lot #:
 1827831UDAA
 Assembly Location:
 UTAC

 Number of Leads:
 28
 Lead Finish:
 100% Sn

 Fab Location:
 UMC
 Tracking Number:
 4344

Reason for Qualification: A4915 - 3-Phase MOSFET Driver (UMC Transfer)

Reliability Qualification Results						
4915 STR#4344 Requirements						
Stress Test	Abv.	Test #	Test Method	Test Conditions	s.s.	Results
HAST	HAST	A2	JESD22-A110	130°C, 2 ATM, 85% RH, 0, 96 hrs	77	0 Rejects
Electrostatic Discharge Charged Device Model	CDM	E3	JESD22-C101	Test Conditions, Sampling Size are defined in the Test Method		Classification = C3, >1kV
Electrical Distributions	ED	E5	AEC Q100-009	Tri-Temp Electrical Distributions	30 pcs	0 Rejects; Cpk>1.67

Reliability Qualification Results						
4915 STR#4343					Requirements	
Stress Test	Abv.	Test #	Test Method	Test Conditions	s.s.	Results
High Temperature Operating Life	HTOL	B1	JESD22-A108	Ta = 125°C 0, 168 hrs	77	0 Rejects
Electrostatic Discharge Human Body Model	НВМ	E2	JESD22-A114	Test Conditions, Sampling Size ar in the Test Method	e defined	Classification 2, HBM = 2.5kV
Latch-Up	LU	E4	AEC Q100-004	Test Conditions, Sampling Size ar in the Test Method	e defined	Class II, Level A
Electrical Distributions	ED	E5	AEC Q100-009	Tri-Temp Electrical Distributions	30 pcs	0 Rejects; Cpk>1.67





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## **Reliability Qualification Results**

Device: A4915 (949151)
Assy Lot #: 1827722LBAA
Number of Leads: 28
Fab Location: UMC

Package: WET (MLP)
Assembly Location: UTAC
Lead Finish: 100% Sn
Tracking Number: 4343

Reason for Qualification: A4915 - 3-Phase MOSFET Driver

Reliability Qualification Results							
4915 STR#4343						Requirements	
Stress Test	Abv.	Test #	Test Method	Test Conditions	s.s.	Results	
HAST	HAST	A2	JESD22-A110	130°C, 2 ATM, 85% RH, 0, 96 hrs	77	0 Rejects	
High Temperature Operating Life	HTOL	B1	JESD22-A108	Ta = 125°C 0, 168 hrs	77	0 Rejects	
Electrostatic Discharge Human Body Model	НВМ	E2	JESD22-A114	Test Conditions, Sampling Size are defined in the Test Method		Classification 2, HBM = 2.5kV	
Electrostatic Discharge Charged Device Model	CDM	E3	JESD22-C101	Test Conditions, Sampling Size are defined in the Test Method		Classification = C3, >1kV	
Latch-Up	LU	E4	AEC Q100-004	Test Conditions, Sampling Size are defined in the Test Method		Class II, Level A	
Electrical Distributions	ED	E5	AEC Q100-009	Tri-Temp Electrical Distributions	30 pcs	0 Rejects; Cpk>1.67	

Reliability Qualification Results						
4915 STR#4349 Requirements						
Stress Test	Abv.	Test #	Test Method	Test Conditions	s.s.	Results
HAST	HAST	A2	JESD22-A110	130°C, 2 ATM, 85% RH, 0, 96 hrs	77	0 Rejects
Electrostatic Discharge Charged Device Model	CDM	E3	JESD22-C101	Test Conditions, Sampling Size are defined in the Test Method		Classification = C3, >1kV
Electrical Distributions	ED	E5	AEC Q100-009	Tri-Temp Electrical Distributions	30 pcs	0 Rejects; Cpk>1.67

This device qualification is considered to be passing all environmental stress evaluations per the *Allegro MicroSystems*, specification.

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Expected completion date for internal qualification: Complete									
Expected PPAP availability date: N/A									
Target implementation date: June 2020  Estimated date of first shipment: July 2020  Expected sample availability date: Available Upon Request									
							Customer Approval Rec		quired: tion Only
							Allegro's procedure for technical judgment, to or function. However, for each and every app a change on its applicat requests may be made. Account Manager or local consideration so we can re extend the implementation	e product/process change provide notification of sig- as Allegro cannot ensure of lication; the customer reta- tion suitability. If samples via the contact information I Sales contact for any questi- neet our target date for imple in date, this change will be in	r of changes as early as possible. Under notification, Allegro strives, based on its nificant changes that may affect form, fit evaluation of product/process changes ins responsibility to validate the impact of are needed for validation of a change, in provided herein. Please contact your sons. We would kindly request your ementation. Unless both parties agree to applemented as scheduled.
Customer comments/Con	ditions of Acceptance:								
Approved by: cc: Allegro Sales/Marke	Date: ting/Quality	Title:							