



Process Change:

**PCN Number:** 1109 Chgnot.doc rev 10 04/13 - NO

Other:

### **Product/Process Change Notification (PCN)**

Customer: North American and Asi	a Distributors <b>Da</b>	<b>Date:</b> 8/26/13		
Customer Part # and/or Lot# aft Originator: Julie Hurley	<b>fected:</b> A3979SLPTR-T <b>Phone:</b> 508-854-5491	Fax: 508-853-3353		
<b>Duration of Change:</b>	Permanent	Temporary (explain)		

Allegro currently manufactures the A3979SLPTR-T at Polar Semiconductor, LLC, Bloomington, MN, USA Wafer Fab and Unisem, Perak, Ipoh, Malaysia Assembly. The A3979SLPTR-T will be changing to United Microelectronics Corporation (UMC), Hsinshu, Taiwan Wafer Fab and dual Assembly source at and Unisem, Perak, Ipoh, Malaysia and Jiangsu Changjiang Electronics Tech (JCET), Jiangyin, Jiangsu, China

## What is the part or process changing from (provide details)?

- 1. Polar Semiconductor, LLC, Bloomington, MN USA Wafer Fab
- 2. Unisem, Perak, Ipoh, Malaysia Assembly

**Summary description of change:** Part Change x

#### What is the part or process changing to (provide details)?

- 1 United Microelectronics Corporation (UMC), Hsinshu, Taiwan Wafer Fab
- 2. Dual Source Assembly:

Unisem, Perak, Ipoh, Malaysia

or

Jiangsu Changjiang Electronics Tech (JCET), Jiangyin, Jiangsu, China

#### Describe how this change affects the customer:

There is no change to the Form, Fit, or Function of the device.





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Is a PPAP update required?

Yes

Yes

No x

No (explain)

Is reliability testing required?

(If Yes, refer to attached plan)
Per the below plan:
Per JEDEC and AECQ100 standards

Reliability Qualification Plan/Results

 Device:
 7877, (3977)
 Number of Leads:
 28

 Fab Location:
 UMC
 Assembly Location:
 Unisem

 Assy Lot #:
 1246396UAAA
 Lead Finish:
 100% Sn

 Package:
 LP (TSSOP)
 Tracking Number:
 2104

Reason For Qualification: 7877-Microstepping DMOS Driver with Translator

Reliability Qualification Test Plan/Results								
7877 - STR#2104						Requirements		
Stress Test	Abv.	Test #	Test Method	Test Conditions	S.S.	Results		
Preconditioning	PC	A1	JESD22-A113	85°C/60% RH, 168 hrs, Peak Reflow=260°C	260	0 Rejects		
HAST	HAST	A2	JESD22-A110	130°C, 2 ATM, 85% RH, 0, 96 hrs	77	0 Rejects		
Autoclave	AC	А3	JESD22-A102	121°C, 100% RH, 15 PSIG, 0, 96 hrs	77	0 Rejects		
Temperature Cycle	тс	A4	JESD22-A104	-65°C to +150°C, 0, 500 Cycles	77	0 Rejects		
High Temperature Operating Life	HTOL	B1	JESD22-A108	125°C, 0, 1000 hrs	77	0 Rejects		
Early Life Failure Rate	ELFR	B2	AEC-Q100- 008 / JESD22-A108	125°C, 0, 48 hrs	800	0 Rejects		
Wire Bond Pull	WBP	C2	800021			0 Rejects; Cpk>1.33		
Electrostatic Discharge Human Body Model	НВМ	E2	JESD22-A114	Test Conditions, Sampling Size are defined in the Test Method		Classification H2, HBM =2.5 kV		
Electrostatic Discharge Charged Device Model	CDM	E3	JESD22-C101	Test Conditions, Sampling Size are defined in the Test Method		Classification = IV, > 1kV		
Latch-Up	LU	E4	AEC Q100- 004	Test Conditions, Sampling Size are defined in the Test Method		Class II, Level A		
Electrical Distributions	ED	E5	AEC Q100- 009	Tri-Temp Characterization	1 lot	0 Rejects; Cpk>1.67		

This device qualification is considered to be passing all environmental stress evaluations per the  $Allegro\ MicroSystems,\ Inc.\ 900019$  specification.





Expected completion date for internal qualification: Complete

Expected PPAP availability date: N/A

Target implementation date: 11/1/2013

Estimated date of first shipment: 1/1/2014

Expected sample availability date: Available Now

**Customer Approval Required:** 

No X For Notification Only

cc: Allegro Sales/Marketing/Quality