SCLS601B – DECEMBER 2004 – REVISED AUGUST 2012

HIGH-SPEED CMOS LOGIC 16-CHANNEL ANALOG MULTIPLEXER and DEMULTIPLEXER

Check for Samples: CD74HCT4067-Q1

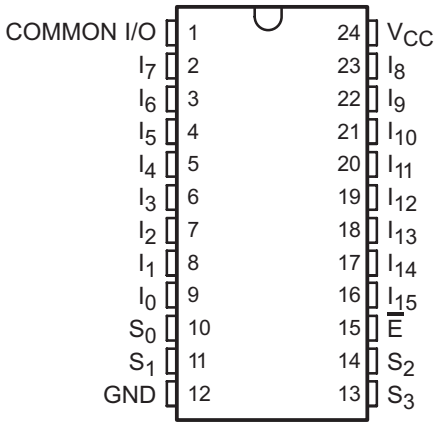
1 FEATURES

- Qualified for Automotive Applications
- AEC-Q100 Test Guidance With the Following Results:
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level H1A
  - Device CDM ESD Classification Level C2
- Wide Analog Input Voltage Range
- Low ON Resistance
  - 70 Ω Typical (V_{CC} = 4.5 V)
- Fast Switching and Propagation Speeds
- Break-Before-Make Switching
  - 6 ns Typical (V_{CC} = 4.5 V)
- Fanout (Over Temperature Range)
  - Standard Outputs: 10 LSTTL Loads
  - Bus Driver Outputs: 15 LSTTL Loads
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- 4.5-V to 5.5-V Operation
- Direct LSTTL Input Logic Compatibility: V_{IL} = 0.8 V Max, V_{IH} = 2 V Min
- CMOS Input Compatibility: $I_I \leq 1$ µA at V_{OL}, V_{OH}

2 APPLICATIONS

- Automotive
- Analog Switch
- Analog Multiplexer and Demultiplexer

M PACKAGE
(TOP VIEW)



3 DESCRIPTION

The CD74HCT4067-Q1 device is a digitally controlled analog switch that utilizes silicon-gate CMOS technology to achieve operating speeds similar to LSTTL, with the low power consumption of standard CMOS integrated circuits.

This analog multiplexer and demultiplexer controls analog voltages that may vary across the voltage supply range. It is a bidirectional switch, thus allowing any analog input to be used as an output and vice-versa. The switch has low (on) resistance and low (off) leakages. In addition, the device has an enable control that, when high, disables all switches to their off state.

ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER(3)	TOP-SIDE MARKING
–40°C to 125°C	DW-SOIC-M	Reel of 2000	CD74HCT4067QM96Q1	HCT4067I

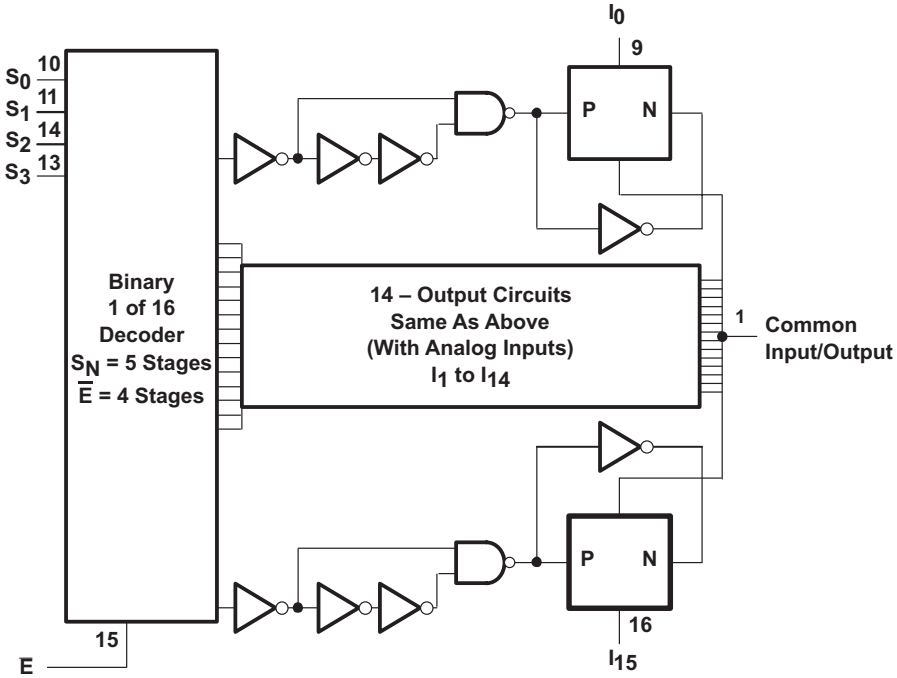
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(3) The suffix 96 denotes tape and reel.

Table 1. FUNCTION TABLE(1)

S0	S1	S2	S3	$\overline{E}$	SELECTED CHANNEL
X	X	X	X	H	None
L	L	L	L	L	0
H	L	L	L	L	1
L	H	L	L	L	2
H	H	L	L	L	3
L	L	H	L	L	4
H	L	H	L	L	5
L	H	H	L	L	6
H	H	H	L	L	7
L	L	L	H	L	8
H	L	L	H	L	9
L	H	L	H	L	10
H	H	L	H	L	11
L	L	H	H	L	12
H	L	H	H	L	13
L	H	H	H	L	14
H	H	H	H	L	15

(1) H = High level
L = Low level
X = Don't care

Logic Diagram (Positive Logic)



3.1 ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE		UNIT
		MIN	MAX	
V_{CC}	Supply voltage range(2)	−0.5	7	V
I_{IK}	Input clamp current (V_I < −0.5 V or V_I > V_{CC} + 0.5 V)		±20	mA
I_{OK}	Output clamp current (V_O < −0.5 V or V_O > V_{CC} + 0.5 V)		±20	mA
I_O	Switch current (V_O > −0.5 V or V_O < V_{CC} + 0.5 V)		±25	mA
I_O	Output source or sink current per output pin (V_O > −0.5 V or V_O < V_{CC} + 0.5 V)		±25	mA
	Continuous current through V_{CC} or GND		±50	mA
T_J	Maximum junction temperature		150	°C
T_{stg}	Storage temperature range	−65	150	°C
ESD Rating	Human Body Model (HBM) AEC-Q100 classification level H1A		400	V
	Charged Device Model (CDM) AEC-Q100 classification level C2		250	V
	Latch-up per JESD78D	Class 1		

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are referenced to GND, unless otherwise specified.

3.2 THERMAL INFORMATION

THERMAL METRIC(1)		CD74HCT4067-Q1	UNIT
		DW (24 PINS)	
θ_{JA}	Junction-to-ambient thermal resistance	62.3	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	30.5	
θ_{JB}	Junction-to-board thermal resistance	31.8	
ψ_{JT}	Junction-to-top characterization parameter	7.7	
ψ_{JB}	Junction-to-board characterization parameter	31.5	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	N/A	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

3.3 RECOMMENDED OPERATING CONDITIONS(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		4.5	5.5	V
V_{IH}	High-level input voltage		2		V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 4.5 V	0	500	ns
T_A	Operating free-air temperature		–40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

3.4 ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_I	V_{CC}	T_A = 25°C			T_A = −40°C to 125°C		UNIT
					MIN	TYP	MAX	MIN	MAX	
I_I	Logic input		V_{CC} or GND	5.5 V			±0.1		±1	µA
I_{IZ}	V_{IS} = V_{CC} or GND, $\overline{E}$ = V_{CC}			5.5 V			±0.8		±8	µA
r_{on}	I_O = 1 mA	V_{IS} = V_{CC} or GND	V_{CC} or GND	4.5 V		70	160		200	Ω
		V_{IS} = V_{CC} to GND	V_{CC} to GND	4.5 V		90	180		225	
Δr_{on}	Between any two switches			4.5 V		10				Ω
I_{CC}			V_{CC} or GND	5.5 V			8		80	µA
ΔI_{CC}	Per input pin: 1 unit load(1)		V_{CC} − 2.1 V	4.5 V to 5.5 V		100	360		450	µA
C_I	Control inputs						10		10	pF

(1) For dual-supply systems, theoretical worst-case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

3.5 HCT INPUT LOADING

INPUT	UNIT LOADS(1)
S_0 – S_3	0.5
$\overline{E}$	0.3

(1) Unit load is ΔI_{CC} limit specified in the electrical characteristics table, for example, 360 µA max at 25°C.

3.6 SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted) see Figure 5

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V_{CC}	T_A = 25°C			T_A = −40°C TO 125°C		UNIT
					MIN	TYP	MAX	MIN	MAX	
t_{pd}	I_n	Common I/O	C_L = 15 pF	5 V		6				ns
			C_L = 50 pF	4.5 V			15		19	
t_{en}	$\overline{E}$	Common I/O	C_L = 15 pF	5 V		25				ns
			C_L = 50 pF	4.5 V			60		75	
t_{en}	S_n	Common I/O	C_L = 15 pF	5 V		25				ns
			C_L = 50 pF	4.5 V			60		75	
t_{dis}	$\overline{E}$	Common I/O	C_L = 15 pF	5 V		23				ns
			C_L = 50 pF	4.5 V			55		69	
t_{dis}	S_n	Common I/O	C_L = 15 pF	5 V		21				ns
			C_L = 50 pF	4.5 V			58		73	

3.7 OPERATING CHARACTERISTICS

V_{CC} = 5 V, T_A = 25°C, input t_r, t_f = 6 ns

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{pd}	Power dissipation capacitance(1)			96		pF

(1) C_{pd} is used to determine the dynamic power consumption (P_D), per package.
$P_D = (C_{pd} \times V_{CC}^2 \times f_I) + \Sigma (C_L + C_S) \times V_{CC}^2 \times f_O$
f_O = output frequency
f_I = input frequency
C_L = output load capacitance
C_S = switch capacitance
V_{CC} = supply voltage

3.8 ANALOG CHANNEL CHARACTERISTICS

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
f_{max}	Switch frequency response bandwidth at −3 dB	See Figure 1 and Figure 7 (1) (2)	4.5 V	89	MHz
	Sine-wave distortion	See Figure 2	4.5 V	0.051	%
	Switch OFF signal feedthrough	See Figure 4 and Figure 8	4.5 V	−75	dB
C_S	Switch input capacitance			5	pF
C_{COM}	Common capacitance			50	pF

(1) Adjust input voltage to obtain 0 dBm at output, f = 1 MHz.
(2) V_{IS} is centered at V_{CC} / 2

4 PARAMETER MEASUREMENT INFORMATION

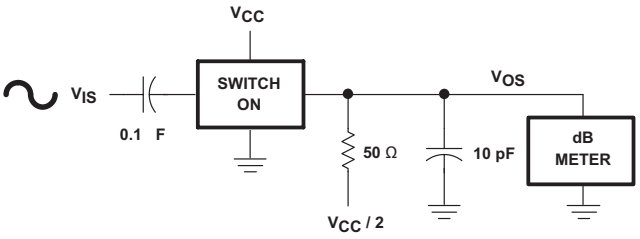


Figure 1. Frequency-Response Test Circuit

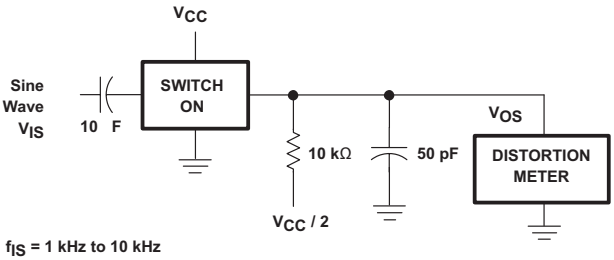


Figure 2. Sine-Wave Distortion Test Circuit

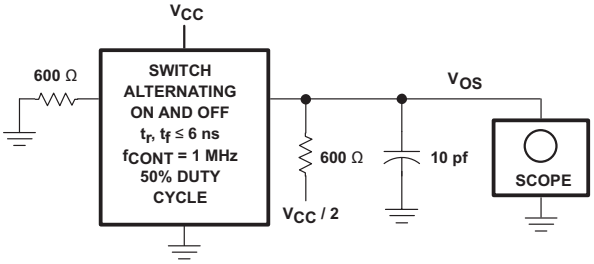


Figure 3. Control-to-Switch Feedthrough Noise Test Circuit

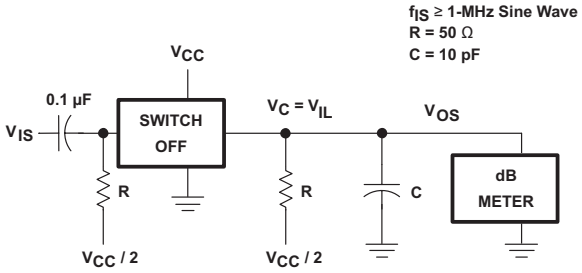
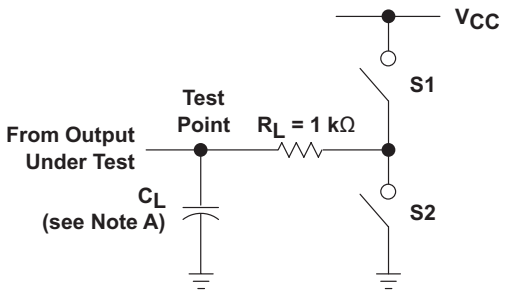


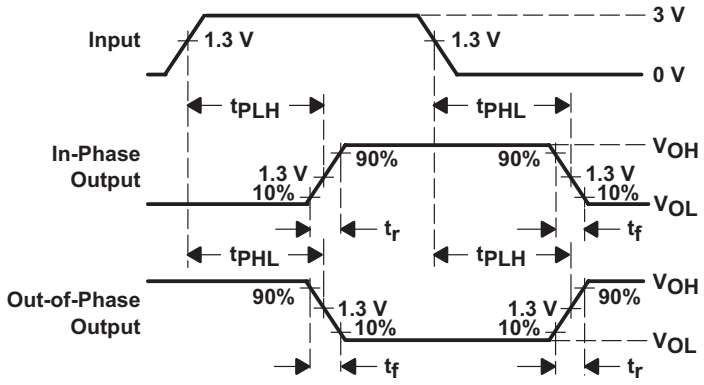
Figure 4. Switch OFF Signal Feedthrough Test Circuit

PARAMETER MEASUREMENT INFORMATION (continued)

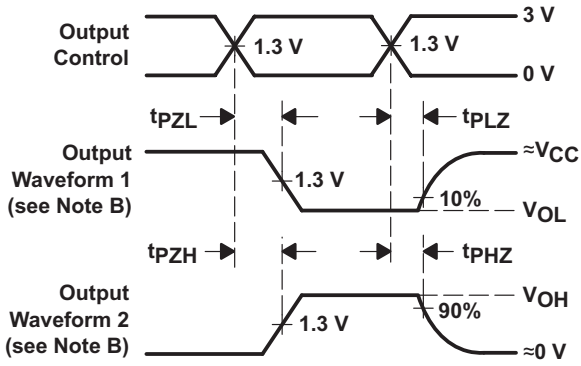


LOAD CIRCUIT

PARAMETER		S1	S2
t_{en}	t_{PZH}	Open	Closed
	t_{PZL}	Closed	Open
t_{dis}	t_{PHZ}	Open	Closed
	t_{PLZ}	Closed	Open
t_{pd}		Open	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORMS
OUTPUT ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. For clock inputs, f_{max} is measured with the input duty cycle at 50%.
E. The outputs are measured one at a time, with one input transition per measurement.
F. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
G. t_{PZL} and t_{PZH} are the same as t_{en}.
H. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 5. Load Circuit and Voltage Waveforms

5 TYPICAL CHARACTERISTICS

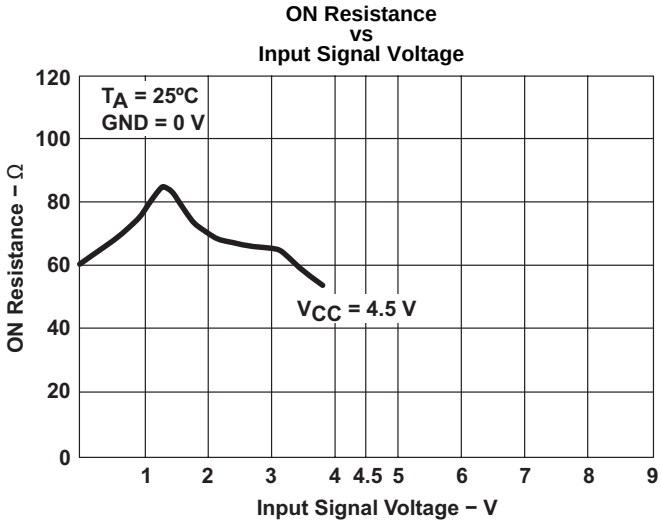


Figure 6.

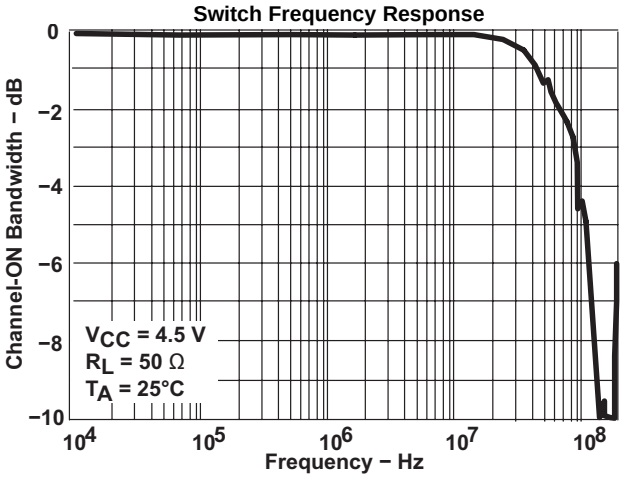


Figure 7.

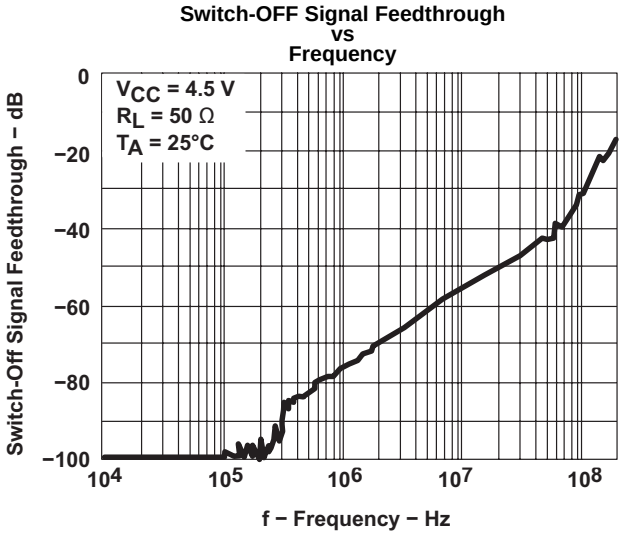


Figure 8.

6 REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (April, 2008) to Revision B	Page
• Changed H2 to H1A and C3B to C2 throughout document	1
• Added AEC-Q100 info to Features	1
• Removed from Features: Wide Operating Temperature Range: –40°C to 85°C	1
• Added applications	1
• Replaced SOIC-M package info in ordering info table with new row for DW-SOIC-M package	1
• Added ESD ratings to Abs Max table	3
• Added latch-up row in Abs Max table	3
• Changed max T_A value from 85°C to 125°C	3
• Changed T_A = -40°C to 85°C column to T_A = -40°C to 125°C	4
• Changed T_A = -40°C to 85°C column to T_A = -40°C to 125°C	4

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD74HCT4067QM96Q1	ACTIVE	SOIC	DW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCT4067I	Samples
D24067IM96G4Q1	ACTIVE	SOIC	DW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HCT4067I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF CD74HCT4067-Q1 :

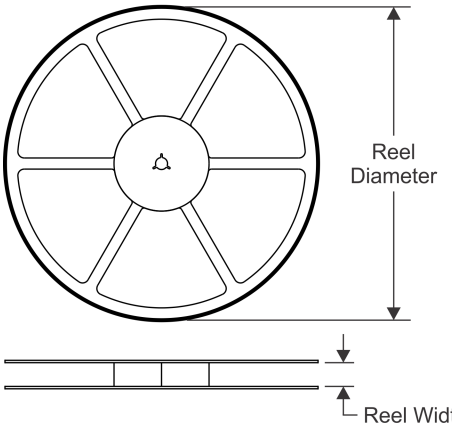
- Catalog: CD74HCT4067

NOTE: Qualified Version Definitions:

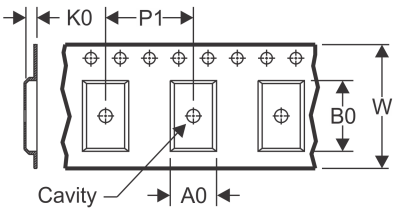
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

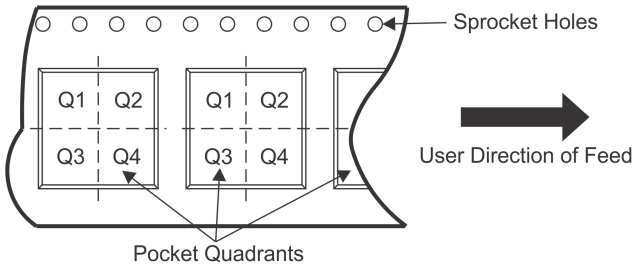


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

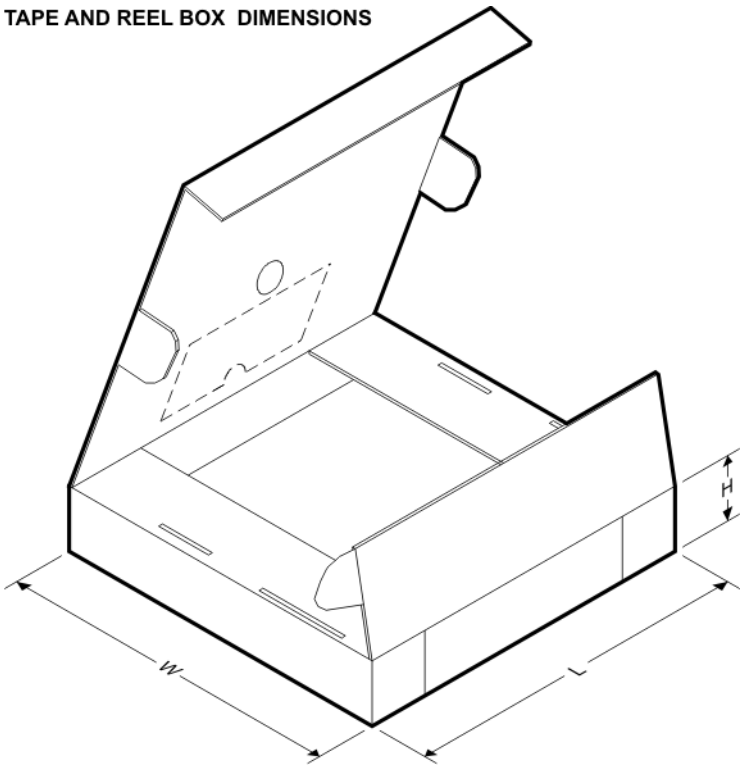
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HCT4067QM96Q1	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1

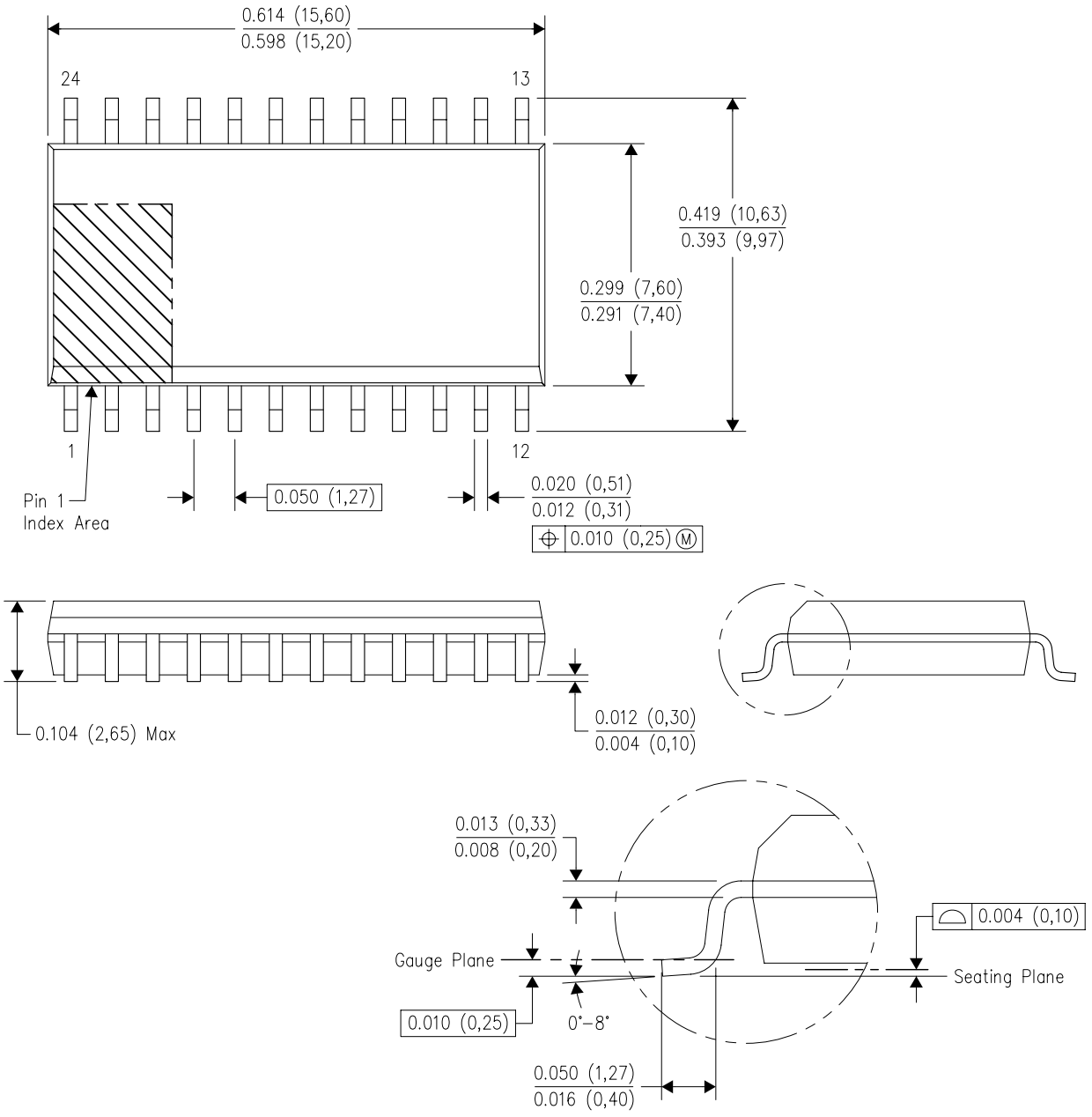
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HCT4067QM96Q1	SOIC	DW	24	2000	350.0	350.0	43.0

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AD.

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