

3.3 V 12.288 MHz Audio Oversampling Clock Generator for USB Applications

NB3N3010B

Description

The NB3N3010B is a precision, low noise clock multiplier that generates an output frequency of 12.288 MHz. This is accomplished by using Frequency-Locked-Loop (FLL) techniques where a 4 kHz reference input is multiplied by 3072, or an 8 kHz input by 1536. The frequency multiplier is selected by the S0 pin.

The two LVCMOS output drivers are disabled to a logic Low with the ENABLEn pin set HIGH. The NB3N3010B operates from a single +3.3 V supply, and is available in the SOIC-8 pin package. The operating temperature range is from 0°C to +85°C.

The NB3N3010B device provides the optimum combination of low cost, flexibility, and high performance. This makes it ideal for applications such as oversampling A-to-D and D-to-A converters from a low reference frequency, such as a USB start-of-frame (SOF) pulse.

Features

- Accepts 8 kHz or 4 kHz Reference Input Derived from USB Start-of-Frame
- Generates 12.288 MHz Frequency-Locked to the Reference
- Fully Integrated Frequency-Lock-Loop with Internal Loop Filter
- Low Skew Dual LVCMOS Outputs
- Very Low Phase Noise Preserves Codec Noise Floor
- Internal Voltage Regulator
- Supply Voltage Required: +3.3 V $\pm 5\%$
- Temperature Range: 0°C to +85°C
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant



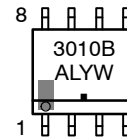
ON Semiconductor®

www.onsemi.com



SOIC-8
D SUFFIX
CASE 751

MARKING DIAGRAM*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note [AND8002/D](#).

ORDERING INFORMATION

Device	Package	Shipping†
NB3N3010BDR2G	SOIC-8 (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

NB3N3010B

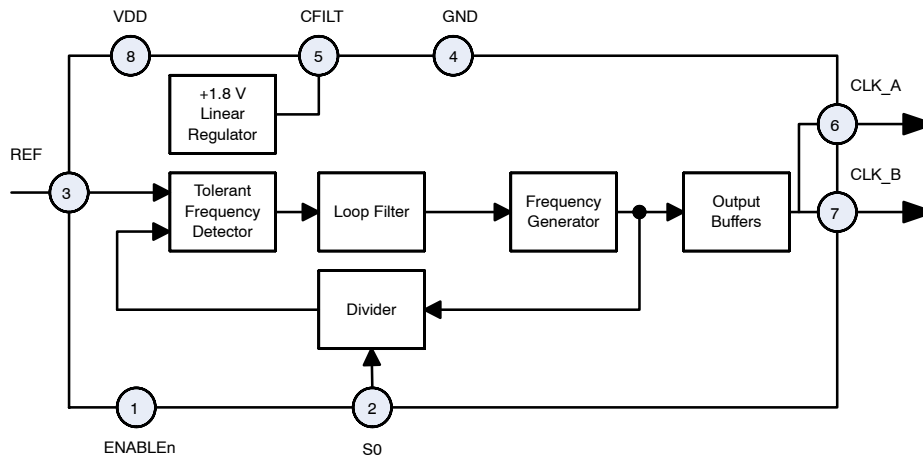


Figure 1. NB3N3010B Simplified Diagram

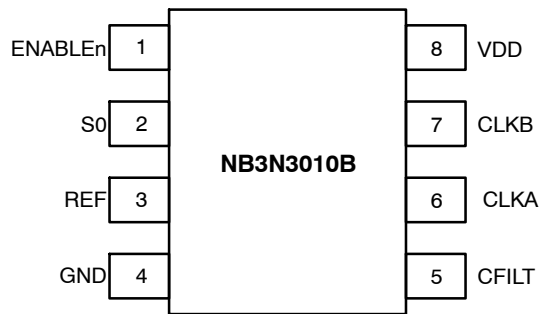


Figure 2. Pinout SOIC-8 (Top View)

Table 1. PIN DESCRIPTION

Pin	Symbol	I/O	Description
1	ENABLEn	LVTTTL/ LVCMOS Input	Low active Output Enable; Defaults HIGH when left open; Internal pull-up resistor to V _{DD} .
2	S0	LVTTTL/ LVCMOS Input	Frequency Select Input. See input frequency select Table 2 for details. Defaults HIGH when left open. Internal pull-up resistor to V _{DD} .
3	REF	Input	Reference Clock input
4	GND	Power Supply	Negative Supply Voltage; Ground 0 V. This pin provides GND return path to the V _{DD} supply.
5	CFILT	Analog	Connection for external filter capacitor for internal +1.8 V regulator; see Figure 4.
6	CLKA	LVCMOS Output	Clock output, copy A (12.288 MHz)
7	CLKB	LVCMOS Output	Clock output, copy B (12.288 MHz)
8	VDD	Power Supply	Positive Supply Voltage, +3.3 V ±5%

NB3N3010B

Table 2. ATTRIBUTES

Characteristic	Value
ESD Protection Human Body Model Machine Model	> 4 kV 400 V
R _{PU} – ENABLE _n Input Pull-up Resistor R _{PU} – SO Input Pull-up Resistor	48 kΩ 48 kΩ
Moisture Sensitivity (Note 1) Pb-Free	Level 1
Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
Transistor Count	12039
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note [AND8003/D](#).

Table 3. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V _{DD}	Positive Power Supply	GND = 0 V		4.6	V
V _I	Input Voltage (VIN)	GND = 0 V		-0.3 V to V _{DD} + 0.3 V	V
T _A	Operating Temperature Range			0 to +85	°C
T _{stg}	Storage Temperature Range			-40 to +150	°C
θ _{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	SOIC-8 SOIC-8	190 130	°C/W °C/W
θ _{JC}	Thermal Resistance (Junction-to-Case)	(Note 2)	SOIC-8	41 to 44	°C/W
T _{sol}	Wave Solder Pb-Free			265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. JEDEC standard multilayer board – 2S2P (2 signal, 2 power).

Table 4. DC CHARACTERISTICS V_{DD} = 3.3 V ±5%, GND = 0 V, T_A = 0°C to +85°C, Note 3.

Symbol	Characteristic	Min	Typ	Max	Unit
V _{DD}	Power Supply Voltage	3.13	3.3	3.47	V
I _{DDOEL}	Power Supply Current (operating, i.e. ENABLE _n is LOW) Outputs Unloaded		21	35	mA
I _{DDOEH}	Power Supply Current (standby, i.e. ENABLE _n is HIGH)		415	600	µA
V _{IH}	Input HIGH Voltage (REF, ENABLE _n , S0)	2.0		V _{DD} + 0.3	V
V _{IL}	Input LOW Voltage (REF, ENABLE _n , S0)	GND – 0.3		0.8	V
V _{OH}	Output HIGH Voltage (CLKA, CLKB), I _{OH} = -12 mA	2.4			V
V _{OL}	Output LOW Voltage (CLKA, CLKB), I _{OL} = 12 mA			0.4	V

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

3. C_{FILT} capacitor must be installed; see Figure 4.

NB3N3010B

Table 5. AC CHARACTERISTICS $V_{DD} = 3.3\text{ V} \pm 5\%$, $GND = 0\text{ V}$, $T_A = 0^\circ\text{C}$ to $+85^\circ\text{C}$ (Note 4)

Symbol	Characteristic	Min	Typ	Max	Unit
f_{out}	Output Clock Frequency: CLKA & CLKB $f_{OUT} = 8\text{ kHz} \times 1536$ $S0 = 1$ $f_{OUT} = 4\text{ kHz} \times 3072$ $S0 = 0$	12.25728 12.25728	12.288 12.288	12.31872 12.31872	MHz
f_{REF}	Reference Input Frequency $S0 = 1$ $S0 = 0$	7.98 3.99	8 4	8.02 4.01	kHz
$t_{jit(per)-ref}$	Reference Input Period Jitter (pk-pk)			250	ns
t_{REFH}	Reference Input Pulse Width (high) $S0 = 1$ $S0 = 0$	33 33		68000 136000	ns
t_{CLKH}	CLKA, CLKB output width, high	13			ns
t_{CLKL}	CLKA, CLKB output width, low	13			ns
t_r	CLKA, CLKB rise time 10% – 90%			4	ns
t_f	CLKA, CLKB fall time 90% – 10%			4	ns
$t_{jit(per)}$	CLKA, CLKB period jitter (over 10k cycles) peak-to-peak RMS			250 20	ps
$t_{jit(cc)}$	CLK_A, CLKB cycle-to-cycle jitter (1k cycles) peak-to-peak RMS			300 35	ps
$t_{sk(LH)}$	CLKA to CLKB output skew (low-to-high transitions)			700	ps
$t_{sk(HL)}$	CLKA to CLKB output skew (high-to-low transitions)			700	ps
	Power Valid to ENABLEn			10	ms
	ENABLEn to CLKA/CLKB		50	100	ms

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm.

4. Outputs loaded with 15 pF max to ground. C_{FILT} capacitor must be installed; see Figure 4.
5. Maximum time required after power is applied to the MCLK FLL until it is ready to accept ENABLEn active.

NB3N3010B

APPLICATION INFORMATION

Figure 1 shows the simplified block diagram of the NB3N3010B device.

The primary function of the NB3N3010B is to accept a selectable 4 kHz or 8 kHz input reference clock, REF, and then multiply it to 12.288 MHz output frequency.

Frequency Select – S0

Either of two expected input REF frequencies, 4 kHz or 8 kHz, will be multiplied by the FLL to achieve 12.288 MHz at the low-skew CLKA and CLKB outputs by selecting the S0 pin; see Table 6.

The pulse high time (T_{HI}) of the input reference signal may vary widely depending on the application. See AC specifications for details.

Output Enable – ENABLEn

A Low active output enable input pin, ENABLEn, is provided. When the ENABLEn input is High inactive, both clock outputs are driven to a logic Low.

The NB3N3010B implements a delay, specified as ENABLEn to Output Delay in the AC Specifications, from the assertion of ENABLEn to the first rising edges on the clock outputs. This delay insures that CLKA and CLKB output pulses are within specification before the output drivers are enabled. When ENABLEn transitions from Low to High (de-asserts), the current cycle of the clock outputs completes normally then the outputs will be held Low. The ENABLEn signal is asynchronous to either the REF input or CLK_x outputs.

Table 6. INPUT FREQUENCY SELECT AND OUTPUT ENABLE FUNCTIONS

ENABLEn*	S0*	f _{REF}	FLL Multiplier	CLKA & CLKB Frequency
0	L	4 kHz	3072	12.288 MHz
0	H	8 kHz	1536	12.288 MHz
1	x	x	x	Disabled Low

*Defaults High when left open.

Typical Power On Sequence

1. Power On
2. Reference Clock present; must be switching before ENABLEn goes High.
3. Output Enable, ENABLEn, High-to-Low

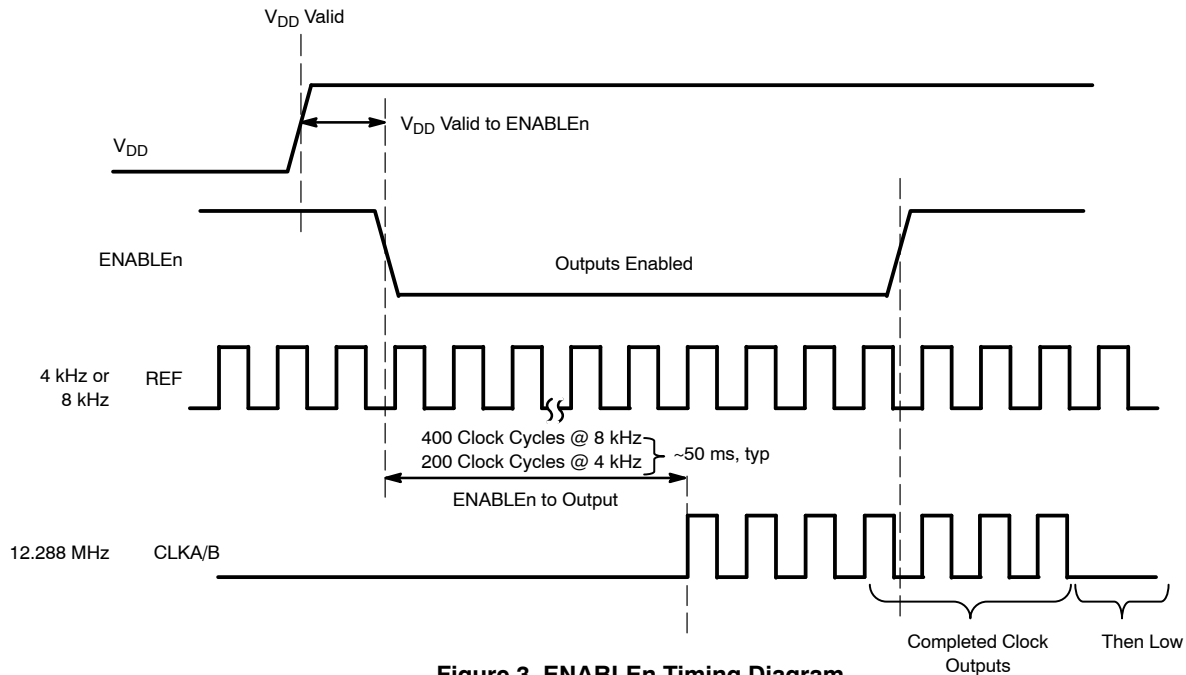


Figure 3. ENABLEn Timing Diagram

CFILT for 1.8 V Regulator

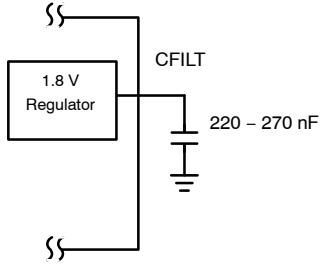


Figure 4. CFILT Capacitor

A low noise 1.8 V LDO/Regulator is integrated to provide a clean supply for the CLKA/CLKB output buffers. The LDO requires a decoupling capacitor in the range of 220 nF to 270 nF for compensation and high frequency PSR, and should be located near the device. The purpose of this design technique is to isolate the high switching noise of the digital outputs from the relatively sensitive internal analog phase-locked loop.

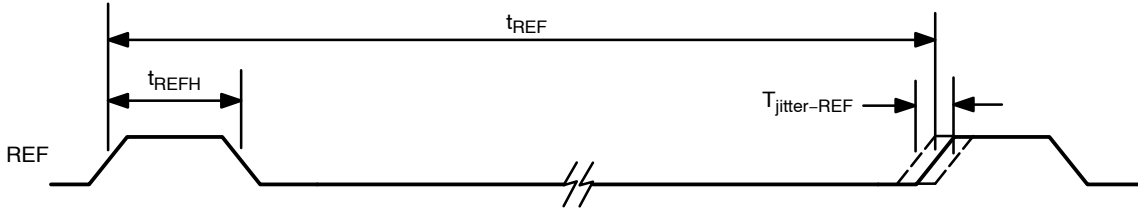


Figure 5. REF Input Timing Diagram

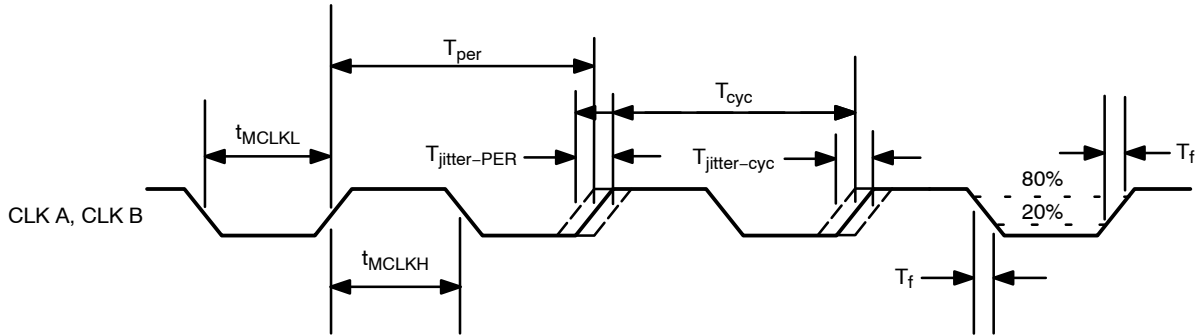


Figure 6. Clock Output Timing Diagram

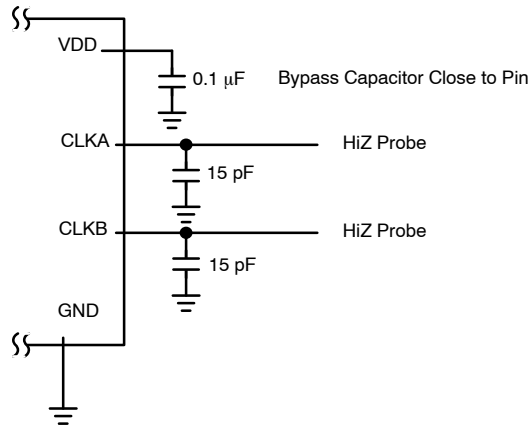


Figure 7. Test Circuit

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1

SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	98ASB42564B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC-8 NB	PAGE 1 OF 2

onsemi and ONsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011

- | | | | |
|---|--|--|--|
| <p>STYLE 1:
 PIN 1. EMITTER
 2. COLLECTOR
 3. COLLECTOR
 4. EMITTER
 5. EMITTER
 6. BASE
 7. BASE
 8. EMITTER</p> | <p>STYLE 2:
 PIN 1. COLLECTOR, DIE, #1
 2. COLLECTOR, #1
 3. COLLECTOR, #2
 4. COLLECTOR, #2
 5. BASE, #2
 6. EMITTER, #2
 7. BASE, #1
 8. EMITTER, #1</p> | <p>STYLE 3:
 PIN 1. DRAIN, DIE #1
 2. DRAIN, #1
 3. DRAIN, #2
 4. DRAIN, #2
 5. GATE, #2
 6. SOURCE, #2
 7. GATE, #1
 8. SOURCE, #1</p> | <p>STYLE 4:
 PIN 1. ANODE
 2. ANODE
 3. ANODE
 4. ANODE
 5. ANODE
 6. ANODE
 7. ANODE
 8. COMMON CATHODE</p> |
| <p>STYLE 5:
 PIN 1. DRAIN
 2. DRAIN
 3. DRAIN
 4. DRAIN
 5. GATE
 6. GATE
 7. SOURCE
 8. SOURCE</p> | <p>STYLE 6:
 PIN 1. SOURCE
 2. DRAIN
 3. DRAIN
 4. SOURCE
 5. SOURCE
 6. GATE
 7. GATE
 8. SOURCE</p> | <p>STYLE 7:
 PIN 1. INPUT
 2. EXTERNAL BYPASS
 3. THIRD STAGE SOURCE
 4. GROUND
 5. DRAIN
 6. GATE 3
 7. SECOND STAGE Vd
 8. FIRST STAGE Vd</p> | <p>STYLE 8:
 PIN 1. COLLECTOR, DIE #1
 2. BASE, #1
 3. BASE, #2
 4. COLLECTOR, #2
 5. COLLECTOR, #2
 6. EMITTER, #2
 7. EMITTER, #1
 8. COLLECTOR, #1</p> |
| <p>STYLE 9:
 PIN 1. EMITTER, COMMON
 2. COLLECTOR, DIE #1
 3. COLLECTOR, DIE #2
 4. EMITTER, COMMON
 5. EMITTER, COMMON
 6. BASE, DIE #2
 7. BASE, DIE #1
 8. EMITTER, COMMON</p> | <p>STYLE 10:
 PIN 1. GROUND
 2. BIAS 1
 3. OUTPUT
 4. GROUND
 5. GROUND
 6. BIAS 2
 7. INPUT
 8. GROUND</p> | <p>STYLE 11:
 PIN 1. SOURCE 1
 2. GATE 1
 3. SOURCE 2
 4. GATE 2
 5. DRAIN 2
 6. DRAIN 2
 7. DRAIN 1
 8. DRAIN 1</p> | <p>STYLE 12:
 PIN 1. SOURCE
 2. SOURCE
 3. SOURCE
 4. GATE
 5. DRAIN
 6. DRAIN
 7. DRAIN
 8. DRAIN</p> |
| <p>STYLE 13:
 PIN 1. N.C.
 2. SOURCE
 3. SOURCE
 4. GATE
 5. DRAIN
 6. DRAIN
 7. DRAIN
 8. DRAIN</p> | <p>STYLE 14:
 PIN 1. N-SOURCE
 2. N-GATE
 3. P-SOURCE
 4. P-GATE
 5. P-DRAIN
 6. P-DRAIN
 7. N-DRAIN
 8. N-DRAIN</p> | <p>STYLE 15:
 PIN 1. ANODE 1
 2. ANODE 1
 3. ANODE 1
 4. ANODE 1
 5. CATHODE, COMMON
 6. CATHODE, COMMON
 7. CATHODE, COMMON
 8. CATHODE, COMMON</p> | <p>STYLE 16:
 PIN 1. EMITTER, DIE #1
 2. BASE, DIE #1
 3. EMITTER, DIE #2
 4. BASE, DIE #2
 5. COLLECTOR, DIE #2
 6. COLLECTOR, DIE #2
 7. COLLECTOR, DIE #1
 8. COLLECTOR, DIE #1</p> |
| <p>STYLE 17:
 PIN 1. VCC
 2. V2OUT
 3. V1OUT
 4. TXE
 5. RXE
 6. VEE
 7. GND
 8. ACC</p> | <p>STYLE 18:
 PIN 1. ANODE
 2. ANODE
 3. SOURCE
 4. GATE
 5. DRAIN
 6. DRAIN
 7. CATHODE
 8. CATHODE</p> | <p>STYLE 19:
 PIN 1. SOURCE 1
 2. GATE 1
 3. SOURCE 2
 4. GATE 2
 5. DRAIN 2
 6. MIRROR 2
 7. DRAIN 1
 8. MIRROR 1</p> | <p>STYLE 20:
 PIN 1. SOURCE (N)
 2. GATE (N)
 3. SOURCE (P)
 4. GATE (P)
 5. DRAIN
 6. DRAIN
 7. DRAIN
 8. DRAIN</p> |
| <p>STYLE 21:
 PIN 1. CATHODE 1
 2. CATHODE 2
 3. CATHODE 3
 4. CATHODE 4
 5. CATHODE 5
 6. COMMON ANODE
 7. COMMON ANODE
 8. CATHODE 6</p> | <p>STYLE 22:
 PIN 1. I/O LINE 1
 2. COMMON CATHODE/VCC
 3. COMMON CATHODE/VCC
 4. I/O LINE 3
 5. COMMON ANODE/GND
 6. I/O LINE 4
 7. I/O LINE 5
 8. COMMON ANODE/GND</p> | <p>STYLE 23:
 PIN 1. LINE 1 IN
 2. COMMON ANODE/GND
 3. COMMON ANODE/GND
 4. LINE 2 IN
 5. LINE 2 OUT
 6. COMMON ANODE/GND
 7. COMMON ANODE/GND
 8. LINE 1 OUT</p> | <p>STYLE 24:
 PIN 1. BASE
 2. EMITTER
 3. COLLECTOR/ANODE
 4. COLLECTOR/ANODE
 5. CATHODE
 6. CATHODE
 7. COLLECTOR/ANODE
 8. COLLECTOR/ANODE</p> |
| <p>STYLE 25:
 PIN 1. VIN
 2. N/C
 3. REXT
 4. GND
 5. IOUT
 6. IOUT
 7. IOUT
 8. IOUT</p> | <p>STYLE 26:
 PIN 1. GND
 2. dv/dt
 3. ENABLE
 4. ILIMIT
 5. SOURCE
 6. SOURCE
 7. SOURCE
 8. VCC</p> | <p>STYLE 27:
 PIN 1. ILIMIT
 2. OVLO
 3. UVLO
 4. INPUT+
 5. SOURCE
 6. SOURCE
 7. SOURCE
 8. DRAIN</p> | <p>STYLE 28:
 PIN 1. SW_TO_GND
 2. DASIC_OFF
 3. DASIC_SW_DET
 4. GND
 5. V_MON
 6. VBULK
 7. VBULK
 8. VIN</p> |
| <p>STYLE 29:
 PIN 1. BASE, DIE #1
 2. EMITTER, #1
 3. BASE, #2
 4. EMITTER, #2
 5. COLLECTOR, #2
 6. COLLECTOR, #2
 7. COLLECTOR, #1
 8. COLLECTOR, #1</p> | <p>STYLE 30:
 PIN 1. DRAIN 1
 2. DRAIN 1
 3. GATE 2
 4. SOURCE 2
 5. SOURCE 1/DRAIN 2
 6. SOURCE 1/DRAIN 2
 7. SOURCE 1/DRAIN 2
 8. GATE 1</p> | | |

DOCUMENT NUMBER:	98ASB42564B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC-8 NB	PAGE 2 OF 2

onsemi and **ONSEMI** are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Email Requests to: orderlit@onsemi.com

onsemi Website: www.onsemi.com

TECHNICAL SUPPORT

North American Technical Support:
Voice Mail: 1 800-282-9855 Toll Free USA/Canada
Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:

Phone: 00421 33 790 2910

For additional information, please contact your local Sales Representative