LM6511 180 ns 3V Comparator

Check for Samples: LM6511

FEATURES

- **(Typical Unless Otherwise Noted)**
- **Operates at +2.7V, +3V, +3.3V, +5V**
- **Low Power Consumption <9.45 mW @ V⁺ = 2.7V (max)**
- **Fast Response Time of 180 ns**

APPLICATIONS

- **Portable Equipment**
- **Cellular Phones**
- **Digital Level Shifting**

DESCRIPTION

The LM6511 voltage comparator is ideal for analog-digital interface circuitry when only a +3V or +3.3V supply is available. The open-collector output permits signal compatibility with a wide variety of digital families: +5V CMOS, +3V CMOS, TTL and so on. Supply voltage may range from 2.7V to 36V between supply voltage leads. The LM6511 operates with little power consumption (P_{diss} < 9.45 mW at V^+ = +2.7V and V^- = 0V).

This voltage comparator offers many features that are available in traditional sub-microsecond comparators: output sync strobe, inputs and output may be isolated from system ground, and wire-ORing. Also, the LM6511 uses the industry-standard, single comparator pinout configuration.

Connection Diagram
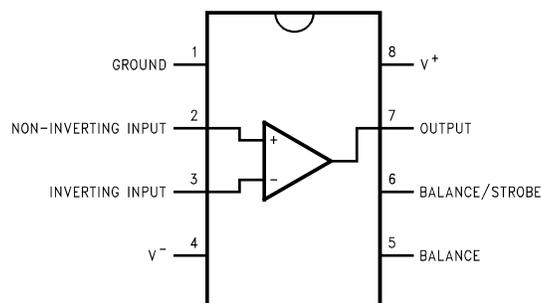
Figure 1. 8-Pin SOIC
See Package Number D

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.
All trademarks are the property of their respective owners.

Absolute Maximum Ratings[(1)(2)]

Supply Voltage		−0.3 to +36V
Output to Negative Supply Voltage		50V
Ground to Negative Supply Voltage		30V
Differential Input Voltage		±30V
Input Voltage		See[(1)]
Storage Temperature Range		−65°C to +150°C
Soldering Information:	SOIC Package (Vapor Phase in 60 sec)	215°C
	SOIC Package (Infrared in 15 sec)	220°C
Power Dissipation		500 mW
Output Short Circuit Duration		10s
Junction Temperature		150°C
ESD Rating (C = +100 pF, R = 1.5 kΩ)		300V

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating ratings indicate conditions the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

Operating Ratings[(1)]

Supply Voltage		2.5V to 30V
Temperature Range		−40°C ≤ T_J ≤ +85°C
Thermal Resistance (θ_{JA})	SOIC Package	170°C/W

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating ratings indicate conditions the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

DC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. **Boldface** limits apply at the temperature extremes. V^+ = 2.7V, V^- = 0V, 50Ω ≤ R_L ≤ 50kΩ, and I_L = 1.0 mA unless otherwise specified

Symbol	Parameter	Conditions	Typical	LM6511I Limit	Units (Limits)
V_{OS}	Offset Voltage	R_S ≤ 50 kΩ[(1)]	1.5	5	mV
				8	max
I_B	Input Bias Current		38	130	nA
				200	max
I_{OS}	Input Offset Current	R_S ≤ 50 kΩ[(1)]	1.5	20	nA
				50	max
I_S	Positive Supply Current		2.7	3.5	mA max
				5	
	Negative Supply Current		1.5	2.0	
				2.5	
V_{SAT}	Saturation Voltage	V_{IN} ≤ 10 mV I_{SINK} = 8 mA	0.23	0.4	V
				0.4	max
A_V	Large Signal Voltage Gain	ΔV_{OUT} = 2V	40		V/mV
CMRR	Common Mode Rejection Ratio		72		dB
I_{STROBE}	Strobe ON Current	See[(2)]	2.0	5.0	mA max

(1) The offset voltage and offset current limits are the maximum values required to drive the output within a volt of either supply with a 1 mA load. Therefore, these parameters define an error band and take into account the worst-case effects of voltage gain and input impedance.
(2) This specification gives the range of current which must be drawn from the strobe pin to ensure the output is properly disabled. Do not short the strobe pin to ground; it should be current driven at 3 mA to 5 mA.

DC Electrical Characteristics (continued)

Unless otherwise specified, all limits guaranteed for T_J = 25°C. **Boldface** limits apply at the temperature extremes. V^+ = 2.7V, V^- = 0V, 50Ω ≤ R_L ≤ 50kΩ, and I_L = 1.0 mA unless otherwise specified

Symbol	Parameter	Conditions	Typical	LM6511I	Units
				Limit	(Limits)
V_{IN}	Input Voltage Range			0.50	V min
				V^+ − 1.25	V max
	Output Leakage Current	V_{IN} ≥ 10 mV, V_{OUT} = 35V, I_{STROBE} = 3 mA	0.2		nA max

## AC Electrical Characteristics

Unless otherwise specified, all limits guaranteed for T_J = 25°C. **Boldface** limits apply at the temperature extremes. V^+ = 2.7V, V^- = 0V, 50Ω ≤ R_L ≤ 50kΩ, and I_L = 1.0 mA unless otherwise specified

Symbol	Parameter	Conditions	Typical	LM6511I	Units
				Limit	(Limits)
T_R	Response Time	See[1]	180		ns

(1)   This specification is for a 100 mV input step with a 25 mV overdrive.

LM6511 Typical Performance Characteristics

V_S = 3V unless otherwise noted
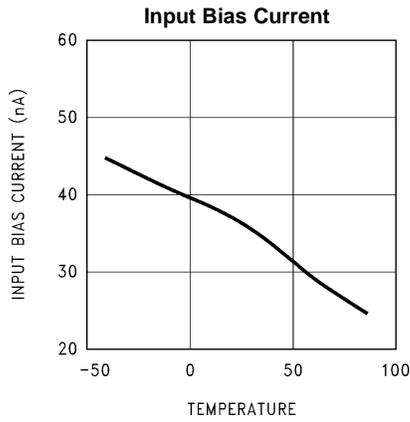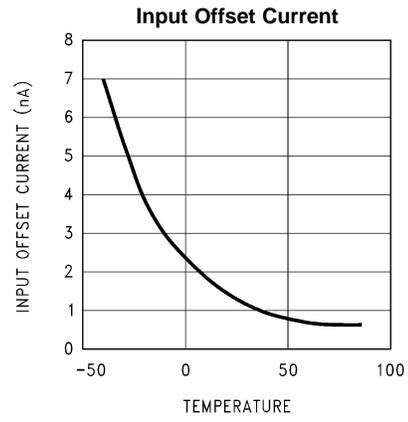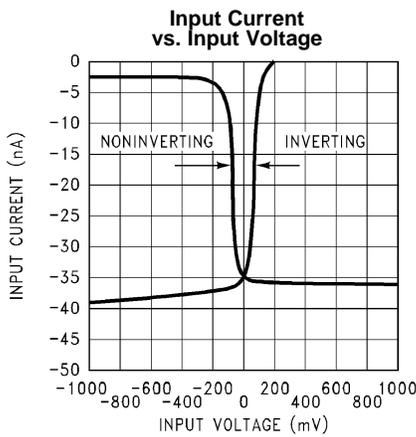
Input Bias Current

Figure 2.

Input Offset Current

Figure 3.

**Input Current
vs. Input Voltage**

Figure 4.

Common Mode Limits

Figure 5.

Transfer Function

Figure 6.

Output Saturation Voltage

Figure 7.

Product Folder Links: *LM6511*
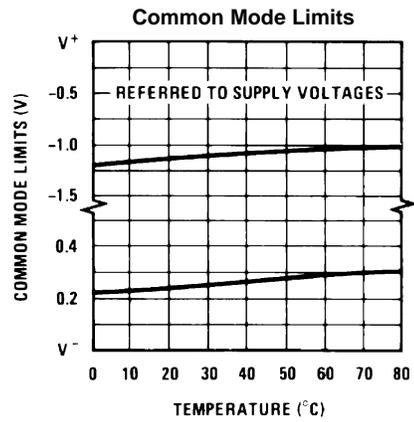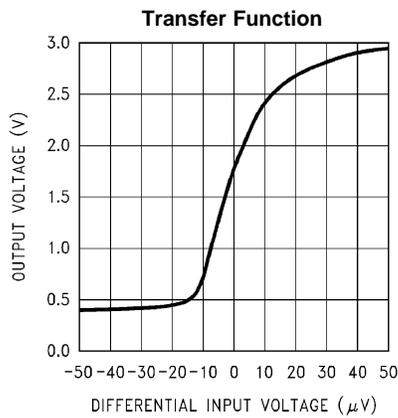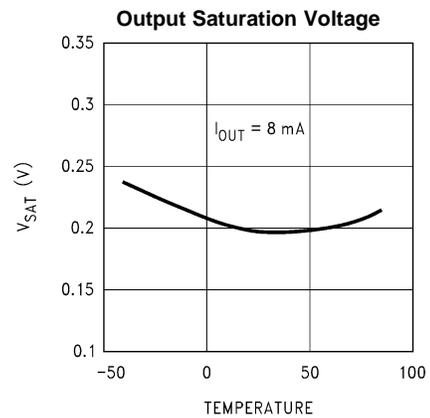
LM6511 Typical Performance Characteristics (continued)

V_S = 3V unless otherwise noted

Output Current Limiting

Figure 8.

Supply Current vs. Temperature

Figure 9.

Output Leakage Current

Figure 10.

Propagation Delay vs. Overdrive
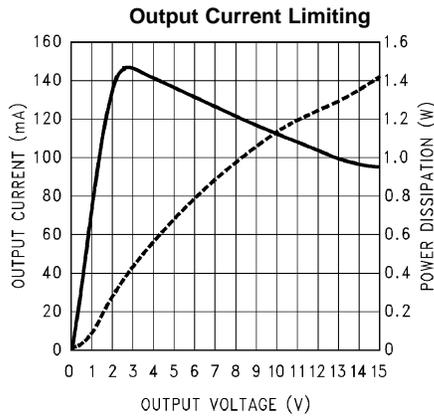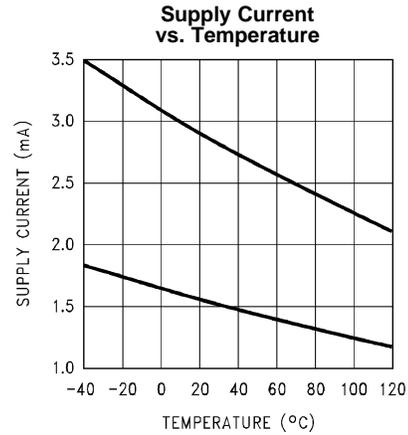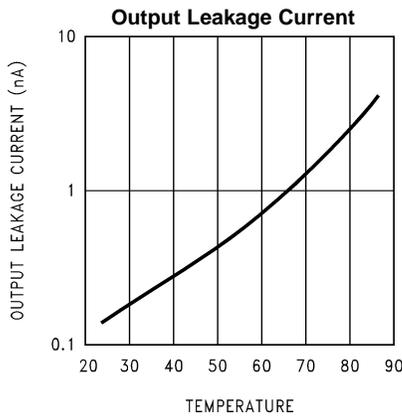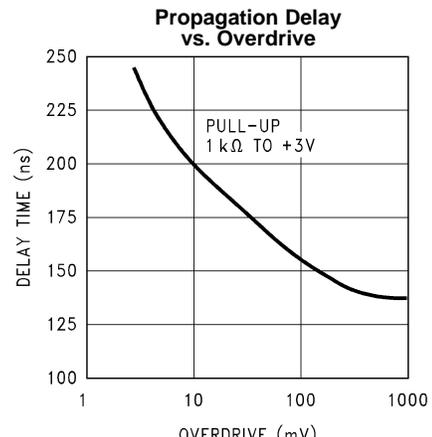
Figure 11.

Typical Application

Figure 12. Universal Logic Level Shifter
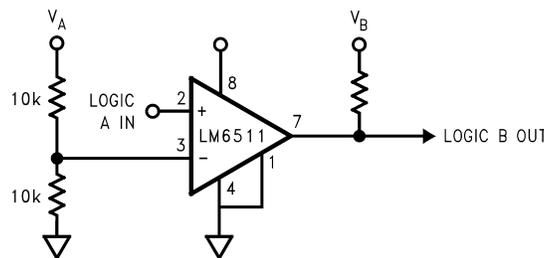
Notes: Because of the very wide operating and output voltage range, the LM6511 may be used to shift logic levels from 3V to TTL or CMOS to the other way around. By biasing the input to ½ of the input logic supply (V_A), this assures that this input remains within the input voltage range. The pull-up resistor should go to the output logic supply (V_B).

Product Folder Links: LM6511

Schematic Diagram

Copyright © 1999–2013, Texas Instruments Incorporated

Product Folder Links: *LM6511*
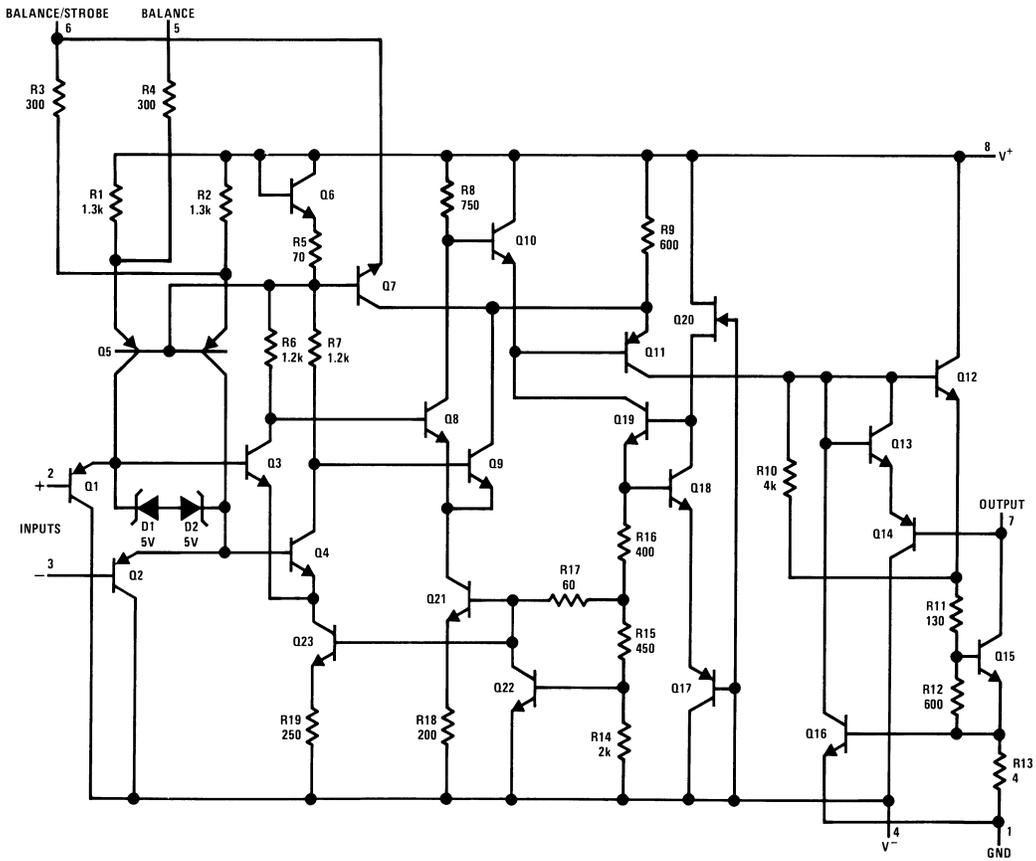
REVISION HISTORY

Changes from Revision B (March 2013) to Revision C   **Page**

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM6511IM	ACTIVE	SOIC	D	8	95	Non-RoHS & Green	Call TI	Level-1-235C-UNLIM	-40 to 85	LM65 11IM	Samples
LM6511IM/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LM65 11IM	Samples
LM6511IMX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	LM65 11IM	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers
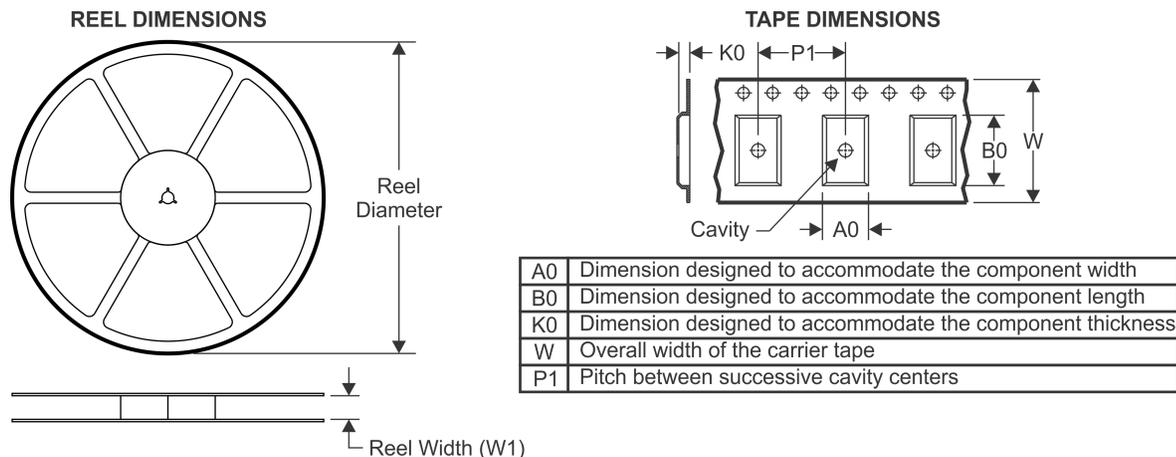
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE
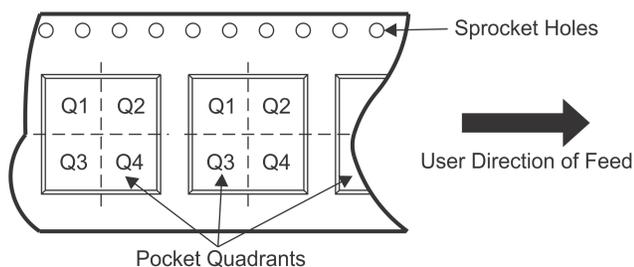
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM6511IMX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS
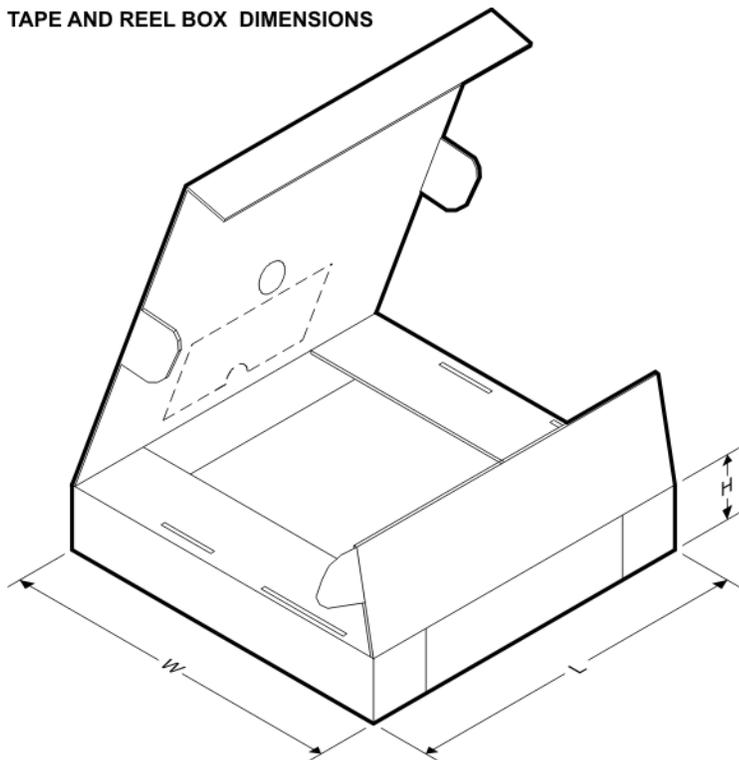
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM6511IMX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

![Texas Instruments logo]

PACKAGE MATERIALS INFORMATION

TUBE
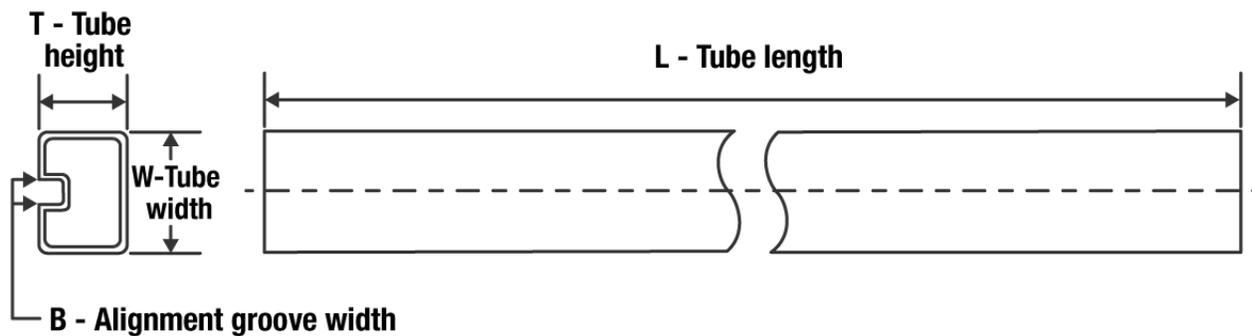
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LM6511IM	D	SOIC	8	95	495	8	4064	3.05
LM6511IM	D	SOIC	8	95	495	8	4064	3.05
LM6511IM/NOPB	D	SOIC	8	95	495	8	4064	3.05
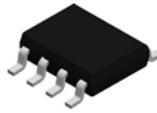
.228-.244   TYP
[5.80-6.19]

A

PIN 1 ID AREA

1

8

6X .050
[1.27]

.189-.197
[4.81-5.00]
NOTE 3

2X
.150
[3.81]

4

5

B

.150-.157
[3.81-3.98]
NOTE 4

8X .012-.020
[0.31-0.51]

⊕ .010 [0.25] Ⓜ C A B

C

SEATING PLANE

⌒ .004 [0.1] C

4X (0°-15°)

.069 MAX
[1.75]

SEE DETAIL A

4X (0°-15°)

.005-.010   TYP
[0.13-0.25]

.010
[0.25]

0°- 8°

.016-.050
[0.41-1.27]

(.041)
[1.04]

.004-.010
[0.11-0.25]

DETAIL A
TYPICAL
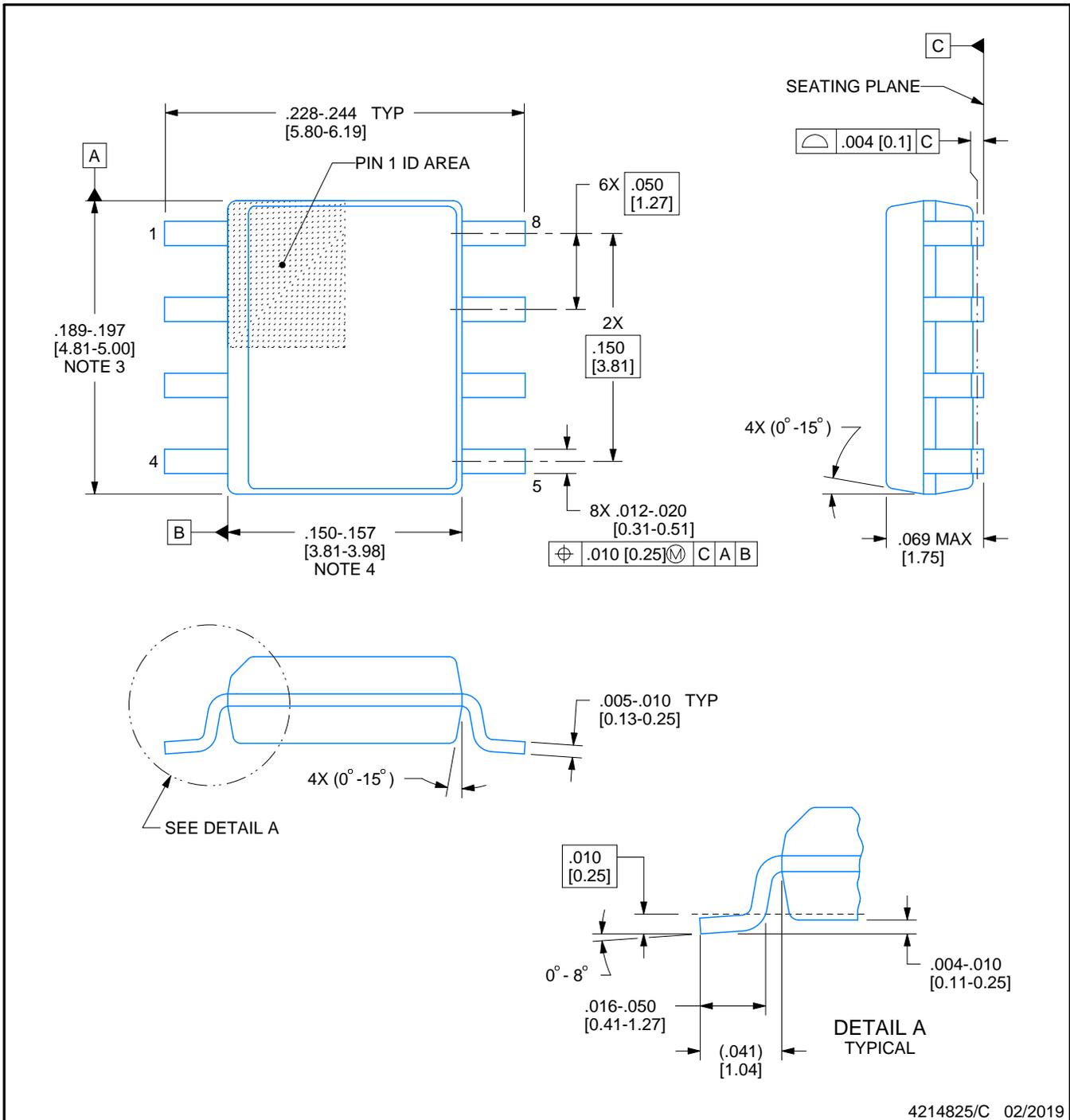
4214825/C   02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches.
   Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not
   exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

8X (.061)
[1.55]

SYMM
₵

SEE
DETAILS

1

8X (.024)
[0.6]

8

SYMM
₵

6X (.050)
[1.27]

4

(R.002) TYP
[0.05]

5

(.213)
[5.4]
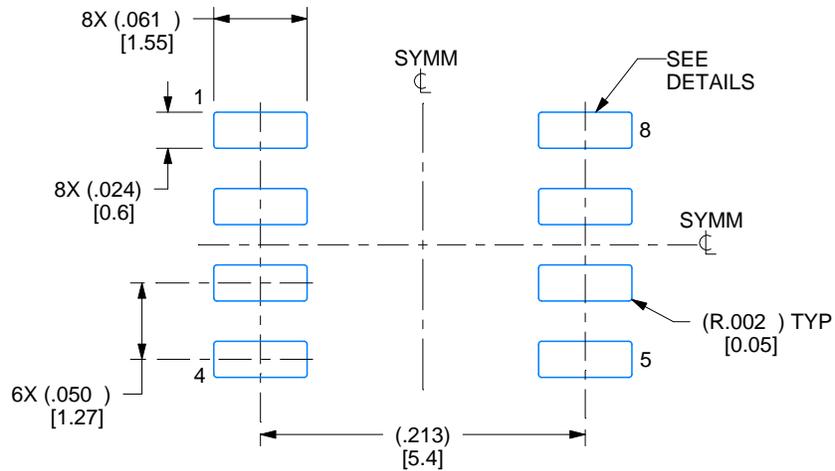
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

METAL

SOLDER MASK
OPENING

SOLDER MASK
OPENING

METAL UNDER
SOLDER MASK

EXPOSED
METAL

EXPOSED
METAL

.0028 MAX
[0.07]
ALL AROUND

.0028 MIN
[0.07]
ALL AROUND

NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED
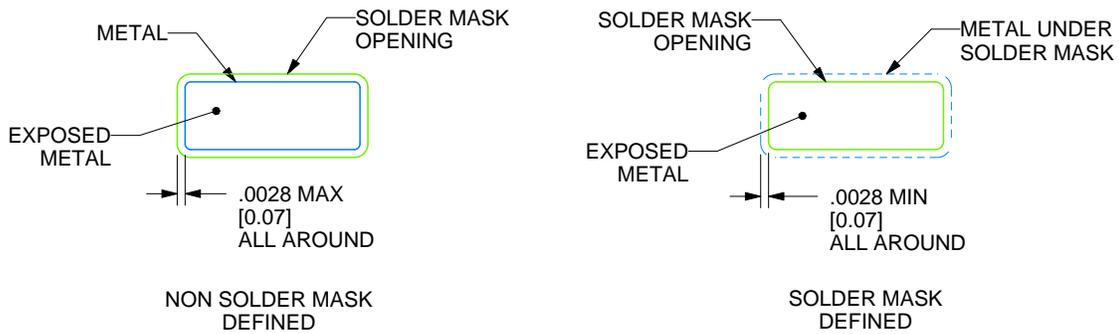
SOLDER MASK DETAILS

4214825/C   02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

8X (.061)
[1.55]

SYMM
℄

1

8X (.024)
[0.6]

8

SYMM
℄

(R.002) TYP
[0.05]

6X (.050)
[1.27]

4

5

(.213)
[5.4]
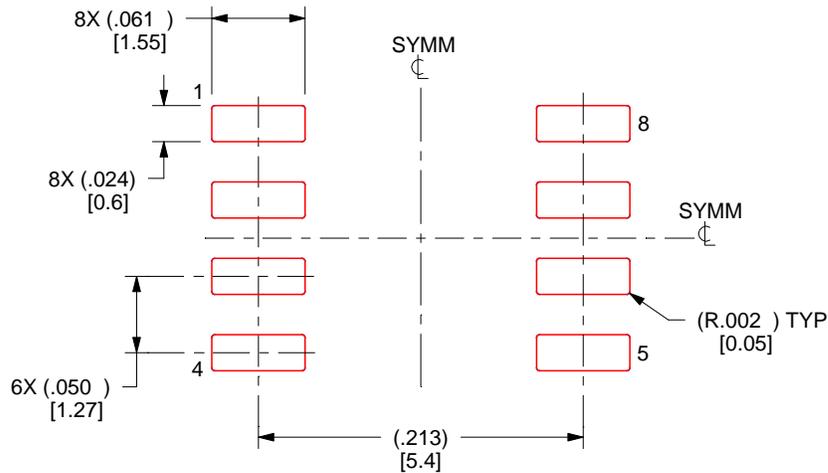
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
   design recommendations.
9. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER