LAN9303/LAN9303i

Small Form Factor Three Port 10/100 Managed Ethernet Switch with Single MII/RMII/Turbo MII

PRODUCT FEATURES

Data Brief

Highlights

- Up to 200Mbps via Turbo MII Interface
- High performance, full featured 3 port switch with VLAN, QoS packet prioritization, Rate Limiting, IGMP monitoring and management functions
- Serial management via I^2C or SMI
- Unique Virtual PHY feature simplifies software development by mimicking the multiple switch ports as a single port PHY

Target Applications

- Cable, satellite, and IP set-top boxes
- Digital televisions
- Digital video recorders
- VoIP/Video phone systems
- Home gateways
- Test/Measurement equipment
- Industrial automation systems

Key Benefits

- Ethernet Switch Fabric
  - 32K buffer RAM
  - 512 entry forwarding table
  - Port based IEEE 802.1Q VLAN support (16 groups)
    - Programmable IEEE 802.1Q tag insertion/removal
  - IEEE 802.1D spanning tree protocol support
  - 4 separate transmit queues available per port
  - Fixed or weighted egress priority servicing
  - QoS/CoS Packet prioritization
    - Input priority determined by VLAN tag, DA lookup, TOS, DIFFSERV or port default value
    - Programmable Traffic Class map based on input priority on per port basis
    - Remapping of 802.1Q priority field on per port basis
    - Programmable rate limiting at the ingress with coloring and random early discard, per port / priority
    - Programmable rate limiting at the egress with leaky bucket algorithm, per port / priority
  - IGMP v1/v2/v3 monitoring for Multicast packet filtering
  - Programmable broadcast storm protection with global % control and enable per port
  - Programmable buffer usage limits
  - Dynamic queues on internal memory
  - Programmable filter by MAC address
- Switch Management
  - Port mirroring/monitoring/sniffing: ingress and/or egress traffic on any port or port pair
  - Fully compliant statistics (MIB) gathering counters
  - Control registers configurable on-the-fly
- Ports
  - Port 0 - MII MAC, MII PHY, RMII PHY modes
  - 2 internal 10/100 PHYs with HP Auto-MDIX support
  - 200Mbps Turbo MII (PHY or MAC mode)
  - Fully compliant with IEEE 802.3 standards
  - 10BASE-T and 100BASE-TX support
  - Full and half duplex support
  - Full duplex flow control
  - Backpressure (forced collision) half duplex flow control
  - Automatic flow control based on programmable levels
  - Automatic 32-bit CRC generation and checking
  - 2K Jumbo packet support
  - Programmable interframe gap, flow control pause value
  - Full transmit/receive statistics
  - Full LED support per port
  - Auto-negotiation
  - Automatic polarity correction
  - Automatic MDI/MDI-X
  - Loop-back mode
- Serial Management
  - I^2C (slave) access to all internal registers
  - MIIM (MDIO) access to PHY related registers
  - SMI (extended MIIM) access to all internal registers
- Other Features
  - General Purpose Timer
  - I^2C Serial EEPROM interface
  - Programmable GPIOs/LEDs
- Single 3.3V power supply
- 56-pin QFN (8x8 mm) Lead-Free RoHS Compliant Package
- Available in Commercial & Industrial Temp. Ranges

Order Number(s):

LAN9303-ABZJ for 56-Pin, QFN Lead-Free RoHS Compliant Package (0 TO 70°C Temp Range)

LAN9303i-ABZJ for 56-Pin, QFN Lead-Free RoHS Compliant Package(-40 TO 85°C Temp Range)

This product meets the halogen maximum concentration values per IEC61249-2-21

For RoHS compliance and environmental information, please visit www.smsc.com/rohs

80 ARKAY DRIVE, HAUPPAUGE, NY 11788 (631) 435-6000 or 1 (800) 443-SEMI

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General Description

The LAN9303/LAN9303i is a full featured, 3 port 10/100 managed Ethernet switch designed for embedded applications where performance, flexibility, ease of integration and system cost control are required. The LAN9303/LAN9303i combines all the functions of a 10/100 switch system, including the Switch Fabric, packet buffers, Buffer Manager, Media Access Controllers (MACs), PHY transceivers, and serial management. The LAN9303/LAN9303i complies with the IEEE 802.3 (full/half-duplex 10BASE-T and 100BASE-TX) Ethernet protocol specification and 802.1D/802.1Q network management protocol specifications, enabling compatibility with industry standard Ethernet and Fast Ethernet applications.

At the core of the device is the high performance, high efficiency 3 port Ethernet Switch Fabric. The Switch Fabric contains a 3 port VLAN layer 2 Switch Engine that supports untagged, VLAN tagged, and priority tagged frames. The Switch Fabric provides an extensive feature set which includes spanning tree protocol support, multicast packet filtering and Quality of Service (QoS) packet prioritization by VLAN tag, destination address, port default value or DIFFSERV/TOS, allowing for a range of prioritization implementations. 32K of buffer RAM allows for the storage of multiple packets while forwarding operations are completed, and a 512 entry forwarding table provides ample room for MAC address forwarding tables. Each port is allocated a cluster of 4 dynamic QoS queues which allow each queue size to grow and shrink with traffic, effectively utilizing all available memory. This memory is managed dynamically via the Buffer Manager block within the Switch Fabric. All aspects of the Switch Fabric are managed via the Switch Fabric configuration and status registers, which are indirectly accessible via the system control and status registers.

The LAN9303/LAN9303i provides 3 switched ports. Each port is fully compliant with the IEEE 802.3 standard and all internal MACs and PHYs support full/half duplex 10BASE-T and 100BASE-TX operation. The LAN9303/LAN9303i provides 2 on-chip PHYs, 1 Virtual PHY and 3 MACs. The Virtual PHY and the third MAC are used to connect the Switch Fabric to an external MAC or PHY. In MAC mode, the device can be connected to an external PHY via the MII/Turbo MII interface. In PHY mode, the device can be connected to an external MAC via the MII/RMII/Turbo MII interface. All ports support automatic or manual full duplex flow control or half duplex backpressure (forced collision) flow control. 2K jumbo packet (2048 byte) support allows for oversized packet transfers, effectively increasing throughput while decreasing CPU load. All MAC and PHY related settings are fully configurable via their respective registers within the device.

The integrated I^2C and SMI slave controllers allow for full serial management of the device via the integrated I^2C or MII interface, respectively. The inclusion of these interfaces allows for greater flexibility in the incorporation of the device into various designs. It is this flexibility which allows the device to operate in 2 different modes and under various management conditions. In both MAC and PHY modes, the device can be SMI managed or I^2C managed. This flexibility in management makes the LAN9303/LAN9303i a candidate for virtually all switch applications.

The LAN9303/LAN9303i contains an I^2C master EEPROM controller for connection to an optional EEPROM. This allows for the storage and retrieval of static data. The internal EEPROM Loader can be optionally configured to automatically load stored configuration settings from the EEPROM into the device at reset. The I^2C management slave and master EEPROM controller share common pins.

In addition to the primary functionality described above, the LAN9303/LAN9303i provides additional features designed for extended functionality. These include a configurable 16-bit General Purpose Timer (GPT), a 32-bit 25MHz free running counter, and 6-bit configurable GPIO/LED interface.

The LAN9303/LAN9303i's performance, features and small size make it an ideal solution for many applications in the consumer electronics and industrial automation markets. Targeted applications include: set top boxes (cable, satellite and IP), digital televisions, digital video recorders, voice over IP and video phone systems, home gateways, and test and measurement equipment.

Block Diagram

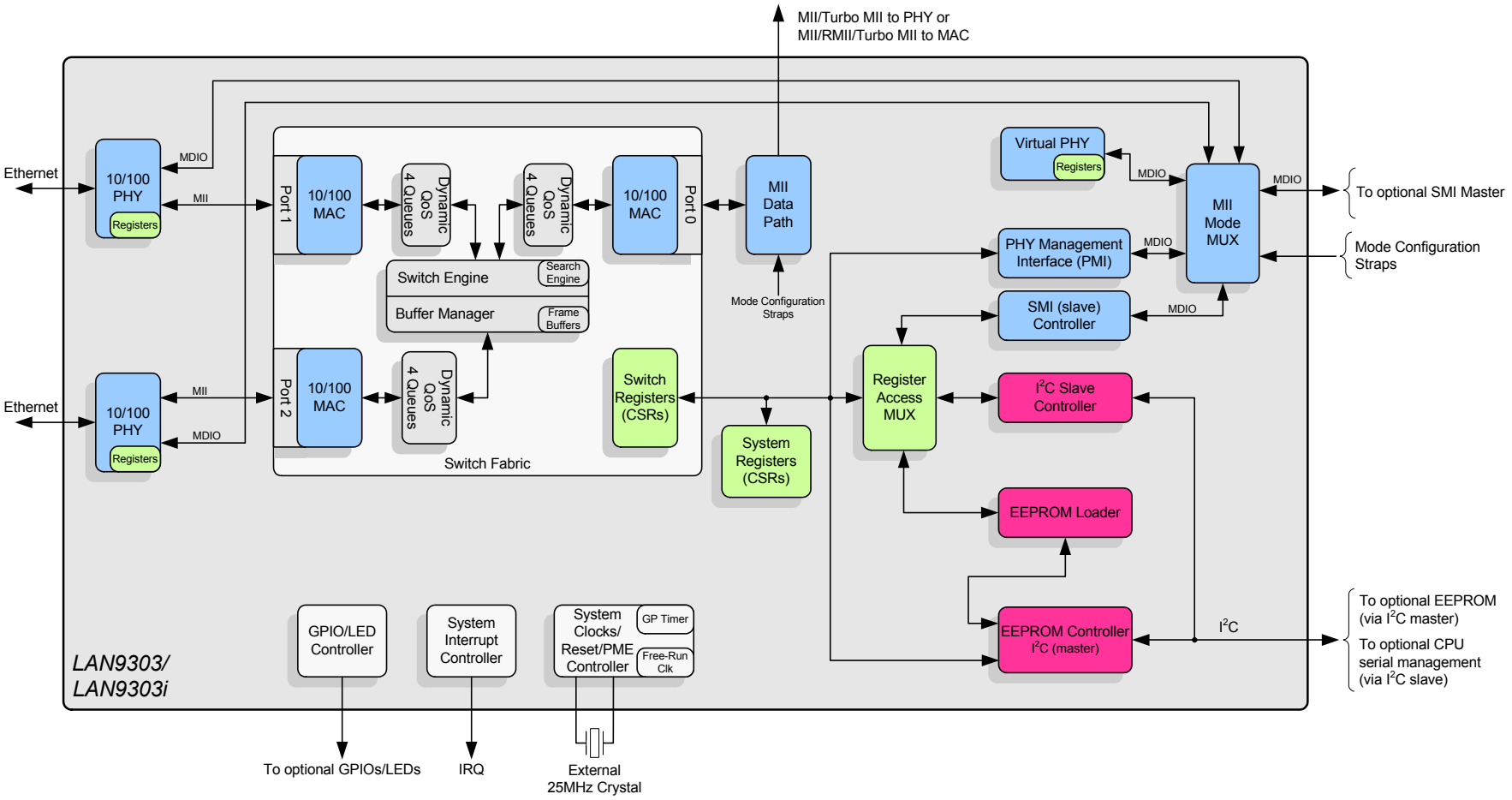


Figure 1 Internal Block Diagram

Package Outline

56-QFN Package Outline

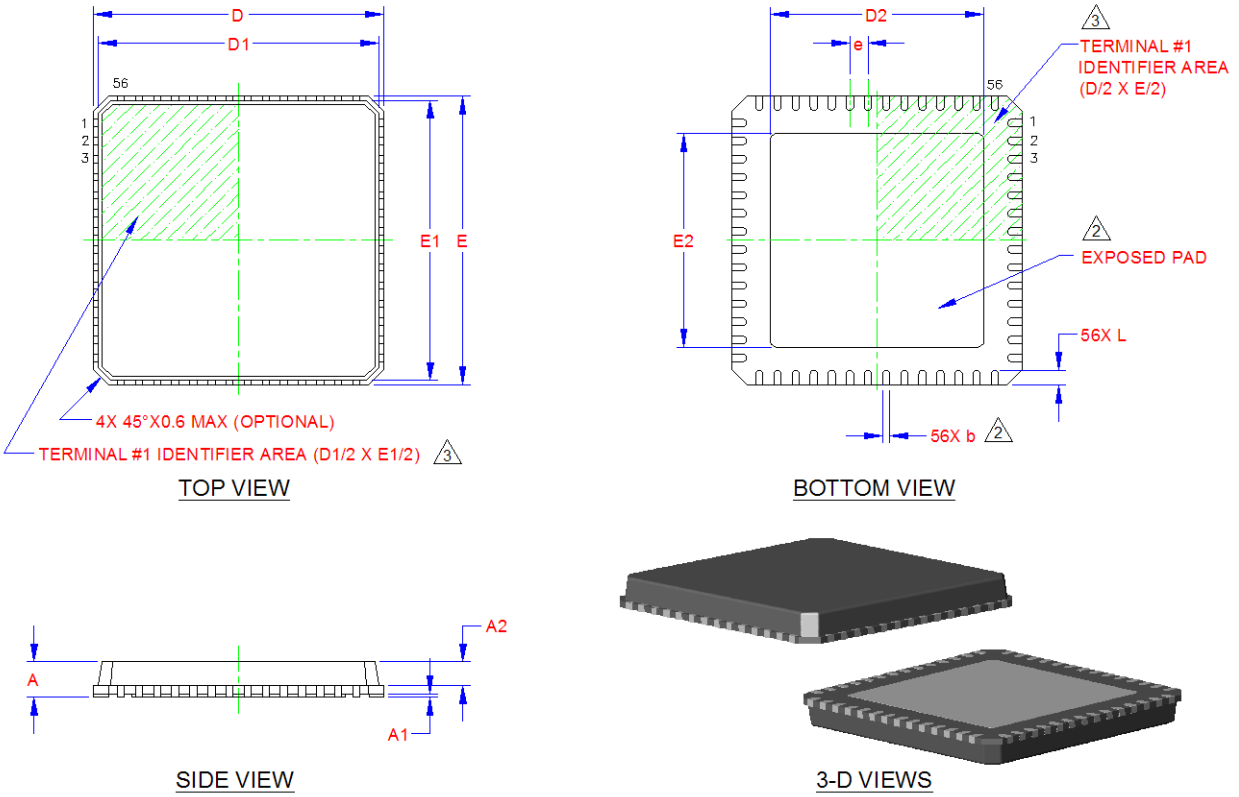


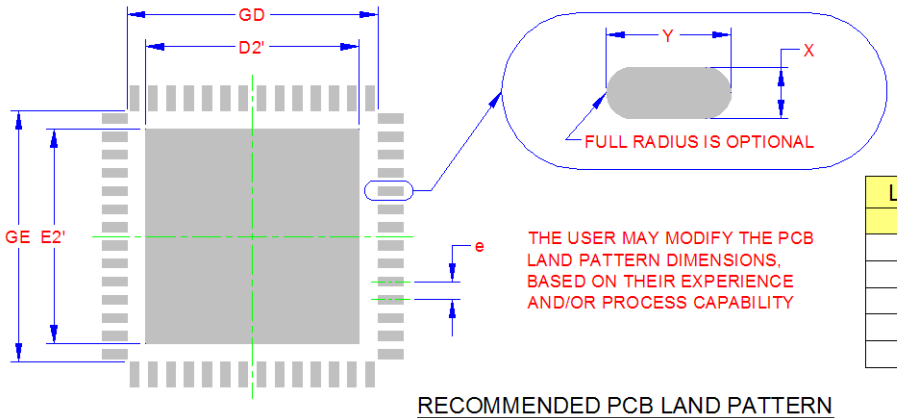
Figure 2 56-QFN Package Definition

Table 1 56-QFN Dimensions

	MIN	NOMINAL	MAX	REMARKS
A	0.70	-	1.00	Overall Package Height
A1	0	0.02	0.05	Standoff
A2	-	-	0.90	Mold Cap Thickness
D/E	7.85	8.00	8.15	X/Y Body Size
D1/E1	7.55	-	7.95	X/Y Mold Cap Size
D2/E2	5.75	5.90	6.05	X/Y Exposed Pad Size
L	0.30	-	0.50	Terminal Length
b	0.18	0.25	0.30	Terminal Width
e	0.50 BSC			Terminal Pitch

Notes:

1. All dimensions are in millimeters unless otherwise noted.
2. Position tolerance of each terminal and exposed pad is +/- 0.05mm at maximum material condition. Dimension “b” applies to plated terminals and is measured between 0.15 and 0.30mm from the terminal tip.
3. The pin 1 identifier may vary, but is always located within the zone indicated



LAND PATTERN DIMENSIONS			
SYMBOL	MIN	NOM	MAX
GD/GE	6.93	-	-
D2'/E2'		5.90	
X	-	-	0.28
Y	-	-	0.69
e		0.50	

Figure 3 56-QFN Recommended PCB Land Pattern