

## Terminal Voltage $\pm 2.7V$ or $\pm 5V$ , 128 Taps I<sup>2</sup>C Serial Interface

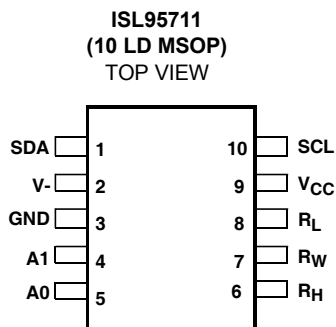
The Intersil ISL95711 is a digitally controlled potentiometer (XDCP). The device consists of a resistor array, wiper switches, a control section, and nonvolatile memory. The wiper position is controlled by a I<sup>2</sup>C interface.

The potentiometer is implemented by a resistor array composed of 127 resistive elements and a wiper switching network. The wiper terminal can be connected to either end of the resistor array or at any one of the Tap Positions in between, providing 128 steps of resolution between R<sub>L</sub> and R<sub>H</sub>. The "position" of the wiper is determined by the value assigned to the volatile Wiper Register (WR). This register has an associated non-volatile Initial Value Register (IVR). The value stored in the IVR will be written into the WR at power-up, allowing wiper position recall after power interruption. The WR and the IVR can be directly written to and read from using standard I<sup>2</sup>C interface protocol. The device is available in either a 10k $\Omega$  or 50k $\Omega$  version.

The device can be used as a three-terminal potentiometer or as a two-terminal variable resistor in a wide variety of applications including:

- Industrial and automotive control
- Parameter and bias adjustments
- Amplifier bias and control

## Pinout



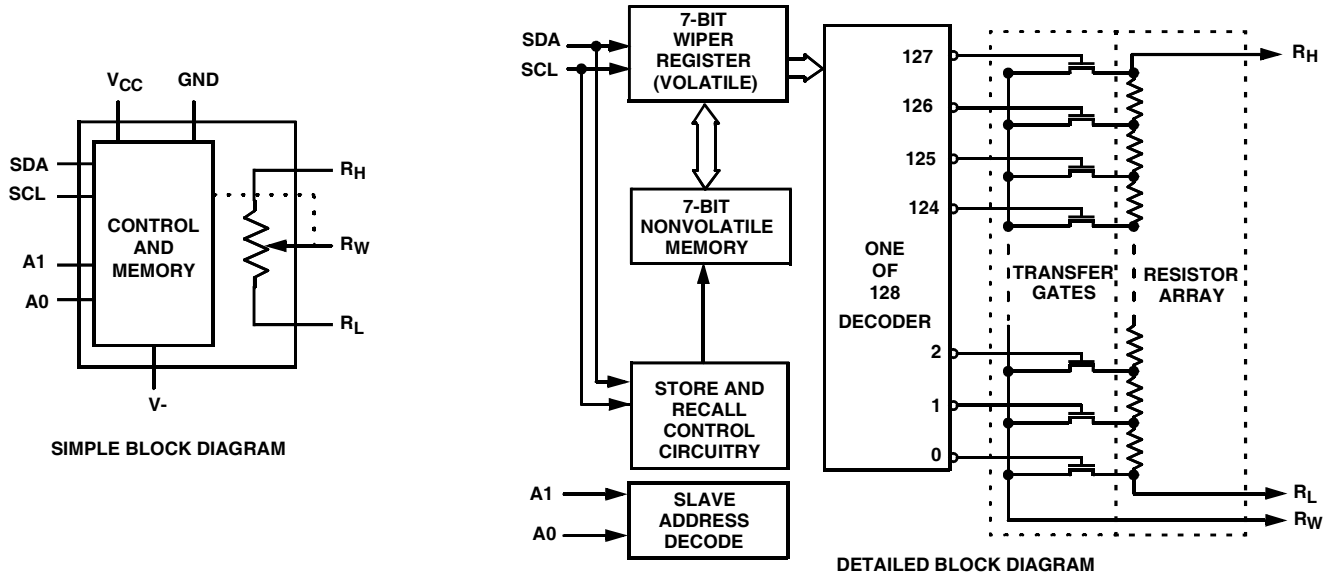
## Ordering Information

PART NUMBER (Notes 1, 2)	PART MARKING	RESISTANCE OPTION ( $\Omega$ )	TEMP. RANGE ( $^{\circ}C$ )	PACKAGE (Pb-Free)	PKG. DWG. #
ISL95711WIU10Z	AKO	10k	-40 to +85	10 Ld MSOP	M10.118
ISL95711UIU10Z	AKQ	50k	-40 to +85	10 Ld MSOP	M10.118

### NOTES:

1. Add "-T" suffix for tape and reel.
2. Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

**Block Diagram**



**Pin Descriptions**

PIN NUMBER	SYMBOL	DESCRIPTION
1	SDA	Open drain Data I/O for I <sup>2</sup> C serial interface
2	V-	Negative supply voltage for the potentiometer wiper control
3	GND	Ground
4	A1	A1 and A0 are address select pins used to set the slave address for the I <sup>2</sup> C serial interface
5	A0	A1 and A0 are address select pins used to set the slave address for the I <sup>2</sup> C serial interface
6	R <sub>H</sub>	A fixed terminal for one end of the potentiometer resistor.
7	R <sub>W</sub>	The wiper terminal which is equivalent to the movable terminal of a potentiometer.
8	R <sub>L</sub>	A fixed terminal for one end of the potentiometer resistor.
9	V <sub>CC</sub>	Positive logic supply voltage
10	SCL	Clock input for the I <sup>2</sup> C serial interface

**Absolute Maximum Ratings**

Temperature under bias	-65°C to +135°C
Storage temperature	-65°C to +150°C
Voltage on SDA, SCL, A0, and A1 with respect to GND	-0.3 to $V_{CC}+0.3V$
Voltage on V- (referenced to GND)	-6V
$\Delta V =  V_{(RH)} - V_{(RL)} $	.12V
Lead temperature (soldering 10s)	300°C
$I_W$ (10s)	$\pm 6mA$
$V_{CC}$	-0.03V to 6V
$R_H, R_L, R_W$	V- to $V_{CC}$
ESD (Mil-Std 883, Method 3015)	>2kV
ESD Machine Model	>150V

**Thermal Information**

Thermal Resistance (Typical, Note 3)	$\theta_{JA}$ (°C/W)
MSOP Package	+170

**Recommended Operating Conditions**

Temperature Range (Industrial)	-40°C to +85°C
$V_{CC}$	2.7V to 5.5V
V-	-2.7V to -5.5V

**CAUTION:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device (at these or any other conditions above those listed in the operational sections of this specification) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**NOTE:**

- $\theta_{JA}$  is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

**Analog Specifications**

Over recommended operating conditions unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (Note 1)	MAX	UNIT
$R_{TOTAL}$	$R_H$ to $R_L$ resistance	W option		10		k $\Omega$
		U option		50		k $\Omega$
	$R_H$ to $R_L$ resistance tolerance		-20		+20	%
$TC_R$ (Notes 12, 13)	Resistance Temperature Coefficient	$I_{DCP} = 1mA$ $T = -40^\circ C$ to $+85^\circ C$		$\pm 50$		ppm/ $^\circ C$
$R_H, R_L$	$R_H, R_L$ terminal voltage		V-		$V_{CC}$	V
$R_W$	Wiper resistance	V- = -5.5V; $V_{CC} = +5.5V$ , wiper current = $(V_{CC}-V-)/R_{TOTAL}$		70	200	$\Omega$
$C_H/C_L/C_W$	Potentiometer Capacitance (Note 13)			10/10/ 25		pF
$I_{LkgDCP}$	Leakage on $R_H, R_L, R_W$ pins	Voltage at pins; V- to $V_{CC}$		0.1	1	$\mu A$
<b>VOLTAGE DIVIDER MODE</b> (V- @ $R_L$ ; $V_{CC}$ @ $R_H$ ; Voltage at $R_W = V_{RW}$ unloaded)						
INL (Note 6)	Integral non-linearity		-1		1	LSB (Note 6)
DNL (Note 5)	Differential non-linearity	W, U options	-0.5		0.5	LSB (Note 2)
ZSerror (Note 3)	Zero-scale error	W option	0	1	4	LSB (Note 2)
		U option	0	0.5	2	
FSerror (Note 4)	Full-scale error	W option	-4	-1	0	LSB (Note 2)
		U option	-2	-1	0	
$TC_V$ (Notes 7, 13)	Ratiometric Temperature Coefficient	DCP Register set at 63d, $T = -40^\circ C$ to $+85^\circ C$		$\pm 4$		ppm/ $^\circ C$
<b>RESISTOR MODE</b> (Measurements between $R_W$ and $R_L$ with $R_H$ not connected, or between $R_W$ and $R_H$ with $R_L$ not connected)						
RINL (Note 11)	Integral non-linearity	DCP register set between 20 hex and 7F hex. Monotonic over all tap positions	-1		1	MI (Note 8)
RDNL (Note 10)	Differential non-linearity	W and U options	-0.5		0.5	MI (Note 8)
Roffset (Note 9)	Offset	DCP Register set to 00 hex, W option	0	2	5	MI (Note 8)
		DCP Register set to 00 hex, U option	0	0.5	2	

**Operating Specifications** Over the recommended operating conditions unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (Note 1)	MAX	UNITS
I <sub>CC1</sub>	V <sub>CC</sub> supply current, volatile write/read	f <sub>SCL</sub> = 400kHz; SDA = Open; (for I <sup>2</sup> C, Active, Read and Volatile Write States only)			200	μA
I <sub>V-1</sub>	V- supply current, volatile write/read	f <sub>SCL</sub> = 400kHz; SDA = Open; (for I <sup>2</sup> C, Active, Read and Volatile Write States only)	-100			μA
I <sub>CC2</sub>	V <sub>CC</sub> supply current, non volatile write	f <sub>SCL</sub> = 400kHz; SDA = Open; (for I <sup>2</sup> C, Active, Nonvolatile Write State only)			200	μA
I <sub>V-2</sub>	V- supply current, nonvolatile write	f <sub>SCL</sub> = 400kHz; SDA = Open; (for I <sup>2</sup> C, Active, Nonvolatile Write State only)	-3			mA
I <sub>CCSB</sub>	V <sub>CC</sub> current (standby)	V <sub>CC</sub> = +5.5V, I <sup>2</sup> C Interface in Standby State			1	μA
		V <sub>CC</sub> = +3.6V, I <sup>2</sup> C Interface in Standby State			1	μA
I <sub>V-SB</sub>	V- current (standby)	V- = -5.5V, I <sup>2</sup> C Interface in Standby State	-5			μA
		V- = -3.6V, I <sup>2</sup> C Interface in Standby State	-2			μA
I <sub>LkgDig</sub>	Leakage current, at pins SDA, SCL, A0, and A1	Voltage at pin from GND to V <sub>CC</sub>	-10		10	μA
t <sub>DCP</sub> (Note 13)	DCP wiper response time	SCL falling edge of last bit of DCP Data Byte to wiper change		1		μs
V <sub>por</sub>	Power-on recall for both V- and V <sub>CC</sub>	V-	-2.5			V
		V <sub>CC</sub>			2.5	V
V-Ramp	V- ramp rate		0.2			V/ms
t <sub>D</sub> (Note 13)	Power-up delay	V <sub>CC</sub> above V <sub>por</sub> , to DCP Initial Value Register recall completed, and I <sup>2</sup> C Interface in standby state		3		ms

**EEPROM SPECS**

	EEPROM Endurance		200,000			Cycles
	EEPROM Retention	Temperature ≤ +75°C	50			Years

**SERIAL INTERFACE SPECS**

V <sub>IL</sub>	A0, A1, SDA, and SCL input buffer LOW voltage		-0.3		0.3*V <sub>CC</sub>	V
V <sub>IH</sub>	A0, A1, SDA, and SCL input buffer HIGH voltage		0.7*V <sub>CC</sub>		V <sub>CC</sub> +0.3	V
Hysteresis	SDA and SCL input buffer hysteresis		0.05*V <sub>CC</sub>			V
V <sub>OL</sub>	SDA output buffer LOW voltage, sinking 4mA		0		0.4	V
C <sub>pin</sub> (Note 15)	A0, A1, SDA, and SCL pin capacitance				10	pF
f <sub>SCL</sub>	SCL frequency				400	kHz
t <sub>IN</sub>	Pulse width suppression time at SDA and SCL inputs	Any pulse narrower than the max spec is suppressed.			50	ns
t <sub>AA</sub>	SCL falling edge to SDA output data valid	SCL falling edge crossing 30% of V <sub>CC</sub> , until SDA exits the 30% to 70% of V <sub>CC</sub> window.			900	ns
t <sub>BUF</sub>	Time the bus must be free before the start of a new transmission	SDA crossing 70% of V <sub>CC</sub> during a STOP condition, to SDA crossing 70% of V <sub>CC</sub> during the following START condition.	1300			ns
t <sub>LOW</sub>	Clock LOW time	Measured at the 30% of V <sub>CC</sub> crossing.	1300			ns
t <sub>HIGH</sub>	Clock HIGH time	Measured at the 70% of V <sub>CC</sub> crossing.	600			ns
t <sub>SU:STA</sub>	START condition setup time	SCL rising edge to SDA falling edge. Both crossing 70% of V <sub>CC</sub> .	600			ns

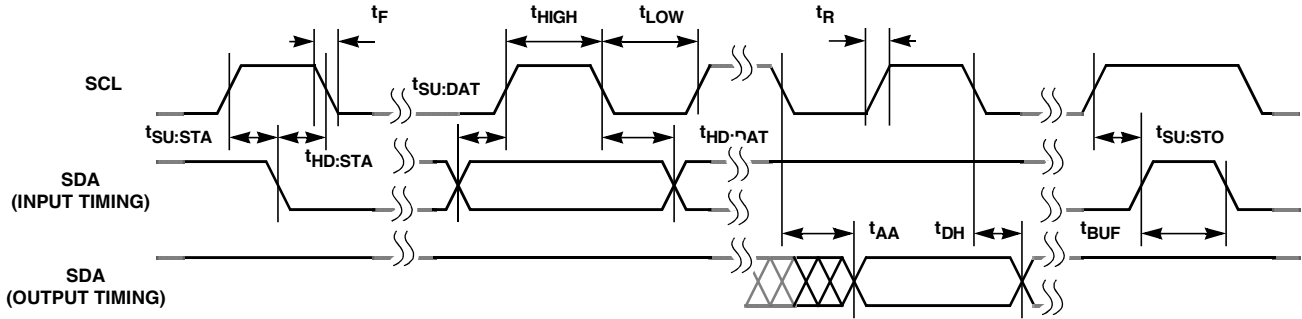
**Operating Specifications** Over the recommended operating conditions unless otherwise specified. (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP (Note 1)	MAX	UNITS
t <sub>HD:STA</sub>	START condition hold time	From SDA falling edge crossing 30% of V <sub>CC</sub> to SCL falling edge crossing 70% of V <sub>CC</sub> .	600			ns
t <sub>SU:DAT</sub>	Input data setup time	From SDA exiting the 30% to 70% of V <sub>CC</sub> window, to SCL rising edge crossing 30% of V <sub>CC</sub>	100			ns
t <sub>HD:DAT</sub>	Input data hold time	From SCL rising edge crossing 70% of V <sub>CC</sub> to SDA entering the 30% to 70% of V <sub>CC</sub> window.	0			ns
t <sub>SU:STO</sub>	STOP condition setup time	From SCL rising edge crossing 70% of V <sub>CC</sub> , to SDA rising edge crossing 30% of V <sub>CC</sub> .	600			ns
t <sub>HD:STO</sub>	STOP condition setup time	From SDA rising edge to SCL falling edge. Both crossing 70% of V <sub>CC</sub> .	600			ns
t <sub>DH</sub>	Output data hold time	From SCL falling edge crossing 30% of V <sub>CC</sub> , until SDA enters the 30% to 70% of V <sub>CC</sub> window.	0			ns
t <sub>R</sub> (Note 15)	SDA and SCL rise time	From 30% to 70% of V <sub>CC</sub>	20 + 0.1 * C <sub>b</sub>		250	ns
t <sub>F</sub> (Note 15)	SDA and SCL fall time	From 70% to 30% of V <sub>CC</sub>	20 + 0.1 * C <sub>b</sub>		250	ns
C <sub>b</sub> (Note 15)	Capacitive loading of SDA or SCL	Total on-chip and off-chip	10		400	pF
R <sub>pu</sub> (Note 15)	SDA and SCL bus pull-up resistor off-chip	Maximum is determined by t <sub>R</sub> and t <sub>F</sub> . For C <sub>b</sub> = 400pF, max is about 2~2.5kΩ. For C <sub>b</sub> = 40pF, max is about 15~20kΩ.	1			kΩ
t <sub>WC</sub> (Notes 14)	Non-volatile Write cycle time			12	20	ms
t <sub>SU:A</sub>	A0, A1 setup time	Before START condition	600			ns
t <sub>HD:A</sub>	A0, A1 hold time	After STOP condition	600			ns

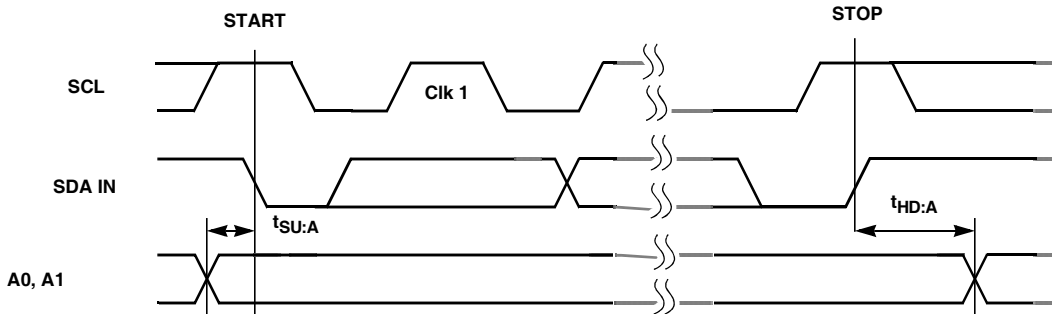
NOTES:

- Typical values are for T<sub>A</sub> = +25°C and ±5V supply voltage.
- LSB: [V(RW)<sub>127</sub> - V(RW)<sub>0</sub>]/127. V(RW)<sub>127</sub> and V(RW)<sub>0</sub> are V(RW) for the DCP register set to 7F hex and 00 hex respectively. LSB is the incremental voltage when changing from one tap to an adjacent tap.
- ZS error = (V(RW)<sub>0</sub> - V-)/LSB.
- FS error = [V(RW)<sub>127</sub> - V<sub>CC</sub>]/LSB.
- DNL = [V(RW)<sub>i</sub> - V(RW)<sub>i-1</sub>]/LSB - 1, for i = 1 to 127. i is the DCP register setting.
- INL = V(RW)<sub>i</sub> - (i \* LSB - V(RW)<sub>0</sub>)/LSB for i = 1 to 127.
- $TC_V = \frac{\text{Max}(V(RW)_i) - \text{Min}(V(RW)_i)}{[\text{Max}(V(RW)_i) + \text{Min}(V(RW)_i)]/2} \times \frac{10^6}{125^\circ\text{C}}$   
for i = 16 to 120 decimal. Max( ) is the maximum value of the wiper voltage and Min( ) is the minimum value of the wiper voltage over the temperature range.
- MI = |R<sub>127</sub> - R<sub>0</sub>|/127. R<sub>127</sub> and R<sub>0</sub> are the measured resistances for the DCP register set to 127d and 0 respectively.
- R<sub>offset</sub> = R<sub>0</sub>/MI, when measuring between R<sub>W</sub> and R<sub>L</sub>.  
R<sub>offset</sub> = R<sub>127</sub>/MI, when measuring between R<sub>W</sub> and R<sub>H</sub>.
- RDNL = (R<sub>i</sub> - R<sub>i-1</sub>)/MI - 1, for i = 16 to 127.
- RINL = [R<sub>i</sub> - (MI \* i) - R<sub>0</sub>]/MI, for i = 16 to 127.
- $TC_R = \frac{[\text{Max}(R_i) - \text{Min}(R_i)]}{[\text{Max}(R_i) + \text{Min}(R_i)]/2} \times \frac{10^6}{125^\circ\text{C}}$   
for i = 16 to 127d. Max( ) is the maximum value of the resistance and Min( ) is the minimum value of the resistance over the temperature range.
- This parameter is not 100% tested.
- t<sub>WC</sub> is the minimum cycle time to be allowed for any non-volatile Write by the user, unless Acknowledge Polling is used. It is the time from a valid STOP condition at the end of a Write sequence of a I<sup>2</sup>C serial interface Write operation, to the end of the self-timed internal non-volatile write cycle.
- These are I<sup>2</sup>C specific parameters and are not directly tested, however they are used during device testing to validate device specification.

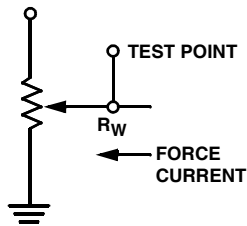
**SDA vs SCL Timing**



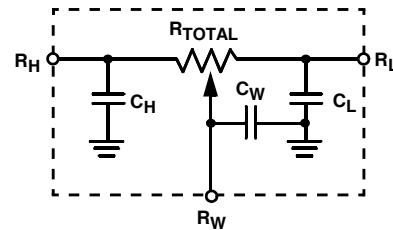
**A0, A1 Pin Timing**



**Test Circuit**



**Equivalent Circuit**



**Pin Descriptions**

**Potentiometer Pins**

**R<sub>H</sub> AND R<sub>L</sub>**

The high (R<sub>H</sub>) and low (R<sub>L</sub>) terminals of the ISL95711 are equivalent to the fixed terminals of a mechanical potentiometer. R<sub>H</sub> and R<sub>L</sub> are referenced to the relative position of the wiper and not the voltage potential on the terminals. With WR set to 127, the wiper will be closest to R<sub>H</sub>, and with the WR set to 00, the wiper is closest to R<sub>L</sub>.

**R<sub>W</sub>**

R<sub>W</sub> is the wiper terminal and is equivalent to the movable terminal of a mechanical potentiometer. The position of the wiper within the array is determined by the WR.

**Bus Interface Pins**

**SERIAL DATA INPUT/OUTPUT (SDA)**

The SDA is a bidirectional serial data input/output pin for the I<sup>2</sup>C interface. It receives device address, operation code,

wiper register address and data from a I<sup>2</sup>C external master device at the rising edge of the serial clock SCL, and it shifts out data after each falling edge of the serial clock SCL.

SDA requires an external pull-up resistor, since it's an open drain input/output.

**SERIAL CLOCK (SCL)**

This input is the serial clock of the I<sup>2</sup>C serial interface.

SCL requires an external pull-up resistor, since it's an open drain input.

**DEVICE ADDRESS (A1-A0)**

The Address inputs are used to set the least significant 2 bits of the 7-bit I<sup>2</sup>C interface slave address. A match in the slave address serial data stream must be made with the Address input pins in order to initiate communication with the ISL95711. A maximum of 4 ISL95711 devices may occupy the I<sup>2</sup>C serial bus.

Typical Performance Curves

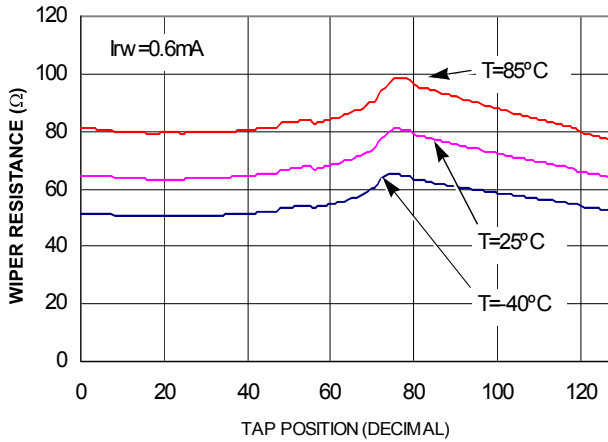


FIGURE 1. WIPER RESISTANCE vs TAP POSITION [I(RW) = V<sub>CC</sub>/R<sub>TOTAL</sub>] for 10kΩ (W)

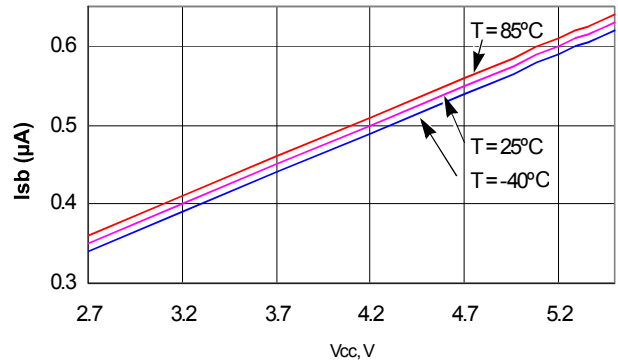


FIGURE 2. STANDBY I<sub>CC</sub> vs V<sub>CC</sub>

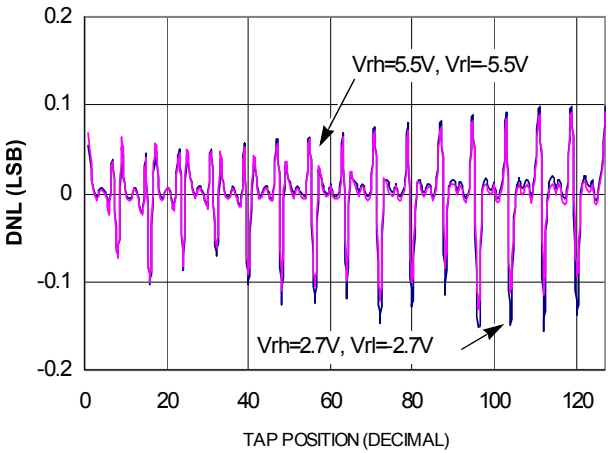


FIGURE 3. DNL vs TAP POSITION IN VOLTAGE DIVIDER MODE FOR 10kΩ (W)

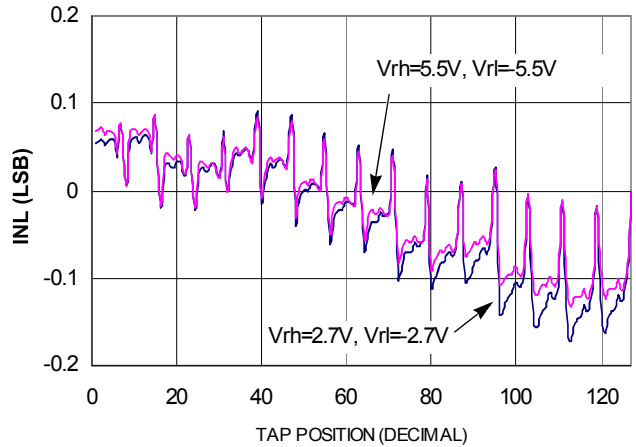


FIGURE 4. INL vs TAP POSITION IN VOLTAGE DIVIDER MODE FOR 10kΩ (W)

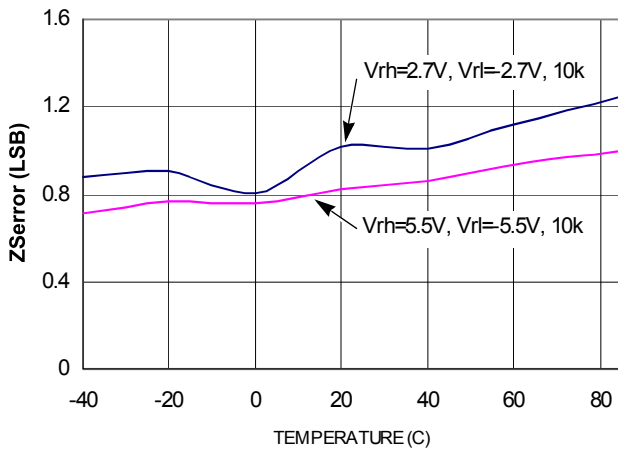


FIGURE 5. ZSerror vs TEMPERATURE

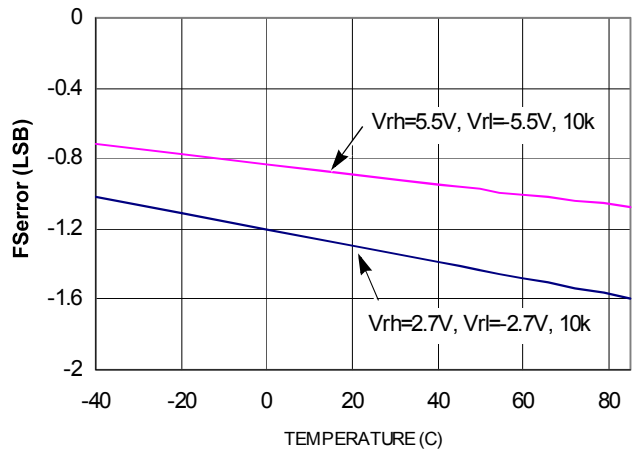


FIGURE 6. FSerror vs TEMPERATURE

Typical Performance Curves (Continued)

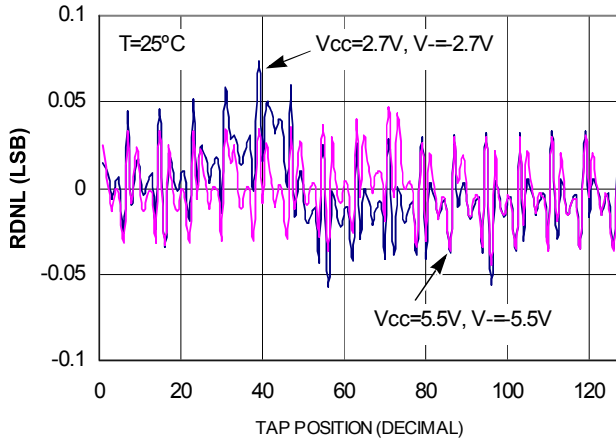


FIGURE 7. DNL vs TAP POSITION IN RHEOSTAT MODE FOR 10kΩ (W)

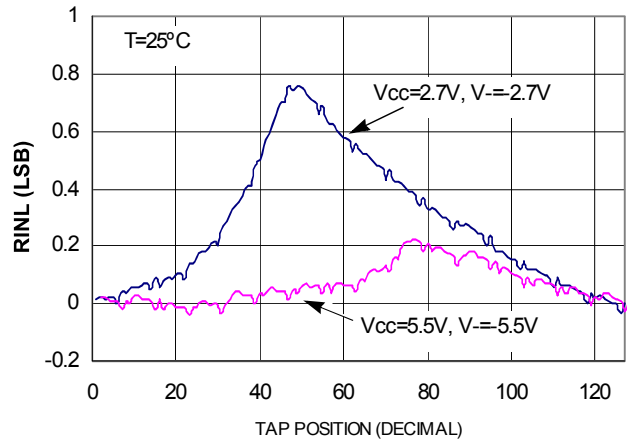


FIGURE 8. INL vs TAP POSITION IN RHEOSTAT MODE FOR 10kΩ (W)

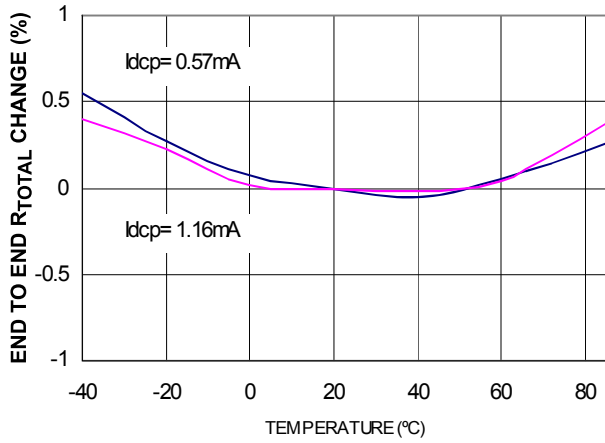


FIGURE 9. END TO END  $R_{TOTAL}$  % CHANGE vs TEMPERATURE

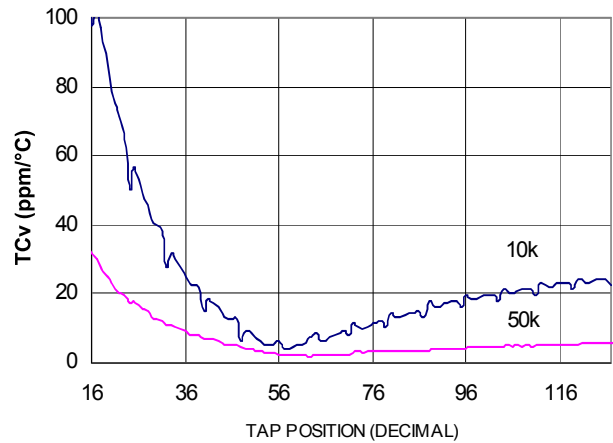


FIGURE 10. TC FOR VOLTAGE DIVIDER MODE IN ppm

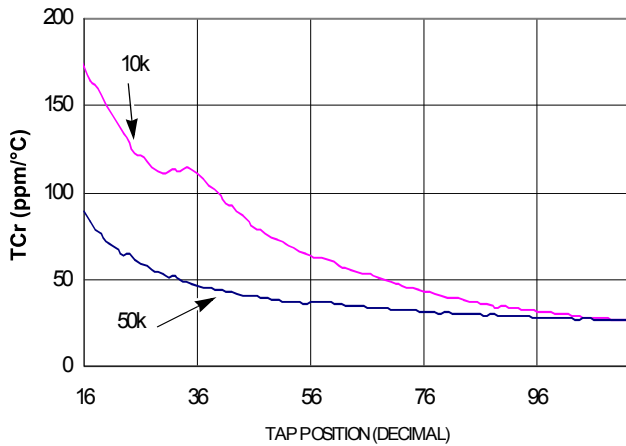


FIGURE 11. TC FOR RHEOSTAT MODE IN ppm

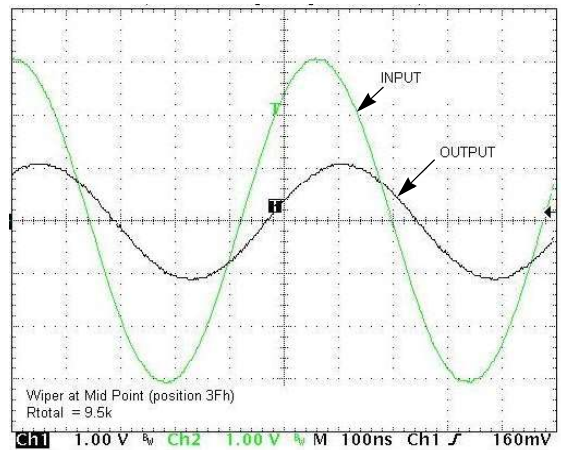


FIGURE 12. FREQUENCY RESPONSE (1.8MHz)



## Typical Performance Curves (Continued)

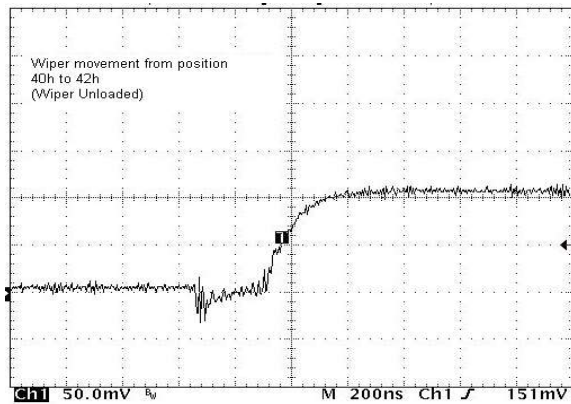


FIGURE 13. WIPER MOVEMENT

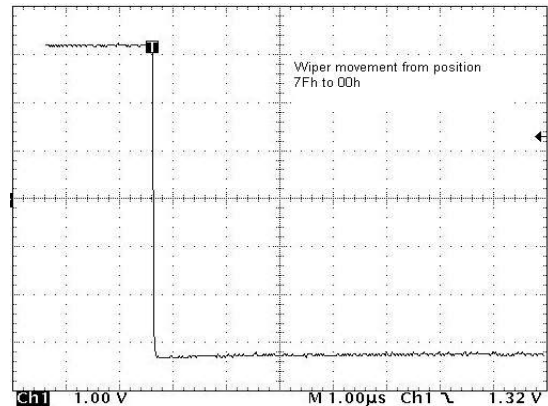


FIGURE 14. LARGE SIGNAL SETTLING TIME

### Principles of Operation

The ISL95711 is an integrated circuit incorporating one DCP with its associated register, non-volatile memory, and the I<sup>2</sup>C serial interface providing direct communication between a host and the potentiometer and memory. The resistor array is comprised of individual resistors connected in series. At either end of the array and between each resistor is an electronic switch that transfers the potential at that point to the wiper.

The wiper, when at either fixed terminal, acts like its mechanical equivalent and does not move beyond the last position. That is, the counter does not wrap around when clocked to either extreme.

The electronic switches on the device operate in a “make before break” mode when the wiper changes tap positions.

When the device is powered-down, the last value stored in the IVR will be maintained in the nonvolatile memory. When power is restored, the contents of the IVR are recalled and the wiper is set to that value.

The ISL95711 has dual supplies, V<sub>CC</sub> and V<sub>-</sub>. For proper operation of the chip, it is recommended both power supplies ramp up simultaneously to their final values within 20ms. The chip design gives priority to the V<sub>-</sub> supply stabilization and then looks at V<sub>CC</sub> stabilization. As the V<sub>-</sub> supply goes below -2.5V, the R<sub>W</sub> pin goes to the default code of 64. As V<sub>CC</sub> also exceeds 2.5V (after V<sub>-</sub> < -2.5V), the R<sub>W</sub> pin goes to the code stored in the EEPROM memory value (this is referred as power on recall).

### DCP Description

The DCP is implemented with a combination of resistor elements and CMOS switches. The physical ends of the DCP are equivalent to the fixed terminals of a mechanical potentiometer (R<sub>H</sub> and R<sub>L</sub> pins). The R<sub>W</sub> pin is connected to intermediate nodes, and is equivalent to the wiper terminal of a mechanical potentiometer. The position of the wiper terminal is controlled by a 7-bit volatile Wiper Register (WR). When the WR contains all zeroes (00h), the wiper terminal (R<sub>W</sub>) is closest to its “Low” terminal (R<sub>L</sub>). When the WR contains all ones (7Fh), the wiper terminal (R<sub>W</sub>) is closest to its “High” terminal (R<sub>H</sub>). As the value of the WR increases from all zeroes (00h) to all ones (7Fh), the wiper moves monotonically from the position closest to R<sub>L</sub> to the position closest to R<sub>H</sub>. At the same time, the resistance between R<sub>W</sub> and R<sub>L</sub> increases monotonically, while the resistance between R<sub>H</sub> and R<sub>W</sub> decreases monotonically.

While the ISL95711 is being powered up, the WR is reset to 40h (64 decimal), which locates the R<sub>W</sub> at the center between R<sub>L</sub> and R<sub>H</sub>. Soon after the power supply voltage becomes large enough for reliable non-volatile memory reading (~ ±2.5V), the ISL95711 reads the value stored on a non-volatile Initial Value Register (IVR) and loads it into the WR.

The WR and IVR can be read or written directly using the I<sup>2</sup>C serial interface as described in the following sections.

### Memory Description

The ISL95711 contains 1 non-volatile byte known as the Initial Value Register (IVR). It is accessed by the I<sup>2</sup>C interface operations with Address 00h. The IVR contains the value which is loaded into the Volatile Wiper Register (WR) at power-up.

The volatile WR, and the non-volatile IVR of a DCP are accessed with the same address.

The Access Control Register (ACR) determines which byte at address 00h is accessed (IVR or WR). The volatile ACR must be set as follows:

When the ACR is all zeroes, which is the default at power-up:

- A read operation to address 0 outputs the value of the non-volatile IVR.
- A write operation to address 0 writes the same value to the WR and IVR of the corresponding DCP.

When the ACR is 80h:

- A read operation to address 0 outputs the value of the volatile WR.
- A write operation to address 0 only writes to the corresponding volatile WR.

It is not possible to write to an IVR without writing the same value to its corresponding WR.

00h and 80h are the only values that should be written to address 2. All other values are reserved and must not be written to address 2.

TABLE 1. MEMORY MAP

ADDRESS	NON-VOLATILE	VOLATILE
2	-	ACR
1	Reserved	
0	IVR	WR

WR: Wiper Register, IVR: Initial value Register.

The ISL95711 is pre-programmed with 40h in the IVR.

## I<sup>2</sup>C Serial Interface

The ISL95711 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master always initiates data transfers and provides the clock for both transmit and receive operations. Therefore, the ISL95711 operates as a slave device in all applications.

All communication over the I<sup>2</sup>C interface is conducted by sending the MSB of each byte of data first.

### Protocol Conventions

Data states on the SDA line can change only during SCL LOW periods. SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions (See Figure 15). On power-up of the ISL95711 the SDA pin is in the input mode.

All I<sup>2</sup>C interface operations must begin with a START condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The ISL95711 continuously monitors the SDA

and SCL lines for the START condition and does not respond to any command until this condition is met (See Figure 15). A START condition is ignored during the power-up sequence and during internal non-volatile write cycles.

All I<sup>2</sup>C interface operations must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH (See Figure 15). A STOP condition at the end of a read operation, or at the end of a write operation to volatile bytes only places the device in its standby mode. A STOP condition during a write operation to a non-volatile byte, initiates an internal non-volatile write cycle. The device enters its standby state when the internal non-volatile write cycle is completed.

An ACK, Acknowledge, is a software convention used to indicate a successful data transfer. The transmitting device, either master or slave, releases the SDA bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data (See Figure 16).

The ISL95711 responds with an ACK after recognition of a START condition followed by a valid Identification Byte, and once again after successful receipt of an Address Byte. The ISL95711 also responds with an ACK after receiving a Data Byte of a write operation. The master must respond with an ACK after receiving a Data Byte of a read operation

A valid Identification Byte contains 01010 as the five MSBs, and the following two bits matching the logic values present at pins A1, and A0. The LSB is in the Read/Write bit. Its value is "1" for a Read operation, and "0" for a Write operation. (See Table 2.)

TABLE 2. IDENTIFICATION BYTE FORMAT

Logic values at pins A1, and A0 respectively

0	1	0	1	0	A1	A0	R/W
(MSB)							(LSB)

## Write Operation

A Write operation requires a START condition, followed by a valid Identification Byte, a valid Address Byte, a Data Byte, and a STOP condition. After each of the three bytes, the ISL95711 responds with an ACK. At this time, if the Data Byte is to be written only to volatile registers, then the device enters its standby state. If the Data Byte is to be written also to non-volatile memory, the ISL95711 begins its internal write cycle to non-volatile memory. During the internal non-volatile write cycle, the device ignores transitions at the SDA and SCL pins, and the SDA output is at a high impedance state. When the internal non-volatile write cycle is completed, the ISL95711 enters its standby state (See Figure 17).

The byte at address 02h determines if the Data Byte is to be written to volatile or both volatile and non-volatile. (See "Memory Description" on page 9.)

**Data Protection**

A STOP condition acts as a protection of non-volatile memory. A valid Identification Byte, Address Byte, and total number of SCL pulses act as a protection of both volatile and non-volatile registers. During a Write sequence, the Data Byte is loaded into an internal shift register as it is received. If the Address Byte is 0 or 2, the Data Byte is transferred to the Wiper Register (WR) or to the Access Control Register respectively, at the falling edge of the SCL pulse that loads the last bit (LSB) of the Data Byte. If the Address Byte is 0, and the Access Control Register is all zeros (default), then the STOP condition initiates the internal write cycle to non-volatile memory.

**Read Operation**

A Read operation consists of a three byte instruction followed by one or more Data Bytes (See Figure 18). The master initiates the operation issuing the following sequence: a START, the Identification byte with the  $R/\overline{W}$  bit set to "0", an Address Byte, a second START, and a second Identification byte with the  $R/\overline{W}$  bit set to "1". After each of the three bytes, the ISL95711 responds with an ACK; then the ISL95711 transmits the Data Byte. The master then terminates the read operation (issuing a STOP condition) following the last bit of the Data Byte (See Figure 18).

The byte at address 02h determines if the Data Bytes being read are from volatile or non-volatile memory. (See "Memory Description".)

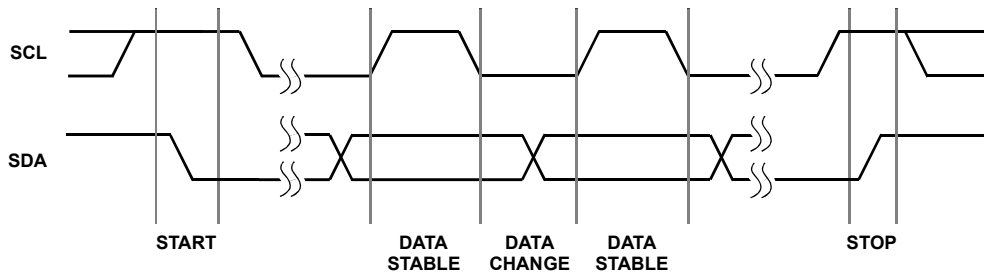


FIGURE 15. VALID DATA CHANGES, START, AND STOP CONDITIONS

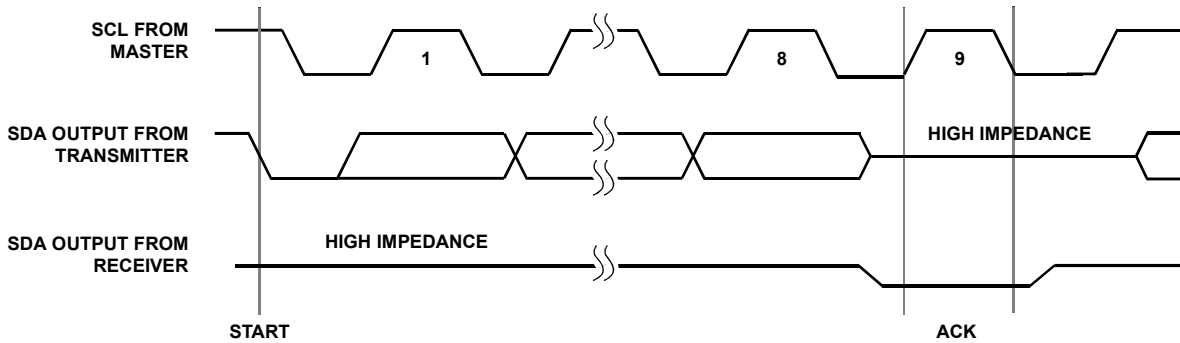


FIGURE 16. ACKNOWLEDGE RESPONSE FROM RECEIVER

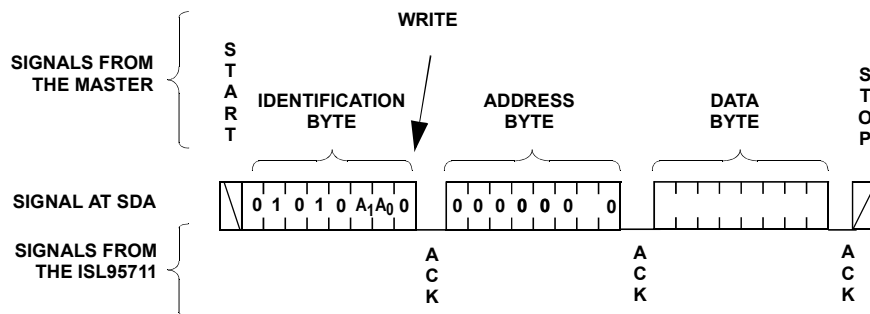


FIGURE 17. BYTE WRITE SEQUENCE

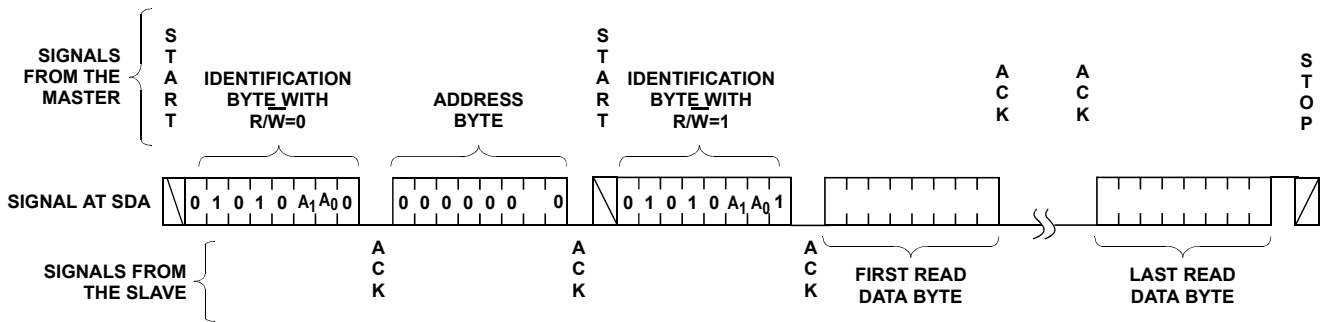


FIGURE 18. READ SEQUENCE

### Communicating with the ISL95711

There are 3 register addresses in the ISL95711, of which two can be used. Address 00h and address 02h are used to control the device. Address 01h is reserved and should not be used. Address 00h contains the non-volatile Initial Value Register (IVR), and the volatile Wiper Register (WR). Address 02h contains only a volatile word and is used as a pointer to either the IVR or WR. See Table 1.

#### Register Descriptions: Access Control

The Access Control Register (ACR) is volatile and is at address 02h. It is 8-bits, and only the MSB is significant, all other bits should be zero (0). The ACR controls which word is accessed at register 00h as follows:

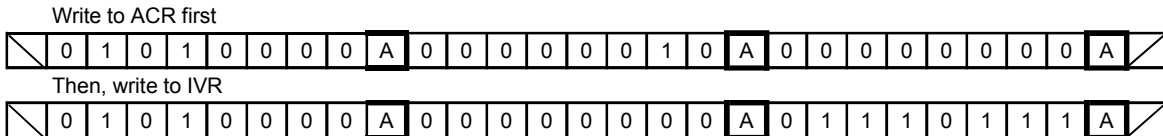
00h = Nonvolatile IVR

80h = Volatile WR

All other bits of the ACR should be written to as zeros. Only the MSB can be either 0 or 1. Power-up default for this address is 00h.

#### Example 1

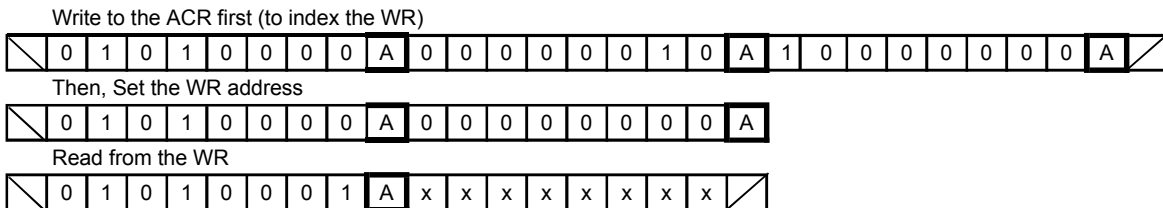
##### Writing a new value (77h) to the IVR:



NOTE: The WR will also reflect this new value since both registers get written to at the same time)

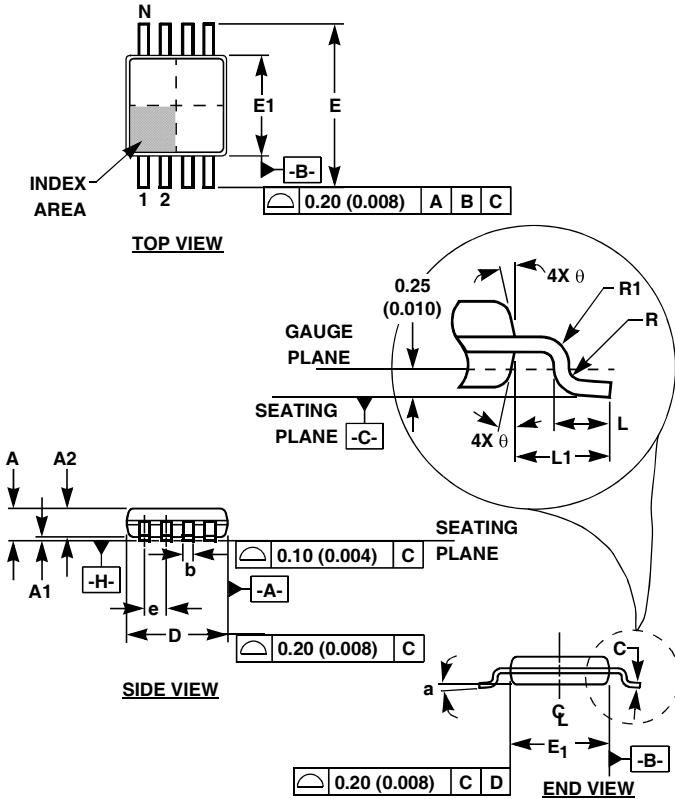
#### Example 2

##### Reading from the WR:



NOTE: A = acknowledge, x = data bit read

Mini Small Outline Plastic Packages (MSOP)



M10.118 (JEDEC MO-187BA)  
10 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.037	0.043	0.94	1.10	-
A1	0.002	0.006	0.05	0.15	-
A2	0.030	0.037	0.75	0.95	-
b	0.007	0.011	0.18	0.27	9
c	0.004	0.008	0.09	0.20	-
D	0.116	0.120	2.95	3.05	3
E1	0.116	0.120	2.95	3.05	4
e	0.020 BSC		0.50 BSC		-
E	0.187	0.199	4.75	5.05	-
L	0.016	0.028	0.40	0.70	6
L1	0.037 REF		0.95 REF		-
N	10		10		7
R	0.003	-	0.07	-	-
R1	0.003	-	0.07	-	-
θ	5°	15°	5°	15°	-
α	0°	6°	0°	6°	-

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NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-187BA.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.
3. Dimension "D" does not include mold flash, protrusions or gate burrs and are measured at Datum Plane. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension "E1" does not include interlead flash or protrusions and are measured at Datum Plane. [-H-] Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. Formed leads shall be planar with respect to one another within 0.10mm (.004) at seating Plane.
6. "L" is the length of terminal for soldering to a substrate.
7. "N" is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of "b" dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Datums [-A-] and [-B-] to be determined at Datum plane [-H-].
11. Controlling dimension: MILLIMETER. Converted inch dimensions are for reference only

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