

# Au5411 – 10 OUTPUT, DIFFERENTIAL, ULTRA LOW JITTER BUFFER

## General Description

The Au5411 is a 2.1 GHz, 10 output low-jitter clock fan-out buffer, intended to be used in low jitter, high frequency clock/data distribution and level translation.

The buffer can choose a clock input from primary, secondary or crystal source. The primary and secondary clock sources can be single ended or fully differential. The selected clock can be distributed to two output drive banks A, B and one LVCMOS output.

The crystal input can support crystals from 8 MHz to 50 MHz. It can also support single ended clock.

The output drivers of each bank can be independently programmed to LVPECL, LVDS, HCSL or HIZ mode. The LVCMOS clock output is synchronized to selected clock and can be enabled or disabled in a glitch free manner.

The Au5411 operates from a 3.3 V/2.5 V core supply and 3 independent 3.3 V/2.5 V output supplies. LVCMOS output driver can be operated at 1.8 V

- Features
- Additive jitter performance of 55 fs RMS.
- 3:1 input clock selection
- Two universal clock inputs can operate up to 2.1 GHz and accept LVPECL, LVDS, LVCMOS, CML(ac-coupled only), HCSL, SSTL or single ended clocks
- One crystal input which can support crystals in the frequency range of 8 MHz to 50 MHz or it can accept single ended input clock.
- Two output driver banks A and B which can be programmed independently to LVPECL, LVDS, HCSL or HIZ mode.
- Typical output skew between clock outputs is 30 ps
- Level translation with core supply voltage of 3.3 V/2.5 V and 3.3 V/2.5 V output supply for differential output drivers.
- 3.3 V/2.5 V/1.8 V operation for the single LVCMOS output driver
- The Au5411 buffer is pin controlled.
- High PSRR -70/-73 dBc for LVPECL/LVDS modes
- Au5411 buffer is available in a 48-pin,
- 7mm x 7mm WQFN package.

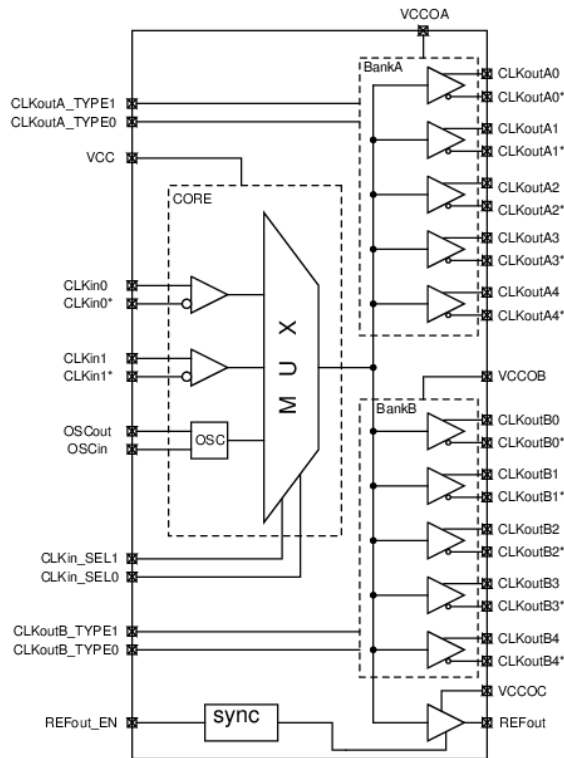


Figure 1 Functional Overview

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## 1 Detailed Pin Description

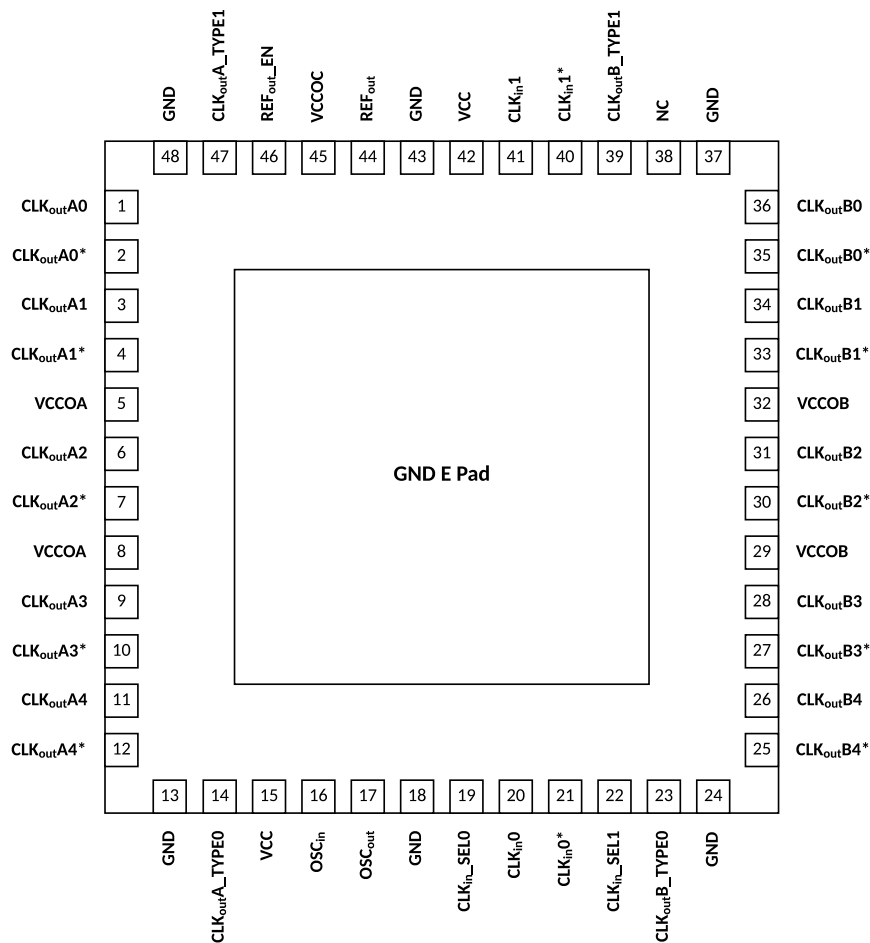


Figure 2 Au5411 Buffer, Differential Output Buffer Top View

Table 1 Detailed Pin Description

| Pin Name                            | Pin Number | Functionality Au5411   |
|-------------------------------------|------------|--|
| Pin group: Bank A clock output pads |            |  |
| CLKoutA0                            | 1          | Differential clock output P of A0. Output type set by CLKoutA_TYPE pins. |
| CLKoutA0*                           | 2          | Differential clock output N of A0. Output type set by CLKoutA_TYPE pins. |
| CLKoutA1                            | 3          | Differential clock output P of A1. Output type set by CLKoutA_TYPE pins. |
| CLKoutA1*                           | 4          | Differential clock output N of A1. Output type set by CLKoutA_TYPE pins. |
| CLKoutA2                            | 6          | Differential clock output P of A2. Output type set by CLKoutA_TYPE pins. |
| CLKoutA2*                           | 7          | Differential clock output N of A2. Output type set by CLKoutA_TYPE pins. |
| CLKoutA3                            | 9          | Differential clock output P of A3. Output type set by CLKoutA_TYPE pins. |
| CLKoutA3*                           | 10         | Differential clock output N of A3. Output type set by CLKoutA_TYPE pins. |
| CLKoutA4                            | 11         | Differential clock output P of A4. Output type set by CLKoutA_TYPE pins. |
| CLKoutA4*                           | 12         | Differential clock output N of A4. Output type set by CLKoutA_TYPE pins. |
| Pin group: Bank B clock output pads |            |  |
| CLKoutB0                            | 36         | Differential clock output P of B0. Output type set by CLKoutB_TYPE pins. |
| CLKoutB0*                           | 35         | Differential clock output N of B0. Output type set by CLKoutB_TYPE pins. |
| CLKoutB1                            | 34         | Differential clock output P of B1. Output type set by CLKoutB_TYPE pins. |
| CLKoutB1*                           | 33         | Differential clock output N of B1. Output type set by CLKoutB_TYPE pins. |
| CLKoutB2                            | 31         | Differential clock output P of B2. Output type set by CLKoutB_TYPE pins. |
| CLKoutB2*                           | 30         | Differential clock output N of B2. Output type set by CLKoutB_TYPE pins. |

| Pin Name                           | Pin Number | Functionality Au5411   |
|------------------------------------|------------|--|
| CLKoutB3                           | 28         | Differential clock output P of B3. Output type set by CLKoutB_TYPE pins.   |
| CLKoutB3*                          | 27         | Differential clock output N of B3. Output type set by CLKoutB_TYPE pins.   |
| CLKoutB4                           | 26         | Differential clock output P of B4. Output type set by CLKoutB_TYPE pins.   |
| CLKoutB4*                          | 25         | Differential clock output N of B4. Output type set by CLKoutB_TYPE pins.   |
| Pin group: Bank C clock output pad |            |  |
| REFout                             | 44         | LVC MOS clock out synchronized with differential clocks  |
| Pin group: Clock inputs            |            |  |
| CLKin0                             | 20         | Universal clock input 0 (+ve polarity) (differential/single-ended)   |
| CLKin0*                            | 21         | Universal clock input 0 (-ve polarity) (differential/single-ended)   |
| CLKin1                             | 41         | Universal clock input 1 (+ve polarity) (differential/single-ended)   |
| CLKin1*                            | 40         | Universal clock input 1 (-ve polarity) (differential/single-ended)   |
| OScin                              | 16         | Input for crystal. It can be over driven by an AC coupled single ended clock in crystal over drive mode.<br>In the external bypass mode, the max voltage at the pin needs to be 1.5V. If the driver is swinging to say 3.3V rail, then a resistor divider is needed on PCB to restrict the swing at Oscin to 1.5V<br>Load supported 6pF to 10pF, freq 8MHz to 50 MHz |
| OScout                             | 17         | Output for crystal. Leave OSCout floating if OSCin is driven by a single-ended clock.  |
| Pin group: Power pins              |            |  |
| VCC                                | 15         | Line supply - 3.3V/2.5V  |
| VCC                                | 42         | Line supply - 3.3V/2.5V  |
| VCCOA                              | 5          | Power supply for Bank A Output buffers. VCCOA can operate from 3.3 V or 2.5 V  |
| VCCOA                              | 8          | Power supply for Bank A Output buffers. VCCOA can operate from 3.3 V or 2.5 V  |
| VCCOB                              | 32         | Power supply for Bank B Output buffers. VCCOB can operate from 3.3 V or 2.5 V  |
| VCCOB                              | 29         | Power supply for Bank B Output buffers. VCCOB can operate from 3.3 V or 2.5 V  |
| VCCOC                              | 45         | Power supply for Bank C Output buffer. VCCOC can operate from 3.3 V or 2.5 V or 1.8 V  |
| GND-EPAD                           | 0          | Ground   |
| GND                                | 13         | ground pin   |
| GND                                | 18         | ground pin   |
| GND                                | 24         | ground pin   |
| GND                                | 37         | ground pin   |
| GND                                | 48         | ground pin   |
| GND                                | 43         | ground pin   |
| Pin group: Control pins            |            |  |
| CLKoutA_Type0                      | 14         | Bank A output buffer type selection pins   |
| CLKoutA_Type1                      | 47         | Bank A output buffer type selection pins   |
| CLKoutB_Type0                      | 23         | Bank B output buffer type selection pins   |
| CLKoutB_Type1                      | 39         | Bank B output buffer type selection pins   |
| REFout_EN                          | 46         | REFout enable input. Enable signal is internally synchronized to selected clock input.   |
| CLKin_SEL0                         | 19         | Clock input selection pins   |
| CLKin_SEL1                         | 22         | Clock input selection pins   |
| NC                                 | 38         | no connect   |



## 2 Electrical Characteristics

**Table 2 Absolute Maximum Ratings**

| Parameters                            | Conditions | Symbol           | Min  | Typ | Max | Units |
|---------------------------------------|------------|------------------|------|-----|-----|-------|
| Core supply voltage, Analog Input     |            | V <sub>CC</sub>  | -0.3 |     | 3.6 | V     |
| Output bank supply voltage            |            | V <sub>CCO</sub> | -0.3 |     | 3.6 | V     |
| Input voltage, All Inputs, except XIN |            | V <sub>IN</sub>  | -0.3 |     | 3.6 | V     |
| XIN                                   |            | V <sub>IN</sub>  | -0.3 |     | 1.5 | V     |
| Storage temperature                   |            | TS               | -55  |     | 150 | °C    |

Notes:

- Exceeding maximum ratings may shorten the useful life of the device.
- Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or at any other conditions beyond those indicated under the DC Electrical Characteristics is not implied. Exposure to Absolute-Maximum-Rated conditions for extended periods may affect device reliability or cause permanent device damage.

**Table 3 Recommended Operating Supply and Temperatures**

| Parameters                              | Conditions | Symbol               | Min   | Typ | Max   | Units |
|---|------------|----------------------|-------|-----|-------|-------|
| Core supply voltage                     |            | V <sub>CC</sub>      | 3.135 | 3.3 | 3.45  | V     |
|   |            | V <sub>CC</sub>      | 2.375 | 2.5 | 2.625 | V     |
| Output supply voltage                   |            | V <sub>CCO</sub> A/B | 3.135 | 3.3 | 3.45  | V     |
|   |            | V <sub>CCO</sub> A/B | 2.375 | 2.5 | 2.625 | V     |
| Output supply voltage for LVCMOS driver |            | V <sub>CCOC</sub>    | 3.135 | 3.3 | 3.45  | V     |
| Output supply voltage                   |            | V <sub>CCOC</sub>    | 2.375 | 2.5 | 2.625 | V     |
| Output supply voltage                   |            | V <sub>CCOC</sub>    | 1.71  | 1.8 | 1.89  | V     |
| Ambient Temperature                     |            | TA                   | -40   |     | 85    | °C    |
| Junction Temperature                    |            | TJ                   |       |     | 125   | °C    |

**Table 4 Electrical Characteristics**

Unless otherwise specified: V<sub>CC</sub> = 3.3 V ± 5%, 2.5 V ± 5%, V<sub>CCO</sub> = 3.3 V ± 5%, 2.5 V ± 5%, -40 °C ≤ TA ≤ 85 °C, CLKIN0/1 driven differentially, input slew rate ≥ 3 V/ns. Typical values represent most likely parametric norms at V<sub>CC</sub> = 3.3 V, V<sub>CCO</sub> = 3.3 V, TA = 25 °C.

| Parameters   | Conditions  | Symbol                                | Min | Typ  | Max  | Units |
|--|---|---------------------------------------|-----|------|------|-------|
| <b>Current Consumption</b>   |   |                                       |     |      |      |       |
| Core supply current when input buffer is selected  | CLKIN0/1 selected, V <sub>CC</sub> = 3.3 V/2.5 V ± 5%, V <sub>CC</sub> = V <sub>CCO</sub> | I <sub>CC_CORE</sub>                  |     | 16.5 | 19.8 | mA    |
| Core supply current when Crystal is selected   | XO selected, V <sub>CC</sub> = 3.3 V/2.5 V ± 5%, V <sub>CC</sub> = V <sub>CCO</sub>       | I <sub>CORE_XO</sub> <sup>(4)</sup>   |     |      | 14   | mA    |
| Increment in core supply when all ODR banks are enabled                                  |   | I <sub>CC_ODR_EN</sub>                |     |      | 2    | mA    |
| Frequency dependent current both bank on core supply. This current scales with frequency | For F <sub>in</sub> = 2100 MHz  | I <sub>CC_DYN</sub> <sup>(1)(4)</sup> |     | 25   | 33   | mA    |
| Additive output supply current per LVPECL bank enabled                                   |   | I <sub>CCO_PECL</sub>                 |     | 165  | 204  | mA    |

| Parameters   | Conditions   | Symbol                 | Min                 | Typ   | Max                 | Units |
|--|--|------------------------|---------------------|-------|---------------------|-------|
| Additive output supply current per LVDS bank enabled       |  | I <sub>CCO_LVDS</sub>  |                     | 40    | 49                  | mA    |
| Additive output supply current per HCSL bank enabled       |  | I <sub>CCO_HCSL</sub>  |                     | 110   | 138                 | mA    |
| Additive output supply current, LVCMOS Output Enabled      | F <sub>IN</sub> = 200 MHz,<br>C <sub>LOAD</sub> = 5 pF,<br>V <sub>CCO</sub> = 3.3 V            | I <sub>CCO_CMOS</sub>  |                     | 6     | 7.2                 | mA    |
|  | F <sub>IN</sub> = 200 MHz,<br>C <sub>LOAD</sub> = 5 pF,<br>V <sub>CCO</sub> = 2.5 V            |                        |                     | 4.5   | 5.5                 | mA    |
| <b>Power Supply Rejection Ratio</b>                        |  |                        |                     |       |                     |       |
| Ripple induced phase spur level, supply ripple of 100mV pp | F <sub>in</sub> = 156.25 MHz,<br>F <sub>offset</sub> = 100 KHz<br>V <sub>CCO</sub> A/B = 2.5 V | PSRR <sub>PECL</sub>   |                     | -67   |                     | dBc   |
| Ripple induced phase spur level, supply ripple of 100mV pp | F <sub>in</sub> = 156.25 MHz,<br>F <sub>offset</sub> = 100 KHz<br>V <sub>CCO</sub> A/B=2.5 V   | PSRR <sub>LVDS</sub>   |                     | -70   |                     | dBc   |
| Ripple induced phase spur level, supply ripple of 100mV pp | F <sub>in</sub> = 156.25 MHz,<br>F <sub>offset</sub> = 100 KHz<br>V <sub>CCO</sub> A/B = 2.5 V | PSRR <sub>HCSL</sub>   |                     | -67.7 |                     | dBc   |
| Input High Current   | V <sub>CC</sub> = 3.3V, V <sub>IH</sub> = V <sub>CC</sub>                                      | I <sub>IH</sub>        |                     | 30    | 50                  | μA    |
| <b>Input Control Pin Characteristic</b>                    |  |                        |                     |       |                     |       |
| Input Low Current  |  | I <sub>IL</sub>        | -20                 | 0.1   |                     | μA    |
| Input high voltage – Logic inputs                          |  | V <sub>IH</sub>        | 0.7*V <sub>CC</sub> |       | V <sub>CC</sub>     | V     |
| Input low voltage – Logic inputs                           |  | V <sub>IL</sub>        | GND                 |       | 0.3*V <sub>CC</sub> | V     |
| Internal Pull-down resistance                              |  | R <sub>pull-down</sub> |                     | 200   |                     | K Ω   |

**Notes:**

- Total current from core supply at frequency F<sub>in</sub> = I<sub>CORE, STATIC</sub> + N\*(0.5\*F<sub>in</sub>/2100M)\* I<sub>CORE, DYN</sub>. Detailed methodology of calculating the power dissipated in each ODR mode is given in the section “Current consumption and Power Dissipation Calculations.” N is the number of output banks enabled.
- Refer to [Section 4.1](#) for more information on current consumption and power dissipation calculations.
- Power supply ripple rejection, or PSRR, is defined as the single-sideband phase spur level (in dBc) modulated onto the clock output when a single-tone sinusoidal signal (ripple) is injected onto the V<sub>cco</sub> supply. Assuming no amplitude modulation effects and small index modulation, the peak-to-peak deterministic jitter (DJ) can be calculated using the measured single-sideband phase spur level (PSRR) as follows: DJ (ps pk-pk) = [ (2 \* 10(PSRR / 20)) / (π \* f<sub>CLK</sub>) ] \* 1E<sup>12</sup>
- Specification is ensured by characterization and is not tested in production.

**Table 5 Input Clock Characteristics**

Unless otherwise specified:  $V_{CC} = 3.3\text{ V} \pm 5\%$ ,  $2.5\text{ V} \pm 5\%$ ,  $V_{CC0} = 3.3\text{ V} \pm 5\%$ ,  $2.5\text{ V} \pm 5\%$ ,  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , CLKIn0/1 driven differentially, input slew rate  $\geq 3\text{ V/ns}$ . Typical values represent most likely parametric norms at  $V_{CC} = 3.3\text{ V}$ ,  $V_{CC0} = 3.3\text{ V}$ ,  $T_A = 25\text{ }^{\circ}\text{C}$ .

| Parameters   | Conditions  | Symbol            | Min  | Typ               | Max     | Units         |
|--|---|-------------------|------|-------------------|---------|---------------|
| <b>Characteristics of Universal Input Clock Pins</b> |   |                   |      |                   |         |               |
| Input frequency range <sup>(4)</sup>                 |   | $F_{CLKin}^{(1)}$ | DC   |                   | 2100    | MHz           |
| Differential input high voltage                      | CLKin driven differentially                             | $V_{IHD}$         |      |                   | VCC     | V             |
| Differential input low voltage                       |   | $V_{ILD}$         | GND  |                   |         | V             |
| Peak differential input voltage swing <sup>(2)</sup> |   | $V_{ID}$          | 0.15 |                   | 1.3     | V             |
| Differential input common mode voltage               | Input differential swing of 150 mV                      | $V_{CMD}$         | 0.25 |                   | VCC-1.2 | V             |
|  | Input differential swing of 350 mV                      |                   | 0.25 |                   | VCC-1.1 | V             |
|  | Input differential swing of 800 mV                      |                   | 0.25 |                   | VCC-0.9 | V             |
| Single ended input high voltage                      | Inverting differential input held at VCC/2, VCC = 3.3 V | $V_{IH}$          | 2    |                   | VCC     | V             |
|  | Inverting differential input held at VCC/2, VCC = 2.5 V |                   | 1.6  |                   | VCC     |               |
| Single ended input low voltage                       | Inverting differential input held at VCC/2, VCC = 3.3 V | $V_{IL}$          | GND  |                   | 1.3     | V             |
|  | Inverting differential input held at VCC/2, VCC = 2.5 V |                   | GND  |                   | 0.9     |               |
| Single ended input voltage swing <sup>(3)</sup>      |   | $V_{LSE}$         | 0.3  |                   | 2       | VPP           |
| Single ended input common mode voltage               |   | $V_{CM}$          | 0.25 |                   | VCC-1.2 | V             |
| Mux Isolation between the two input clock paths      | $F_{in} = 100\text{ MHz}$ ,<br>Foffset > 50 KHz         | $ISO_{MUX}^{(1)}$ |      | -84               |         | dBc           |
|  | $F_{in} = 200\text{ MHz}$ ,<br>Foffset > 50 KHz         |                   |      | -82               |         | dBc           |
|  | $F_{in} = 500\text{ MHz}$ ,<br>Foffset > 50 KHz         |                   |      | -71               |         | dBc           |
|  | $F_{in} = 1000\text{ MHz}$ ,<br>Foffset > 50 KHz        |                   |      | -65               |         | dBc           |
| <b>Crystal Characteristics</b>                       |   |                   |      |                   |         |               |
| Equivalent series resistance                         |   | ESR               |      | 35                | 60      | $\Omega$      |
| Load capacitance                                     |   | CL                | 6    | 8                 | 10      | pF            |
| Shunt Capacitance                                    |   | Co                |      | 2                 | 3       | pF            |
| Power dissipated in the crystal                      |   | Drive level       |      | 100               | 200     | $\mu\text{W}$ |
| Mode of oscillation                                  |   |                   |      | Funda--<br>mental |         |               |
| Crystal frequency range                              |   | $F_{XTAL}^{(1)}$  | 8    |                   | 50      | MHz           |

| Parameters                                | Conditions   | Symbol          | Min | Typ | Max | Units |
|---|--|-----------------|-----|-----|-----|-------|
| External clock frequency range            | XO over drive or Bypass mode   | $F_{CLK}$       |     |     | 250 | MHz   |
| Maximum swing level on OSCin/OSCoout pins | XO over drive or Bypass mode   | $V_{max}$       |     |     | 1.5 | V     |
| Additive jitter <sup>(3)</sup>            | RMS, integration BW 12 KHz to 5 MHz, $F_{crystal} = 25$ MHz. Crystal input select Measured at $VDD = VDDO = 2.5$ V | $t_{jit}^{(1)}$ |     | 155 |     | fs    |

Notes:

1. Specification is ensured by characterization and is not tested in production.
2. Refer to [Section 7](#) for definition of VID and VOD voltages.
3. For clock input frequency  $\geq 100$  MHz, CLKinX can be driven with single-ended (LVCMOS) input swing up to 3.3 Vpp. For clock input frequency  $< 100$  MHz, the single-ended input swing should be limited to 2 Vpp max to prevent input saturation (refer to Driving the Clock Inputs for interfacing 2.5 V/3.3 V LVCMOS clock input  $< 100$  MHz to CLKinX).
4. If the input clock is initially absent when the chip is just powered up, it will take atleast 2 falling edge of clock cycles for the output to appear. Therefore, the buffer level translates DC only after it sees two consecutive falling edge of input clock

**Table 6 Output Clock Characteristics – LVPECL**

Unless otherwise specified:  $V_{cc} = 3.3$  V  $\pm 5\%$ ,  $2.5$  V  $\pm 5\%$ ,  $V_{cco} = 3.3$  V  $\pm 5\%$ ,  $2.5$  V  $\pm 5\%$ ,  $-40$  °C  $\leq T_A \leq 85$  °C, CLKin0/1 driven differentially, input slew rate  $\geq 3$  V/ns. Typical values represent most likely parametric norms at  $V_{cc} = 3.3$  V,  $V_{cco} = 3.3$  V,  $T_A = 25$  °C. Termination is 50  $\Omega$  to VCCO -2V

| Parameters  | Condition   | Symbol                | Min               | Typ  | Max              | Unit |
|---|---|-----------------------|-------------------|------|------------------|------|
| <b>LVPECL</b>   |   |                       |                   |      |                  |      |
| Maximum output frequency, full VOD swing $\geq 600$ mV <sup>(1)</sup> | 50 $\Omega$ termination biased with VCCO -2V  | $F_{CLKOUT\_F}^{(1)}$ | 1000              | 1200 | -                | MHz  |
| Maximum output frequency, full VOD swing $\geq 400$ mV <sup>(1)</sup> |   |                       | 1500              | 2100 |                  | MHz  |
| Additive RMS jitter <sup>(1)</sup>                                    | Integration bandwidth from 10 KHz to 20 MHz, $F_{IN} = 156.25$ MHz, $SR > 3$ V/ns<br>50 $\Omega$ termination biased with VCCO -2V | $Jitter_{ADD}^{(1)}$  |                   | 55   |                  | fs   |
| Noise floor for Foffset $> 10$ MHz                                    | 50 $\Omega$ termination biased with VCCO -2V, $F_{IN} = 156.25$ MHz, $SR > 3$ V/ns  | $Noise_{FLOOR}^{(1)}$ |                   | -159 |                  | dBc  |
| Output Duty Cycle   | 50 $\Omega$ termination biased with VCCO -2V  | ODC                   | 45                |      | 55               | %    |
| Output high voltage   | 50 $\Omega$ termination biased with VCCO -2V  | $V_{OH}$              | $V_{CCO} - 1.165$ |      | $V_{CCO} - 0.75$ | V    |
| Differential output voltage   | 50 $\Omega$ termination biased with VCCO -2V  | $V_{OD}$              | 475               | 678  | 960              | mV   |
| Output low voltage  | 50 $\Omega$ termination biased with VCCO -2V  | $V_{OL}$              | $V_{CCO} - 2.0$   |      | $V_{CCO} - 1.45$ | V    |
| Output rise time, 20% to 80%  | 50 $\Omega$ termination biased with VCCO -2V  | $t_R$                 |                   | 210  | 350              | ps   |
| Output fall time 20% to 80%   | 50 $\Omega$ termination biased with VCCO -2V  | $t_F$                 |                   | 210  | 350              | ps   |
| Input to output delay   | 50 $\Omega$ termination biased with VCCO -2V  | $t_{pd}$              |                   | 876  | 1100             | ps   |

Notes:

1. Specification is guaranteed by characterization and is not tested in production

**Table 7 Output Clock Characteristics - LVDS**

Unless otherwise specified:  $V_{CC} = 3.3\text{ V} \pm 5\%$ ,  $2.5\text{ V} \pm 5\%$ ,  $V_{CCO} = 3.3\text{ V} \pm 5\%$ ,  $2.5\text{ V} \pm 5\%$ ,  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , CLKin0/1 driven differentially, input slew rate  $\geq 3\text{ V/ns}$ . Typical values represent most likely parametric norms at  $V_{CC} = 3.3\text{ V}$ ,  $V_{CCO} = 3.3\text{ V}$ ,  $T_A = 25\text{ }^{\circ}\text{C}$ .

| Parameters  | Conditions   | Symbol                        | Min   | Typ  | Max   | Units  |
|---|--|-------------------------------|-------|------|-------|--------|
| <b>LVDS</b>   |  |                               |       |      |       |        |
| Maximum output frequency, full VOD swing $\geq 250\text{ mV}$ | $R_L = 100\ \Omega$ , differential   | $F_{\text{CLKOUT\_FS}}^{(1)}$ | 1000  | 1600 | -     | MHz    |
| Maximum output frequency, full VOD swing $\geq 200\text{ mV}$ | $R_L = 100\ \Omega$ , differential   |                               | 1500  | 2100 |       | MHz    |
| Additive RMS jitter   | Integration bandwidth from 10 KHz to 20 MHz,<br>$F_{\text{in}} = 156.25\text{ MHz}$ ,<br>$\text{SR} > 3\text{ V/ns}$<br>$R_L = 100\ \Omega$ , differential | $\text{Jitter}_{\text{ADD}}$  |       | 60   |       | fs rms |
| Noise floor for Foffset $> 10\text{ MHz}$                     | $F_{\text{in}} = 156.25\text{ MHz}$ ,<br>$\text{SR} > 3\text{ V/ns}$<br>$R_L = 100\ \Omega$ , differential   | $\text{Noise}_{\text{FLOOR}}$ |       | -159 |       | dBc    |
| Output Duty Cycle   | $R_L = 100\ \Omega$ , differential   | ODC                           | 45    |      | 55    | %      |
| Change in VPP between complementary output states             | $R_L = 100\ \Omega$ , differential   | $\Delta\text{VPP}$            |       |      | 50    | mV     |
| Output differential peak voltage                              | $R_L = 100\ \Omega$ , differential   | $V_{\text{OD}}$               | 247   |      | 454   | mV     |
| Output Common-Mode Voltage                                    | $R_L = 100\ \Omega$ , differential   | $V_{\text{OCM}}$              | 1.125 | 1.2  | 1.375 | V      |
| Output rise time, 20% to 80%                                  | $R_L = 100\ \Omega$ , differential,<br>$C_L < 5\text{ pF}$   | $t_r$                         |       | 210  | 350   | ps     |
| Output fall time 20% to 80%                                   | Uniform transmission line up to 10 inches with characteristic impedance of $50\ \Omega$  | $t_f$                         |       | 210  | 350   | ps     |
| Input to output delay   |  | $t_{\text{pd}}$               |       | 840  | 1100  | ps     |
| Skew between outputs  | $V_{\text{CCO}} = 3.3\text{ V}, 2.5\text{ V}$  | $T_{\text{sk}}$               |       | 30   |       | ps     |

Notes:

1. Specification is ensured by characterization and is not tested in production.

**Table 8 Output Clock Characteristics - HCSL**

| Parameters               | Conditions                                   | Symbol                             | Min | Typ | Max | Units  |
|--------------------------|--|------------------------------------|-----|-----|-----|--------|
| <b>HCSL</b>              |  |                                    |     |     |     |        |
| Maximum output frequency | $R_L = 50\ \Omega$ to GND                    | $F_{\text{CLKOUT\_F}}^1$           | DC  |     | 700 | MHz    |
| Additive RMS jitter      | Integration bandwidth from 10 KHz to 20 MHz, | $\text{Jitter}_{\text{ADD}}^{(1)}$ |     | 55  |     | fs rms |

| Parameters   | Conditions  | Symbol                                | Min  | Typ  | Max  | Units |
|--|---|---------------------------------------|------|------|------|-------|
| Noise floor for Foffset > 10 MHz                     | $F_{IN} = 156.25$ MHz,<br>SR > 3 V/ns<br>$R_L = 50 \Omega$ to GND   | Noise <sub>FLOOR</sub> <sup>(1)</sup> |      | -159 |      | dBc   |
| Output Duty Cycle                                    |   | ODC                                   | 45   |      | 55   | %     |
| Output Low Voltage Min                               |   | $V_{MIN}$                             | -300 |      |      | mV    |
| Differential Output High Voltage                     | $R_L = 50 \Omega$ to GND  | $V_{OH}$                              | 600  | 840  | 1150 | mV    |
| Differential Output Low Voltage                      |   | $V_{OL}$                              | -150 | 28   | 150  | mV    |
| Absolute Crossing point voltage                      | $R_L = 50 \Omega$ to GND,<br>$C_L < 5$ pF   | $V_{CROSS}$                           | 250  |      | 550  | mV    |
| Variation of $V_{CROSS}$ over all rising clock edges |   | $V_{CROSS}$<br>DELTA                  |      |      | 140  | mV    |
| Output rise time, 20% to 80%                         | $F_{IN} = 156.25$ MHz,<br>Uniform transmission line up to 10 inches with characteristic impedance of $50 \Omega$<br>$R_L = 50 \Omega$ to GND,<br>$C_L < 5$ pF | $t_R$                                 |      | 210  | 500  | ps    |
| Output fall time 20% to 80%                          |   | $t_F$                                 |      | 210  | 500  | ps    |
| Input to output delay                                |   | $t_{pd}$                              |      | 825  | 1100 | ps    |

Notes:

1. Specification is ensured by characterization and is not tested in production.

**Table 9 Output Clock Characteristics – LVCMOS**

 Unless otherwise specified:  $V_{CC} = 3.3$  V  $\pm$  5%,  $V_{CCO} = 3.3$  V  $\pm$  5%, 2.5 V  $\pm$  5%,  $-40 \text{ }^\circ\text{C} \leq T_A \leq 85 \text{ }^\circ\text{C}$ , CLKIn0/1 driven differentially, input slew rate  $\geq 3$  V/ns. Typical values represent most likely parametric norms at  $V_{CC} = 3.3$  V,  $V_{CCO} = 3.3$  V,  $T_A = 25 \text{ }^\circ\text{C}$ .

| Parameters                                | Conditions  | Symbol                                | Min               | Typ  | Max | Units  |
|---|---|---------------------------------------|-------------------|------|-----|--------|
| Output Frequency                          |   | $f_{CLKOUT}$                          | 0                 |      | 250 | MHz    |
| Additive RMS jitter                       | $V_{CCO} = 3.3$ V $\pm$ 5%                              | Jitter <sub>ADD</sub> <sup>(1)</sup>  |                   | 55   |     | fs rms |
|   | $V_{CCO} = 2.5$ V $\pm$ 5%                              |                                       |                   | 63   |     | fs rms |
| Noise floor for Foffset > 10 MHz<br>VCCOC | $V_{CCO} = 3.3$ V $\pm$ 5%                              | Noise <sub>FLOOR</sub> <sup>(1)</sup> |                   | -159 |     | dBc    |
|   | $V_{CCO} = 2.5$ V $\pm$ 5%                              |                                       |                   | -157 |     | dBc    |
| Output Duty Cycle                         | For $F_{IN} \leq 200$ MHz                               | ODC                                   | 45                |      | 55  | %      |
|   | For $200 \text{ MHz} < F_{IN} < 250$ MHz                |                                       | 40                |      | 60  | %      |
| Output high voltage                       | $V_{CCO} = 3.3$ V $\pm$ 5%,<br>1 mA pull down current   | $V_{OH}$                              | $V_{CCO} - 0.1$ V |      |     | V      |
|   | $V_{CCO} = 2.5$ V $\pm$ 5%,<br>1 mA pull down current   |                                       | $V_{CCO} - 0.1$ V |      |     | V      |
| Output low voltage                        | $V_{CCO} = 3.3$ V $\pm$ 5%,<br>1 mA pull up current     | $V_{OL}$                              |                   |      | 0.1 | V      |
|   | $V_{CCO} = 2.5$ V $\pm$ 5%,<br>1 mA pull up current     |                                       |                   |      | 0.1 | V      |
| Output rise time, 20% to 80%              | $C_{LOAD} = 5$ pF, $R_{LOAD} = 50 \Omega$<br>AC coupled | $t_R$                                 |                   | 250  | 450 | ps     |

| Parameters                                     | Conditions  | Symbol          | Min | Typ | Max | Units  |
|--|---|-----------------|-----|-----|-----|--------|
| Output fall time 20% to 80%                    |   | $t_F$           |     | 250 | 450 | ps     |
| Output enable time                             |   | $t_{EN}^{(1)}$  |     |     | 4   | cycles |
| Output disable time                            |   | $t_{DIS}^{(1)}$ |     |     | 4   | cycles |
| Input to clock edge to output clock edge delay | VDDO = 3.3 V, PCB trace of 5 inch, 5 pF capacitor | $t_d^{(1)}$     |     | 1.4 | 2.5 | ns     |
|  | VDDO = 2.5 V, PCB trace of 5 inch, 5 pF capacitor |                 |     | 1.5 | 2.7 | ns     |

## Notes:

1. Specification is ensured by characterization and is not tested in production.

### 3 Functional Description

The Au5411 is a 10-output differential clock fan out buffer with low additive jitter that can operate up to 2.1 GHz. It features a 3:1 input multiplexer with an optional crystal oscillator input, two banks of 5 differential outputs with multi-mode buffers (LVPECL, LVDS, HCSL, or Hi-Z), one LVCMOS output, and 3 independent output buffer supplies. The input selection and output buffer modes are controlled via pin strapping. The device is offered in a 48-pin WQFN package.

#### 3.1 V<sub>CC</sub> and V<sub>CCO</sub> Power Supplies

The Au5411 has separate 3.3/2.5 core (V<sub>CC</sub>) and 3 independent 3.3 V/2.5 V output power supplies (V<sub>CCOA</sub>, V<sub>CCOB</sub>) V<sub>CCOC</sub> supply can operate on 3.3 V/2.5 V/1.8 V rail. Output supply operation at 2.5 V enables lower power consumption and output-level compatibility with 2.5 V receiver devices. The output levels for LVPECL (V<sub>OH</sub>, V<sub>OL</sub>) and LVCMOS (V<sub>OH</sub>) are referenced to its respective V<sub>CCO</sub> supply, while the output levels for LVDS and HCSL are relatively constant over the specified V<sub>CCO</sub> range.

#### 3.2 Clock Inputs

The input clock can be selected from CLKin0/CLKin0\*, CLKin1/CLKin1\*, or OSCin. Clock input selection is controlled using the CLKin\_SEL[1:0] inputs as shown in Table 10. When CLKin0 or CLKin1 are selected, the oscillator is power down. The user can float OSCin and OSCout pins, since these pins are internally pulled down. OSCin is pulled down with a 56 KΩ resistance.

Table 10 Input Clock Selection

| CLKin_SEL[1] | CLKin_SEL[0] | Selected Clock                            |
|--------------|--------------|---|
| 0            | 0            | CLKin0, CLKin0*                           |
| 0            | 1            | CLKin1, CLKin1*                           |
| 1            | 0            | Crystal Or Crystal Bypass AC Coupled mode |
| 1            | 1            | Crystal bypass DC Coupled mode            |

#### 3.3 Clock States (Input vs Output States)

Table 11 Input versus Output Stages

| State of Selected Clock input | Output State |
|-------------------------------|--------------|
| Inputs are floating           | Logic low    |
| Inputs are logic low          | Logic low    |
| Inputs are logic high         | Logic high   |

#### 3.4 Output Driver Type

The differential output buffer type for Bank A and Bank B outputs can be separately configured using the CLKoutA\_TYPE[1:0] and CLKoutB\_TYPE[1:0] inputs, respectively, as shown Table 12. For applications where all differential outputs are not needed, any unused output pin should be left floating with a minimum copper length to minimize capacitance and potential coupling and reduce power consumption. If an entire output bank will not be used, it is recommended to disable (Hi-Z) the bank to reduce power.

Table 12 OE Functionality

| CLKOUTX_TYPE1 | CLKOUTX_TYPE0 | CLK Buffer Type |
|---------------|---------------|-----------------|
| 0             | 0             | LVPECL          |
| 0             | 1             | LVDS            |
| 1             | 0             | HCSL            |
| 1             | 1             | HIZ             |



### 3.5 Reference Output

The reference output (REFout) provides a LVCMOS copy of the selected input clock. The LVCMOS output high level is referenced to the VCCOC voltage. REFout can be enabled or disabled using the enable input pin, REFout\_EN, as shown in Table 13. The reference output clock is internally synchronized to the selected clock. This avoids any glitches or runt pulses while enabling or disabling the reference clock. Pulling REFout\_EN to LOW, forces the outputs to the high-impedance state with in 4 falling edges of the input signal. The outputs remain in the high-impedance state as long as REFout\_EN is LOW. When REFout\_EN goes from HIGH to LOW, the output clock is enabled with in 4 falling edges of the input clock signal. The output is enabled at the falling edge of the input clock. This allows to enable the output clock in a glitch free manner.

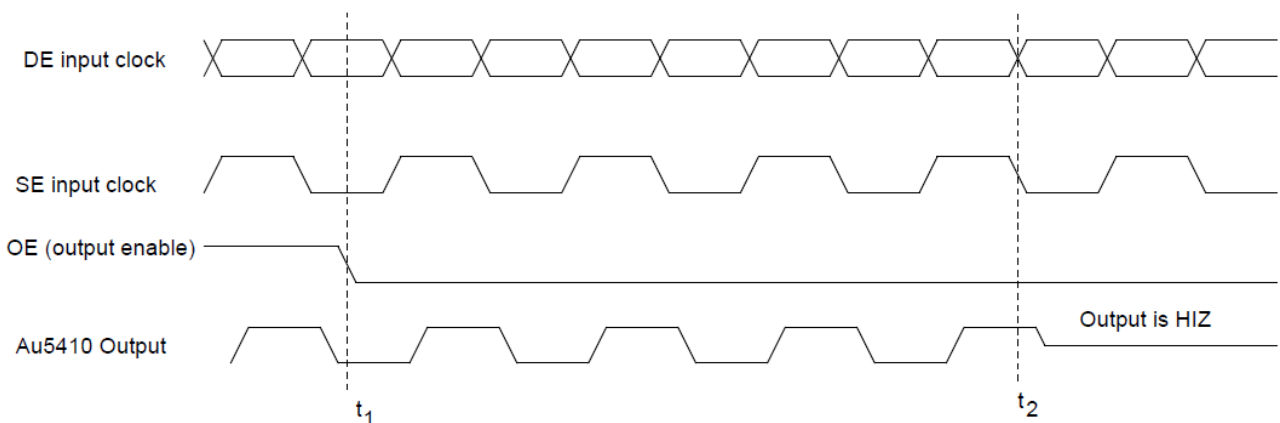
When REFout\_EN goes from low to high, the output clock is enabled within a time delay  $t_d$ , where  $t_d$  is given by the following equation.

$$t_{d,refout\_en} = 0.5n + 3 * T_{in}. T_{in} \text{ is the time period of the input clock.}$$

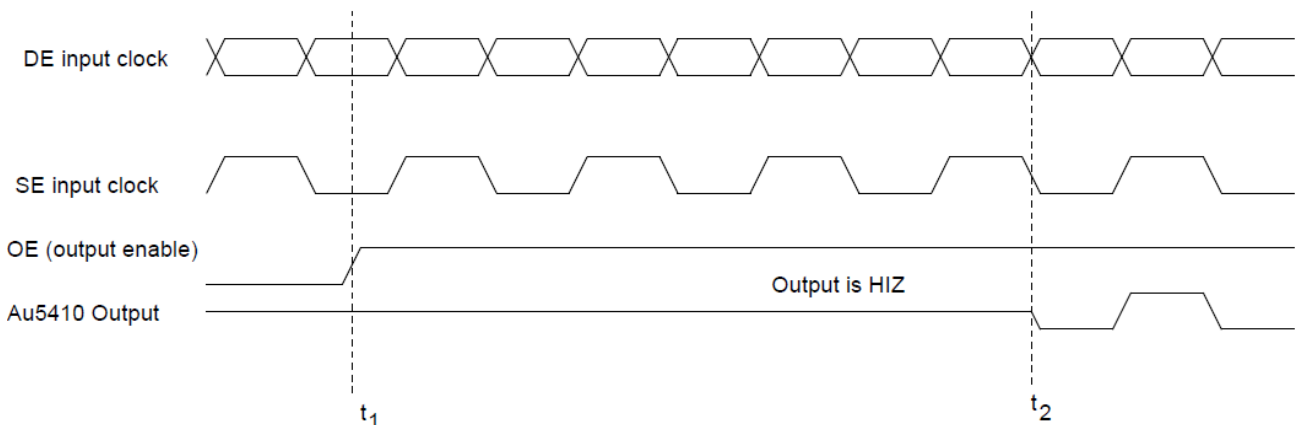
When REFout\_EN is disabled, the use of a resistive loading can be used to set the output to a predetermined level. For example, if REFout\_EN is configured with a 1K  $\Omega$  load to ground, then the output will be pulled to low when disabled.

**Table 13 Reference Output Enable**

| Refout_EN | Output State   |
|-----------|----------------|
| 0         | Disabled (HiZ) |
| 1         | Enabled        |



**Figure 3 REFout\_EN: Output disable**



**Figure 4 REFout\_EN: Output enable**

## 4 Application Information

### 4.1 Current consumption and Power Dissipation Calculations

The current consumption specified in the Electrical Characteristics can be used to calculate the total power dissipation and the IC power dissipation for any output driver configuration. The total current drawn from the VCC is given by the equation below.

$$I_{CC} = I_{CORE,STATIC} + n * \left(\frac{f_{in}}{100}\right) * I_{CORE,DYN}$$

$I_{CC}$ , is the total core current drawn from VCC.  $I_{CORE,STATIC}$ , is the current taken by Au5411, if not clocks are toggling and both the output driver banks are in HIZ state.  $I_{CORE,DYN}$ , is the switching current taken from VCC when the selected input clock is toggling at a frequency of  $f_{in}$ .  $n$ , is the number of output banks that are active.

Current consumed the output supplies in each mode are listed below. The current in output bank A/B in LVPECL mode is given below.

$$I_{CCOA} = I_{CCOB} = I_{CC,LVPECL}$$

The current in output bank A/B in LVDS mode is given below.

$$I_{CCOA} = I_{CCOB} = I_{CC,LVDS}$$

The current in output bank A/B in HCSL mode is given below.

$$I_{CCOA} = I_{CCOB} = I_{CC,HCSL}$$

The current in output bank C is given below.

$$I_{CCOC} = I_{CC,LVCMOS}$$

The equation for the total power dissipation is given below.

$$P_{TOTAL} = V_{CC} * I_{VCC} + V_{CCOA} * I_{CCOA} + V_{CCOB} * I_{CCOB} + V_{CCOC} * I_{CCOC}$$

If the output driver configuration is LVPECL or LVDS, then the power dissipated in any termination resistors and termination voltages need to be accounted to calculate the power dissipation in the device.

The power dissipated in the termination resistor in LVPECL mode is given below.

$$P_{RT,PECL} = \frac{(V_{OH,PECL} - V_{TT})^2}{R_T} + \frac{(V_{OL,PECL} - V_{TT})^2}{R_T}$$

The power dissipated in the termination voltage for LVPECL mode is given below

$$P_{VTT,PECL} = V_{TT} * \left( \frac{(V_{OH,PECL} - V_{TT})}{R_T} + \frac{(V_{OL,PECL} - V_{TT})}{R_T} \right)$$

The power dissipated in the ground referenced termination resistor for HCSL is given below.

$$P_{RT,HCSL} = \frac{V_{OH,HCSL}^2}{R_T}$$

The power dissipated in the device is given below.

$$P_{DEVICE} = P_{TOTAL} - N_1 * (P_{RT,PECL} + P_{VTT,PECL}) - N_2 * P_{RT,HCSL}$$

#### 4.1.1 Example: Worst case power dissipation

BANK A and B output drivers are configured in LVPECL mode. The input frequency is 2100 MHz.  $V_{CC} = 3.465$ ,  $V_{CCOA} = V_{CCOB} = V_{CCOC} = 3.465$ , REFOUT is enabled. Assume 5 pF load for REFOUT.

**Table 14 Worst Case Power Dissipation**

| Parameter      | Value | Unit |
|----------------|-------|------|
| $V_{CC}$       | 3.465 | V    |
| $V_{CCOA}$     | 3.465 | V    |
| $V_{CCOB}$     | 3.465 | V    |
| $V_{CCOC}$     | 3.465 | V    |
| $I_{CC}$       | 52    | mA   |
| $I_{CCOA}$     | 198   | mA   |
| $I_{CCOB}$     | 198   | mA   |
| $I_{CCOC}$     | 10    | mA   |
| $P_{TOTAL}$    | 1588  | mW   |
| $V_{OH\_PECL}$ | 2.5   | V    |
| $V_{OL\_PECL}$ | 1.8   | V    |
| $V_{TT}$       | 1.465 | V    |
| $P_{RT\_PECL}$ | 24    | mW   |
| $P_{VT\_PECL}$ | 40    | mW   |
| $P_{DEVICE}$   | 948   | mW   |

## 4.2 Driving the Clock Inputs

The Au5411 has two universal clock inputs (CLKin0/CLKin0\* and CLKin1/CLKin1\*). Au5411 can accept 3.3 V/2.5 V LVPECL, LVDS, CML, SSTL, and other differential and single-ended signals that meet input common mode, slew rate and swing requirements specified in the Electrical Characteristics. The Au5411 supports a wide common mode voltage range and input signal swing

To achieve the best possible phase noise and jitter performance, it is mandatory for the input to have high slew rate of 3 V/ns (differential) or higher. Driving the input with a lower slew rate will degrade the noise floor and jitter. It is recommended to drive the input signal differentially for better slew rate and jitter. The user can also drive a single ended clock. If the user is driving the single ended clock signal on say CLKin0, then CLKin0\* pin need to be connected to a 0.1 uF capacitor on the PCB.

### 4.2.1 Driving Clock Inputs with LVCMOS Driver (AC coupled)

Figure 5 shows how a differential input can be wired to accept LVCMOS single ended levels in AC coupled mode. The bypass capacitor (C1) is used to help filter noise on the DC bias on the inverting pin of the clock input. This bypass should be located as close to the input pin as possible. Two resistors  $R_{T1}$  and  $R_{T2}$  set the common mode voltage at the output of the LVCMOS driver to  $V_{DD}/2$ . This prevents average DC leakage current from the LVCMOS driver and avoids unnecessary power dissipation.

For example, if the input clock is driven from a single-ended 2.5 V LVCMOS driver and the DC offset (or swing center) of this signal is 1.25 V, the  $R_{T1}$  and  $R_{T2}$  values should be adjusted to set the  $V_1$  at 1.25 V. This configuration requires that the sum of the output impedance of the driver ( $R_o$ ) and the series resistance ( $R_s$ ) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in the following way. First,  $R_{T1}$  and  $R_{T2}$  in parallel should equal the transmission line impedance. For most 50  $\Omega$  applications,  $R_{T1}$  and  $R_{T2}$  can be 100  $\Omega$ .

$$Z_o = R_o + R_s = 50 \text{ Ohm}$$

$$\frac{R_{T1} * R_{T2}}{R_{T1} + R_{T2}} = 50 \text{ Ohm}$$

$$\frac{V_{CC} * R_{T2}}{R_{T1} + R_{T2}} = \frac{V_{CC}}{2}$$

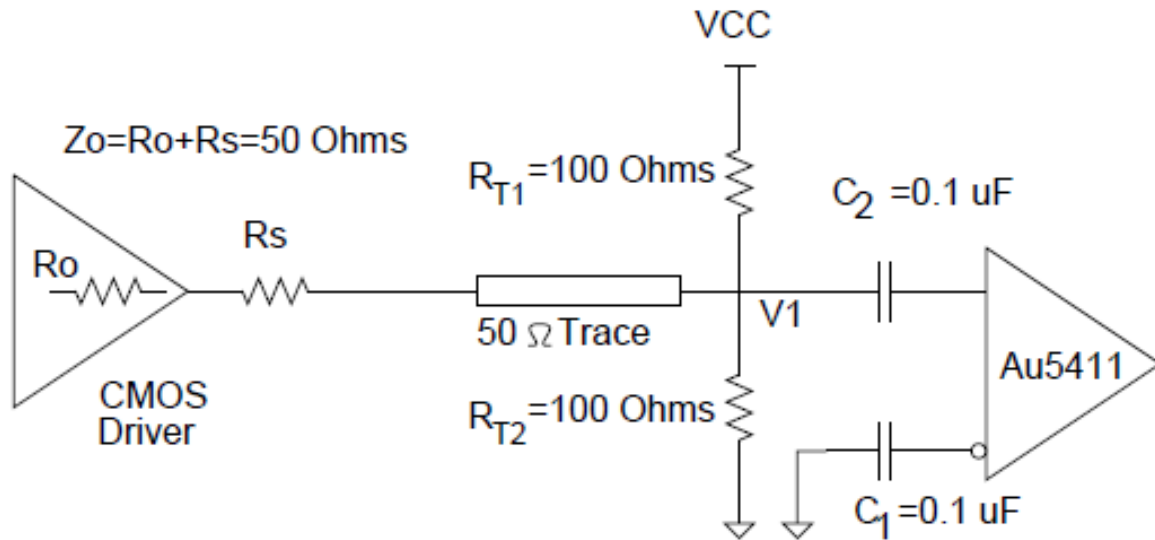


Figure 5 AC coupling LVC MOS clock to Au5411

The inverting differential input can be connected to a 0.1 uF bypass capacitor. This pin is biased internally to a voltage close to VDD/2.

Another variant of the AC coupling of LVC MOS input clock is shown in Figure 6. We use single termination resistor of 50 Ω to ground. A 0.1 uF (C3) ac coupling capacitor is connected in series with the LVC MOS clock source to prevent DC leakage current.

$$Z_o = R_o + R_s = 50 \text{ Ohm}$$

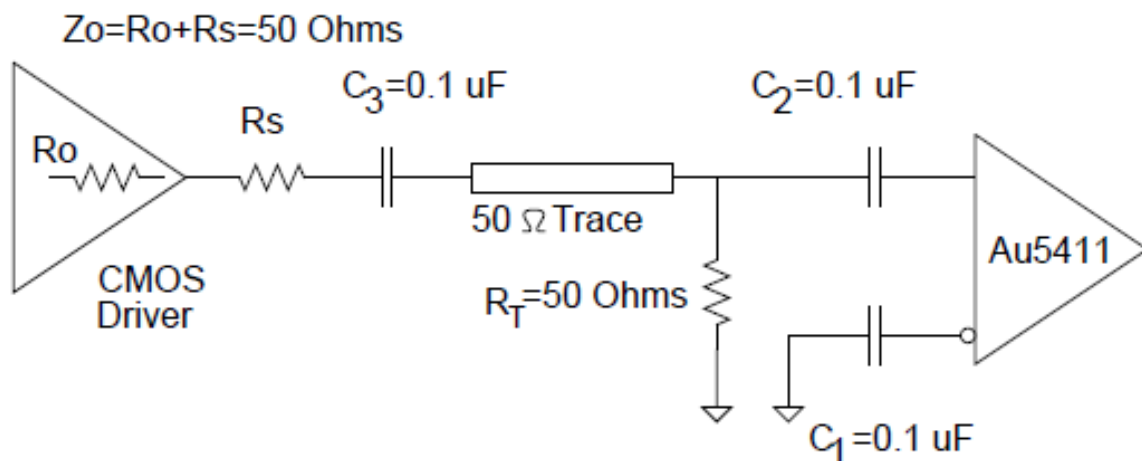


Figure 6 AC coupling of LVC MOS clock with single 50 Ω resistor termination to ground

#### 4.2.2 Driving Clock Inputs with LVC MOS Driver (DC coupled)

Figure 7 shows how a differential input can be wired to accept LVC MOS single ended clock signals in DC coupled mode. The reference voltage  $V1 = VDD/2$  is generated by the bias resistors RS1 and RS2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of RS1 and RS2 might need to be adjusted to position the bias voltage V2 in the center of the input voltage swing.

$$Z_o = R_o + R_s = 50 \text{ Ohm}$$

$$\frac{VCC * R_{S2}}{R_{S1} + R_{S2}} = \frac{VCC}{2}$$

$$\frac{R_{T1} * R_{T2}}{R_{T1} + R_{T2}} = 50 \text{ Ohm}$$

$$\frac{VCC * R_{T2}}{R_{T1} + R_{T2}} = \frac{VCC}{2}$$

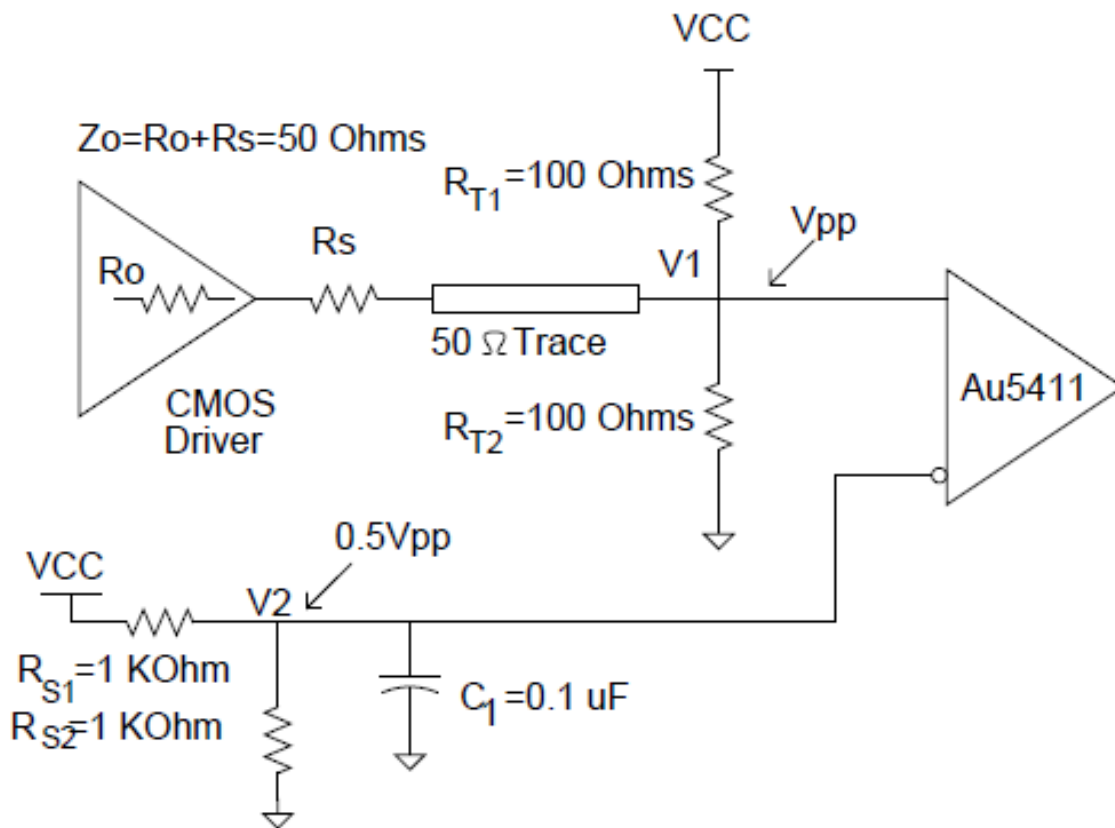


Figure 7 DC coupling of LVCMOS clock to Au5411 – configuration 1

For example, if the input clock is driven from a single-ended 2.5 V LVCMOS driver and the DC offset (or swing center) of this signal is 1.25 V, the  $R_{S1}$  and  $R_{S2}$  values should be adjusted to set the  $V2$  at 1.25 V. The values below are for when both the single ended swing and  $VDD$  are at the same voltage.

This configuration requires that the sum of the output impedance of the driver ( $R_o$ ) and the series resistance ( $R_s$ ) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First,  $R_{T1}$  and  $R_{T2}$  in parallel should equal the transmission line impedance. For most 50  $\Omega$  applications,  $R_{T1}$  and  $R_{T2}$  can be 100  $\Omega$ . The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver.

Figure 8 shows a second input clock configuration where  $R_{T1}$ ,  $R_{T2}$  are removed and replaced with a 50  $\Omega$  termination resistor  $R_T$  to ground. It is possible that LVCMOS driver (or clock source) may not be able to drive 50  $\Omega$  load in DC coupled mode. The user can use series RC termination to overcome this limitation. The design equations for the input clock configuration shown in Figure 8 is given below

$$Z_o = R_o + R_s = 50 \text{ Ohm}$$

$$\frac{VCC * R_{S2}}{R_{S1} + R_{S2}} = \frac{V_{pp}}{2}$$

The LVCMOS single ended clock input with series RC termination near the buffer is shown in Figure 9. There is a single termination resistor  $R_T$  which is connected to ground through a capacitor  $C_{AC}$ . The value of series capacitor is given by a formula.

$$C_{AC} \geq \frac{3T_D}{50\Omega}, T_D \text{ is the transmission line delay}$$

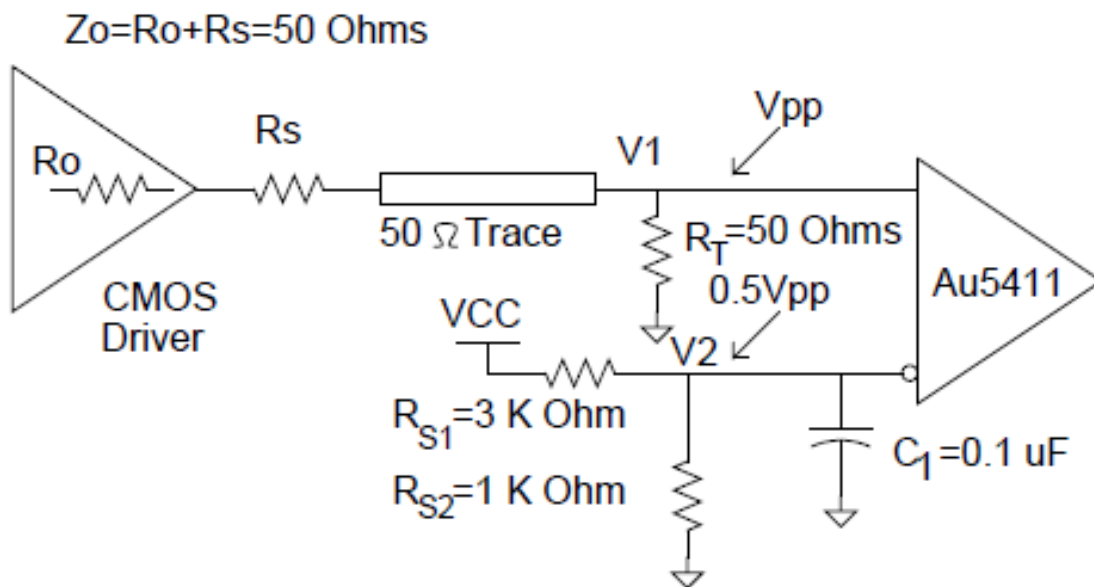


Figure 8 DC coupled LVCMOS input clock configuration – configuration 2

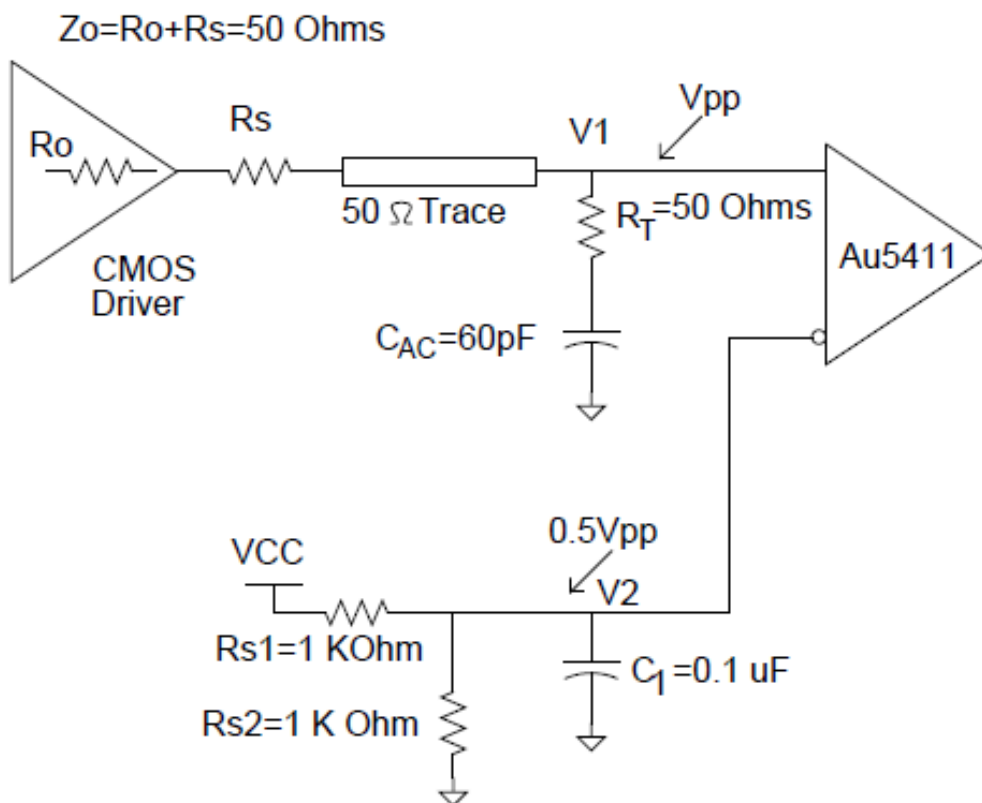


Figure 9 DC coupled LVCMOS input clock with series RC termination – configuration 3

For low frequencies we can direct couple the LVCMOS clock to Au5411 input clock pin as shown below.

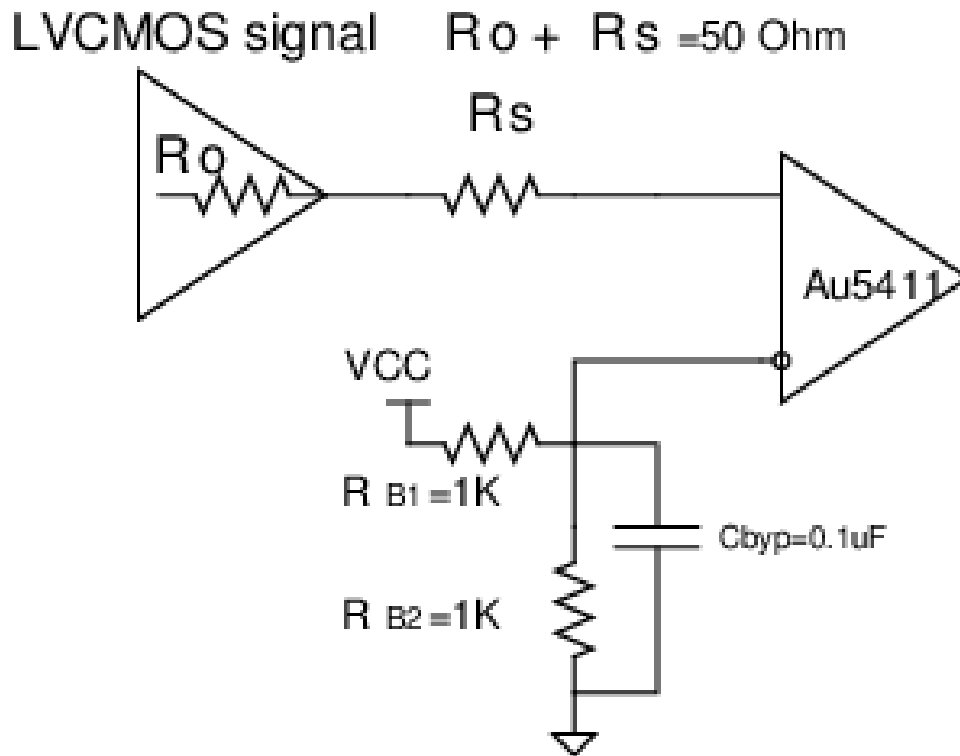


Figure 10: Direct coupling of LVCMOS clock to Au5411

#### 4.2.3 Driving XTAL\_IN with LVCMOS Driver (AC coupled)

The crystal input XTAL\_IN can be overdriven with single ended clock (LVCMOS driver or one side of a differential driver). The peak swing at XTAL\_IN should be limited to 1.5 V. The XTAL\_OUT pin, in this case can be floating. The SEL1, SEL0 should be 2'b10. The maximum voltage at XTAL\_IN should not exceed 1.5 V and minimum voltage should not go below -0.3 V. The slew rate at XTAL\_IN should be greater than 0.2 V/ns.

For 3.3 V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. Figure 11 shows an example of the interface diagram for a high speed 3.3 V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver ( $R_o$ ) and the series resistance ( $R_s$ ) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First,  $R_{T1}$  and  $R_{T2}$  in parallel should equal the transmission line impedance. For most 50  $\Omega$  applications,  $R_{T1}$  and  $R_{T2}$  can be 100  $\Omega$ .

$$Z_o = R_o + R_s = 50 \text{ Ohm}$$

$$\frac{R_{T1} * R_{T2}}{R_{T1} + R_{T2}} = 50 \text{ Ohm}$$

$$\frac{VCC * R_{T2}}{R_{T1} + R_{T2}} = \frac{VCC}{2}$$

For both the AC coupled configurations, the maximum peak to peak swing before the ac coupling capacitor is 1.65 V. The maximum DC bias voltage of XTAL\_IN is 0.675 V. Therefore the maximum swing at the XTAL\_IN pin is given by the equation given below.

$$V_{swing,pk,XTAL\_IN} = 0.675 + 0.5 * 1.65 = 1.5V$$

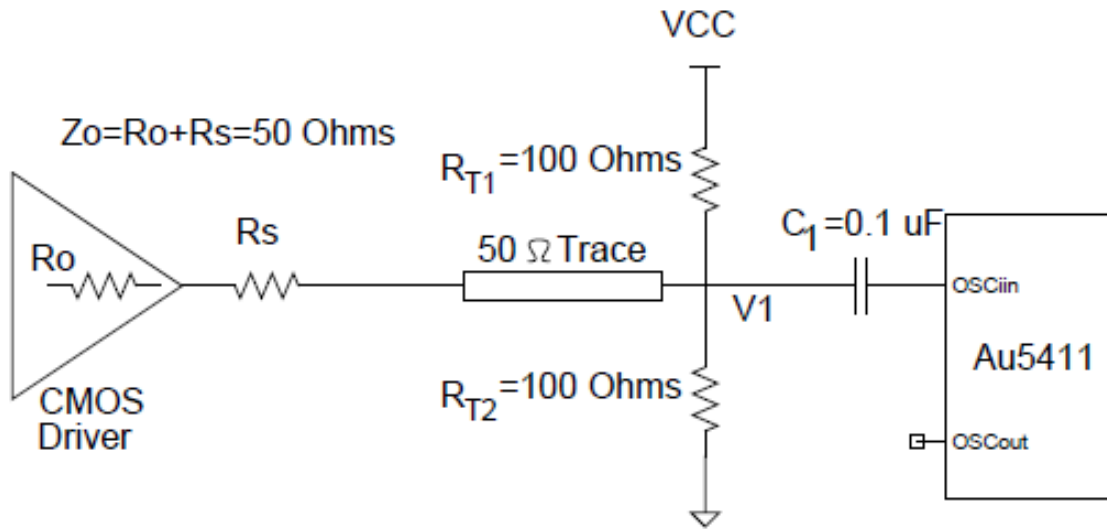


Figure 11 Single ended LVCMOS input – configuration 1, AC coupling to crystal input

Figure 12 shows a second input clock configuration where  $R_{T1}$ ,  $R_{T2}$  are removed and replaced with a 50  $\Omega$  termination resistor  $R_T$  to ground. A 0.1  $\mu F$  is in series with the CMOS driver to prevent any DC leakage current.

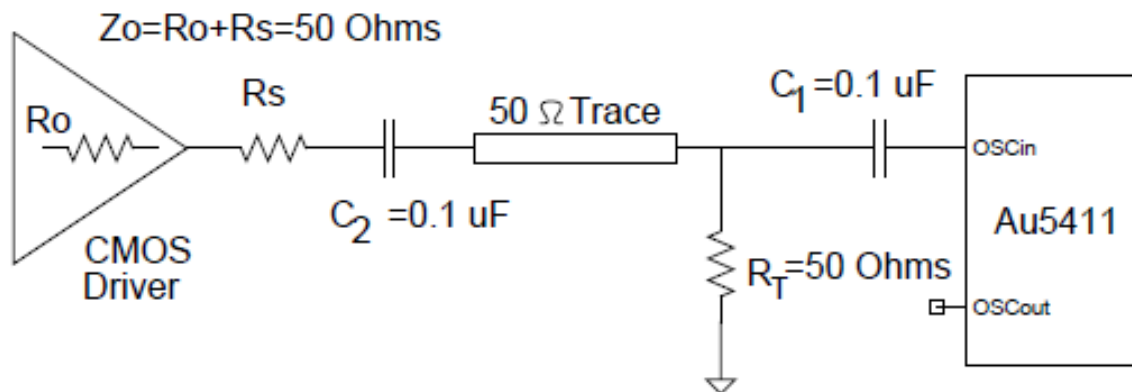


Figure 12 Single ended LVCMOS input – configuration 2, AC coupling to crystal input

#### 4.2.4 Driving XTAL\_IN with LVCMOS Driver (DC coupled)

The crystal input XTAL\_IN can be overdriven with single ended clock as shown in Figure 13, in DC couple mode. The peak swing at XTAL\_IN should be limited to 1.5 V (voltage at the crystal input pin). The XTAL\_OUT pin, in this case can be floating. The SEL1, SEL0 should be 2'b11. If the LVCMOS driver is on higher supply, say 3.3 V, use a resistor divider on the PCB to scale down the peak output voltage to 1.5 V.



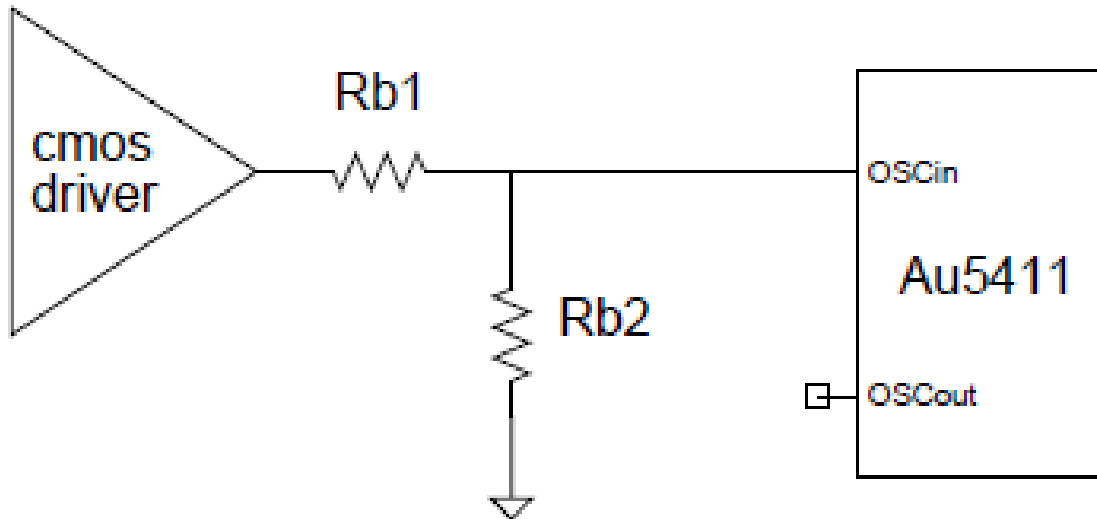


Figure 13 Single ended LVCMOS input, DC coupling to crystal input

#### 4.2.5 LVDS (DC coupled)

Terminate with a differential 100 Ω as close to the receiver as possible. This is shown in Figure 14.

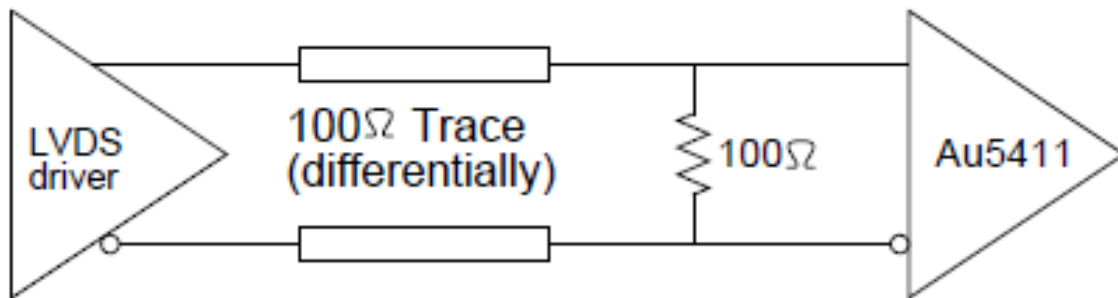


Figure 14 Termination scheme for DC coupled LVDS

#### 4.2.6 HCSL (DC coupled)

Termination resistor is 50 Ω to ground, close to the output driver. A series resistance  $R_s$  is sometimes used to limit the overshoot during fast transients. The termination scheme is shown in Figure 15.

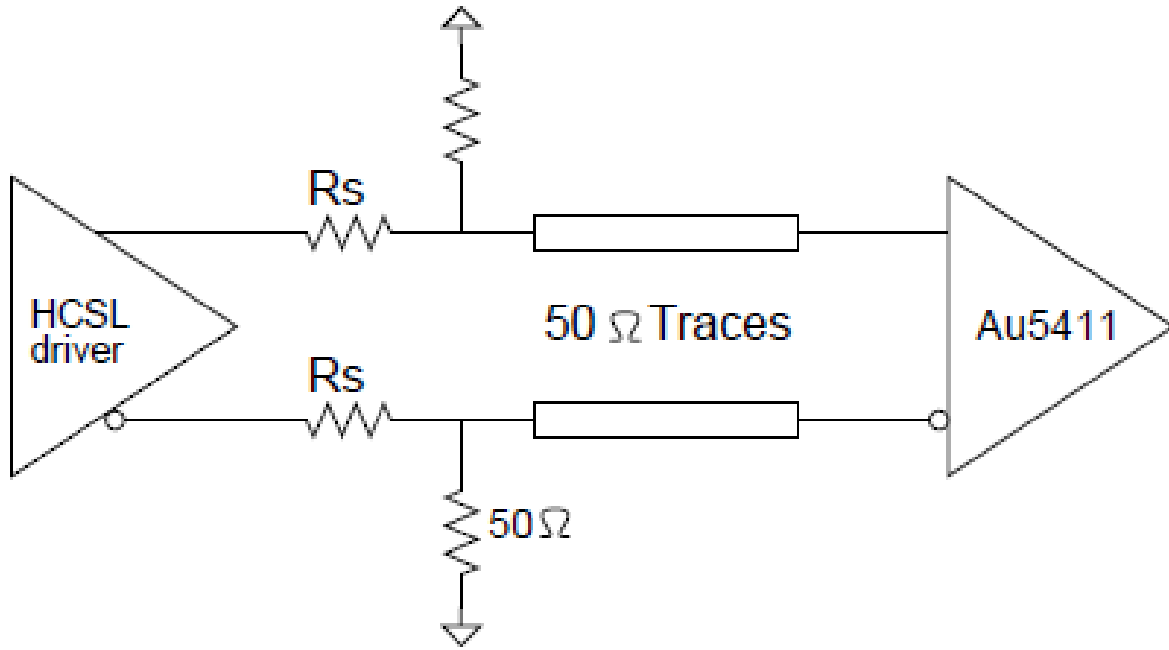


Figure 15 Termination scheme for DC coupled HCSL

#### 4.2.7 LVPECL (DC coupled)

For DC couple operation, the 50 Ω termination resistors are placed close to the receiver. The termination resistors are biased with a voltage source  $V_{TT}$ .

$$V_{TT} = V_{DD0} - 2V.$$

This termination scheme is shown in Figure 16. Alternatively, the user can also implement a Thevenin equivalent of  $V_{TT}$  using a resistor divider. This scheme and the values of the resistors in the resistor divider are given in Figure 17.

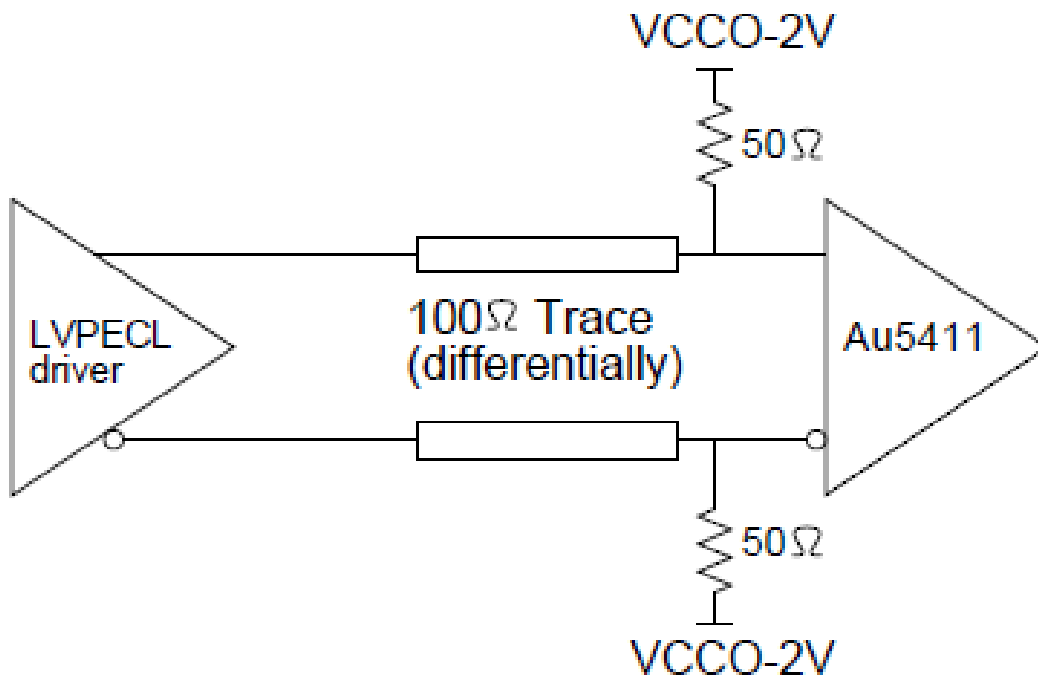


Figure 16 Termination scheme for DC coupled LVPECL

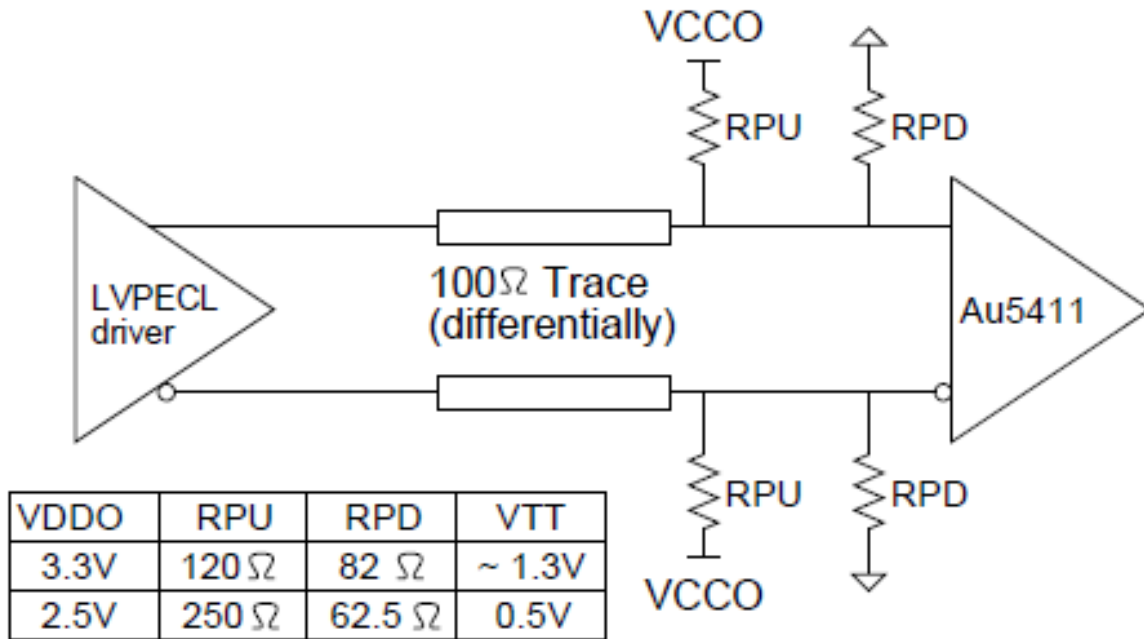


Figure 17 Termination scheme for DC coupled LVPECL, Thevenin equivalent

The design equations for the LVPECL Thevenin equivalent termination are given below.

$$\frac{R_{PD} * R_{PU}}{R_{PD} + R_{PU}} = 50\Omega$$

$$\frac{R_{PD} * VCCO}{R_{PD} + R_{PU}} = VCCO - 2V$$

#### 4.2.8 SSTL (DC coupled)

The SSTL input clock configuration is shown in Figure 18. The transmission line impedance is 60 Ω in the application example given. Therefore we use two 120 Ω resistors from VCCO to ground for biasing the clock input pins. The effective termination impedance in this case is 60 Ω.

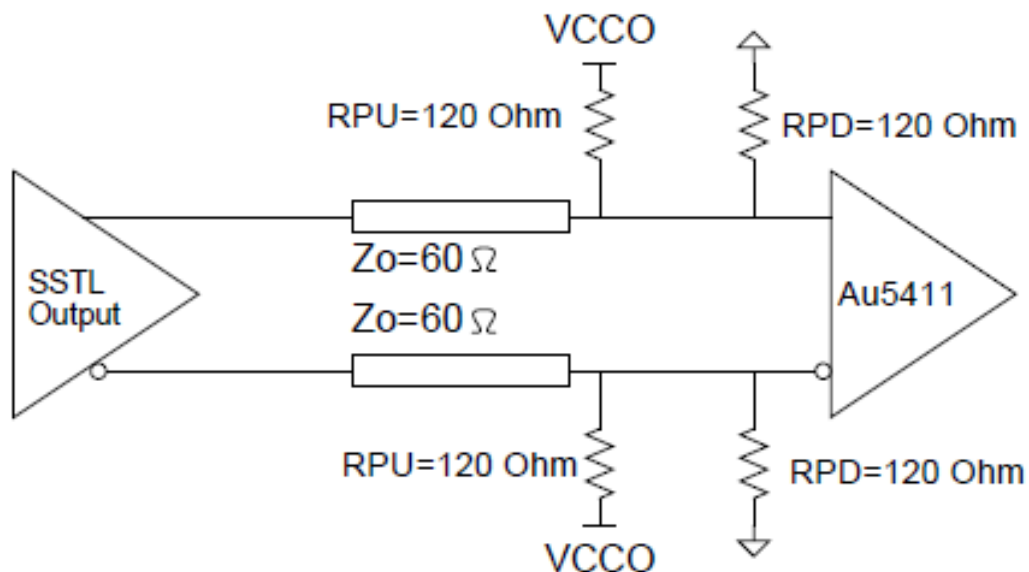


Figure 18 Example of input clock termination for SSTL clock.

### 4.2.9 LVDS (AC coupled)

The load termination resistor should be placed before the AC coupling capacitors. The load termination resistor and the AC coupling capacitors should be placed close to the receiver. The termination scheme is shown in Figure 19.

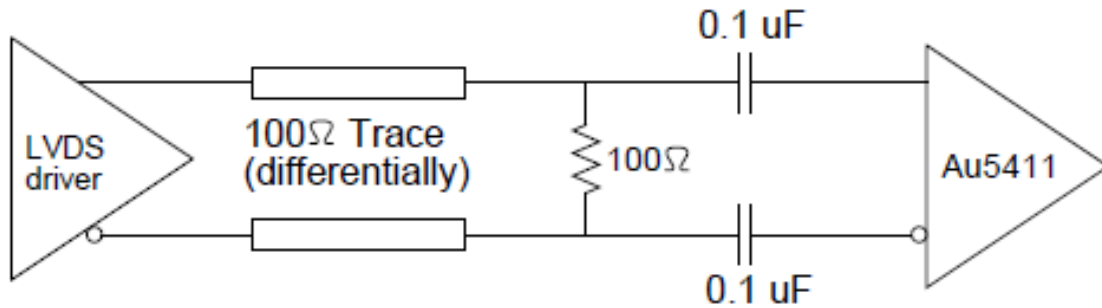


Figure 19 Termination scheme for AC coupled LVDS

### 4.2.10 LVPECL (AC coupled)

The LVPECL should have a DC path to ground. So, the user must place a resistance  $R_T$ , close to the output driver. The LVPECL AC coupling and Thevenin equivalent VTT termination scheme is shown in Figure 20.

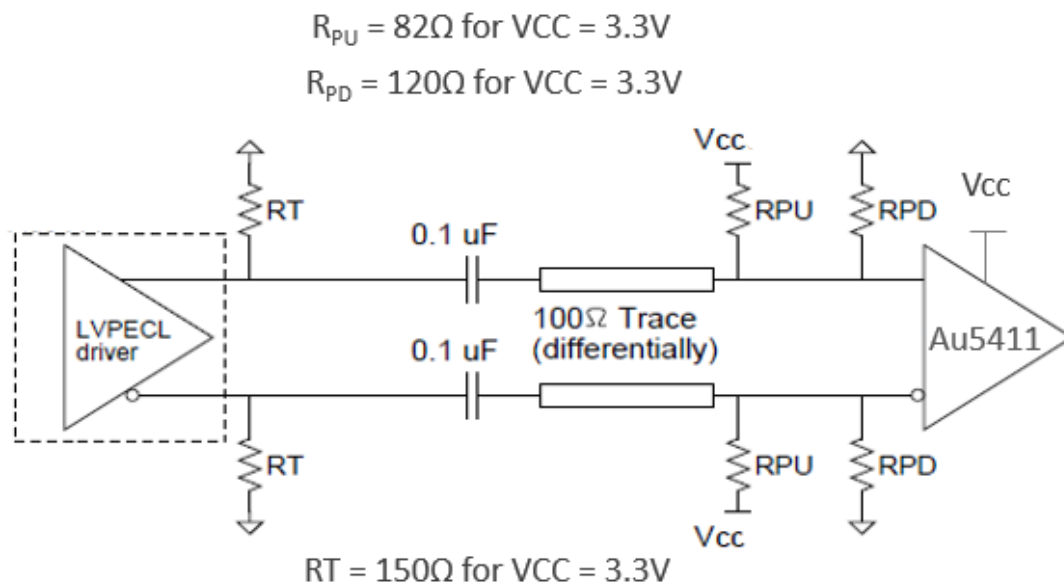


Figure 20 Termination scheme for AC coupled LVPECL, Thevenin Equivalent

The pull up resistance  $R_{PU}$  and pull down resistance  $R_{PD}$  sets the input common mode voltage for Au5411. The value of the input common mode voltage can be estimated by the equation given below

$$V_{ICM} = \frac{V_{CC} * R_{PD}}{R_{PU} + R_{PD}} = \frac{3.3 * 120}{120 + 82} = 1.961V$$

The differential input common mode specification of Au5411 (from data sheet) is  $V_{CC} - 1.1 = 2.2 V$ , therefore the input common mode set by LVPECL AC coupled termination meets the Au5411 input common mode specification.

The LVPECL driver chip has resistance  $R_T$  providing DC path for the output driver current in the LVPECL driver. The effective load impedance at the input side of Au5411 (receiver side) is formed by parallel combination of  $R_{PU}$ ,  $R_{PD}$ .

The effective termination resistor value is given by the equation below

$$R_{termination} = \frac{R_{PU} * R_{PD}}{R_{PU} + R_{PD}} = \frac{120 * 82}{120 + 82} = 48.7\Omega$$

### 4.3 Termination of Output Driver of Au5411 for Various Load Configurations

#### 4.3.1 Au5411 REFOUT Termination for AC Coupled mode

AC coupling of Au5411 LVCMOS output driver is shown in Figure 21. We use single termination resistor of  $50\ \Omega$  to ground. A  $0.1\ \mu\text{F}$  AC coupling capacitor is connected in series with the LVCMOS clock source to prevent DC leakage current. The receiver side is terminated with a single  $50\ \Omega$  resistance to ground. The clock signal is then AC coupled to the receiver, in this example.  $C_1$  is a bypass capacitor that is used to suppress noise on the inverting differential input of the receiver.

$$Z_o = R_o + R_s = 50\ \text{Ohm}$$

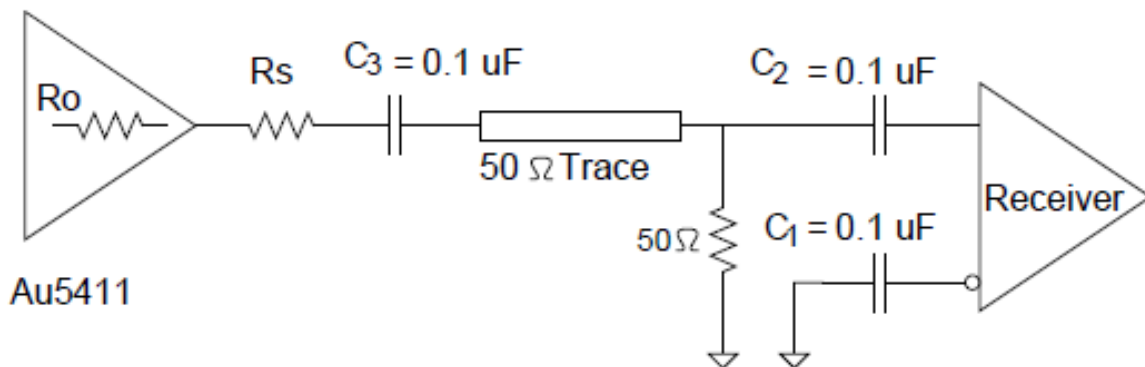


Figure 21 AC coupling of LVCMOS clock with single  $50\ \Omega$  resistor termination to ground

#### 4.3.2 Au5411 REFOUT Termination for DC Coupled mode

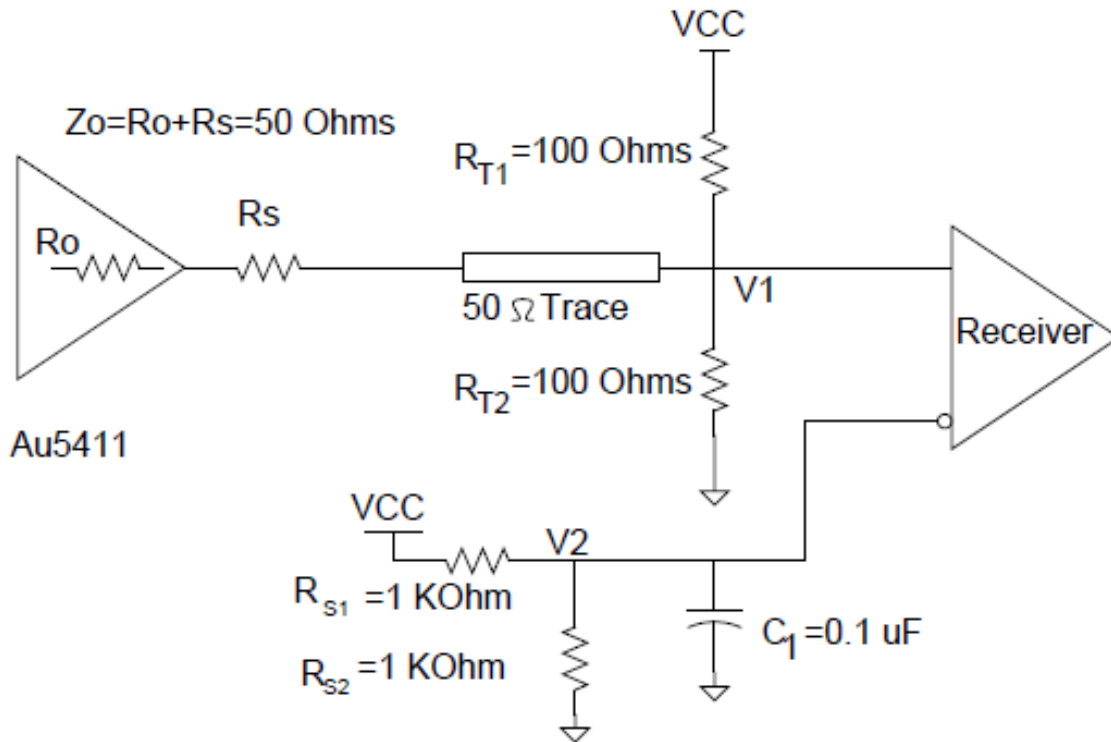
Figure 22 shows how Au5411 LVCMOS output drive can be terminated to send clock signals in DC coupled mode. The reference voltage  $V_1 = V_{DD}/2$  is generated by the bias resistors  $R_{S1}$  and  $R_{S2}$ . The bypass capacitor ( $C_1$ ) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of  $R_{S1}$  and  $R_{S2}$  might need to be adjusted to position the bias voltage  $V_2$  in the center of the input voltage swing.

$$Z_o = R_o + R_s = 50\ \text{Ohm}$$

$$\frac{V_{DD} * R_{S2}}{R_{S1} + R_{S2}} = \frac{V_{DD}}{2}, \text{Typical value of } R_{S1} = R_{S2} = 1\text{K}\Omega$$

$$\frac{R_{T1} * R_{T2}}{R_{T1} + R_{T2}} = 50\ \text{Ohm}, \text{Typical value of } R_{T1} = R_{T2} = 100\Omega$$

$$\frac{V_{DD} * R_{T2}}{R_{T1} + R_{T2}} = \frac{V_{DD}}{2}$$



**Figure 22 DC coupling of LVC MOS output clock termination – configuration 1**

For example, if the Au5411 supply is 2.5 V then the DC offset (or swing center) of this signal is 1.25 V, the  $R_{S1}$  and  $R_{S2}$  values should be adjusted to set the V2 at 1.25 V. The values below are for when both the single ended swing and VDD are at the same voltage.

This configuration requires that the sum of the output impedance of the driver ( $R_o$ ) and the series resistance ( $R_s$ ) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First,  $R_{T1}$  and  $R_{T2}$  in parallel should equal the transmission line impedance. For most 50  $\Omega$  applications,  $R_{T1}$  and  $R_{T2}$  can be 100  $\Omega$ . The values of the resistors can be increased to reduce the loading for slower and weaker LVC MOS driver.

Figure 23 shows a second input clock configuration where  $R_{T1}$ ,  $R_{T2}$  are removed and replaced with a 50  $\Omega$  termination resistor  $R_T$  to ground. There will be DC leakage current from Au5411, for the output termination shown in Figure 23. The user can use series RC termination to overcome this limitation. The design equations for the input clock configuration shown in Figure 23 is given below

$$Z_o = R_o + R_s = 50 \text{ Ohm}$$

$$\frac{VDD * R_{S2}}{R_{S1} + R_{S2}} = \frac{V_{pp}}{2} = \frac{VDD}{4}, \text{ Typical value of } R_{S1} = 3K\Omega, R_{S2} = 1K\Omega$$

The Au5411 LVC MOS output driver termination with series RC termination near the buffer is shown in Figure 24. There is a single termination resistor  $R_T$  which is connected to ground through a capacitor  $C_{AC}$ . The value of series capacitor is given by a formula.

$$C_{AC} \geq \frac{3T_D}{50\Omega}, T_D \text{ is the transmission line delay}$$

Typical value for  $C_{AC}$  is 60 pF, assuming delay of  $T_D = 200 \text{ ps/inch}$  and 5 inch input clock route length.

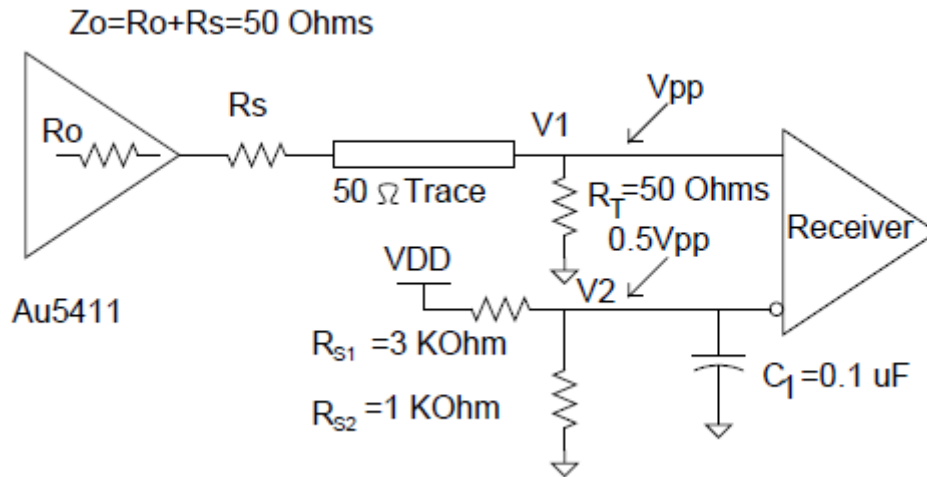


Figure 23 DC coupled LVC MOS output clock configuration – configuration 2

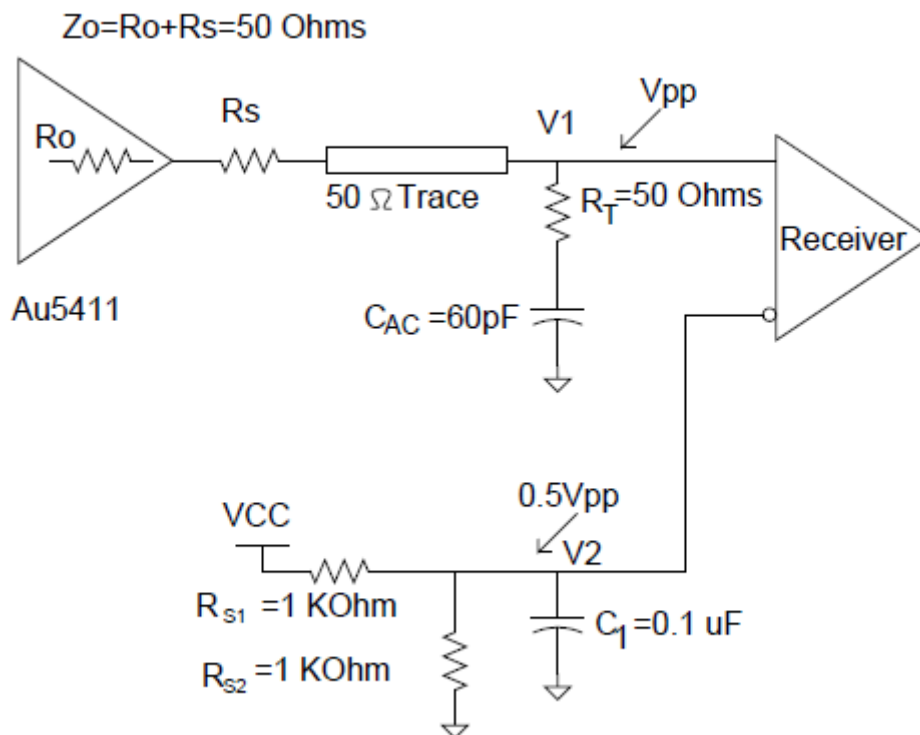


Figure 24 DC coupled LVC MOS output clock with series RC termination – configuration 3

The typical value of  $R_{S1}$  and  $R_{S2}$  in this case is 1K  $\Omega$  and that of  $C_{AC}$  is 60 pF.

### 4.3.3 CMOS (Capacitive load)

The capacitive load can be driven as shown in figure below. For Au5411 LVC MOS driver the  $R_o$  is very close to 50  $\Omega$  by design. Therefore  $R_s = 0$  is recommended.

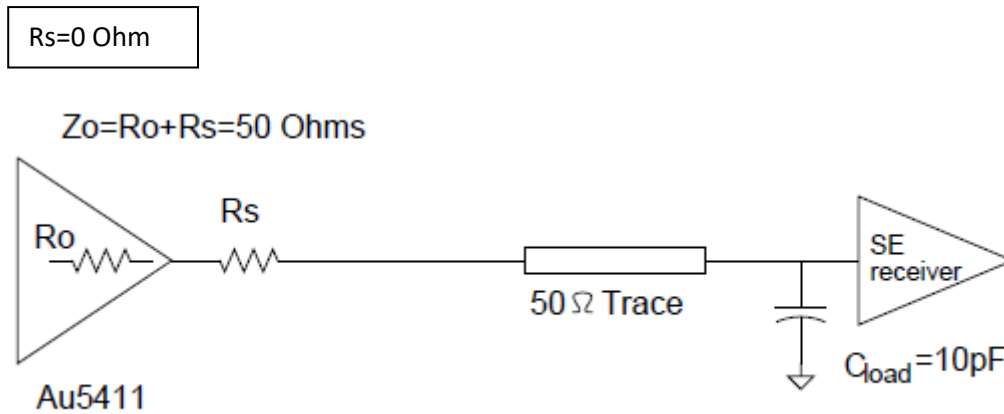


Figure 25 Typical application load

#### 4.4 Termination of Output Drivers (DC coupled)

##### 4.4.1 LVDS DC Coupled Output Termination

Terminate with a differential 100 Ω as close to the receiver as possible. This is shown in Figure 26.

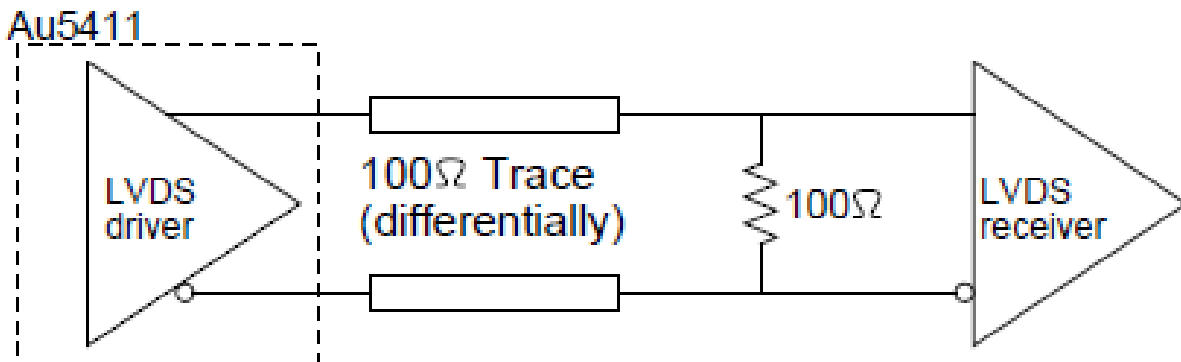


Figure 26 Termination scheme for DC coupled LVDS

##### 4.4.2 HCSL DC Coupled Output Termination

Termination resistor is 50 Ω to ground, close to the output driver. A series resistance  $R_s$  is sometimes used to limit the overshoot during fast transients. The termination scheme is shown in Figure 27.



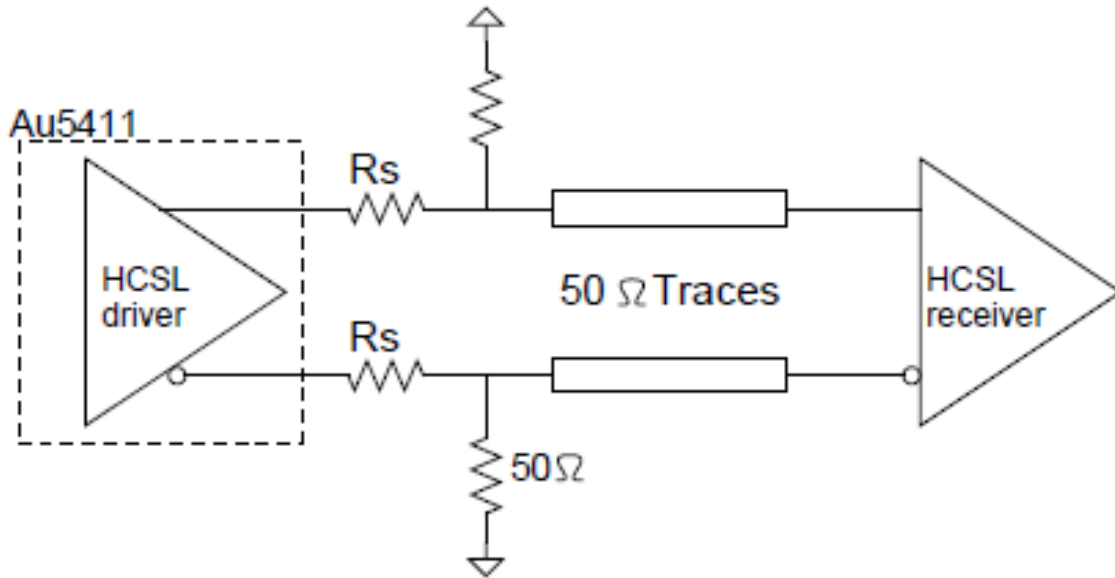


Figure 27 Termination scheme for DC coupled HCSL

#### 4.4.3 LVPECL DC Coupled Output Termination

For DC couple operation, the 50 Ω termination resistors are placed close to the receiver. The termination resistors are biased with a voltage source  $V_{TT}$ . Typically,  $V_{TT} = V_{CCO} - 2V$ . This termination scheme is shown in Figure 28. Alternatively, the user can also implement a Thevenin equivalent of  $V_{TT}$  using a resistor divider. This scheme and the values of the resistors in the resistor divider are given in Figure 29.

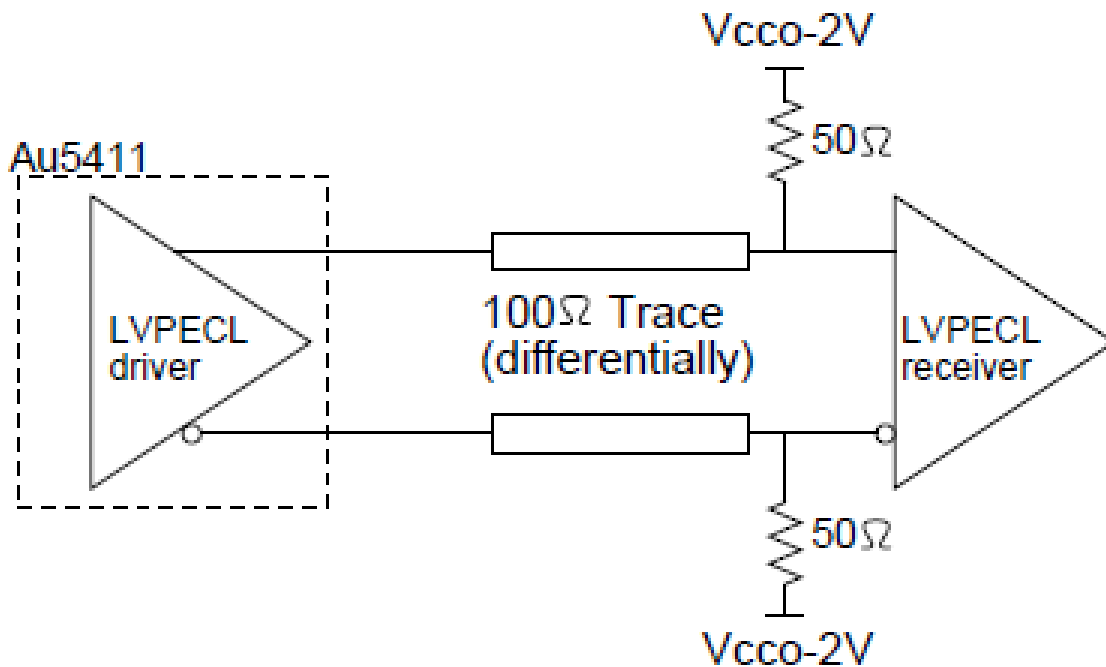


Figure 28 Termination scheme for DC coupled LVPECL

$$\frac{R_{PD} * R_{PU}}{R_{PD} + R_{PU}} = 50\Omega$$

$$\frac{R_{PD} * VDDO}{R_{PD} + R_{PU}} = VCCO - 2V$$

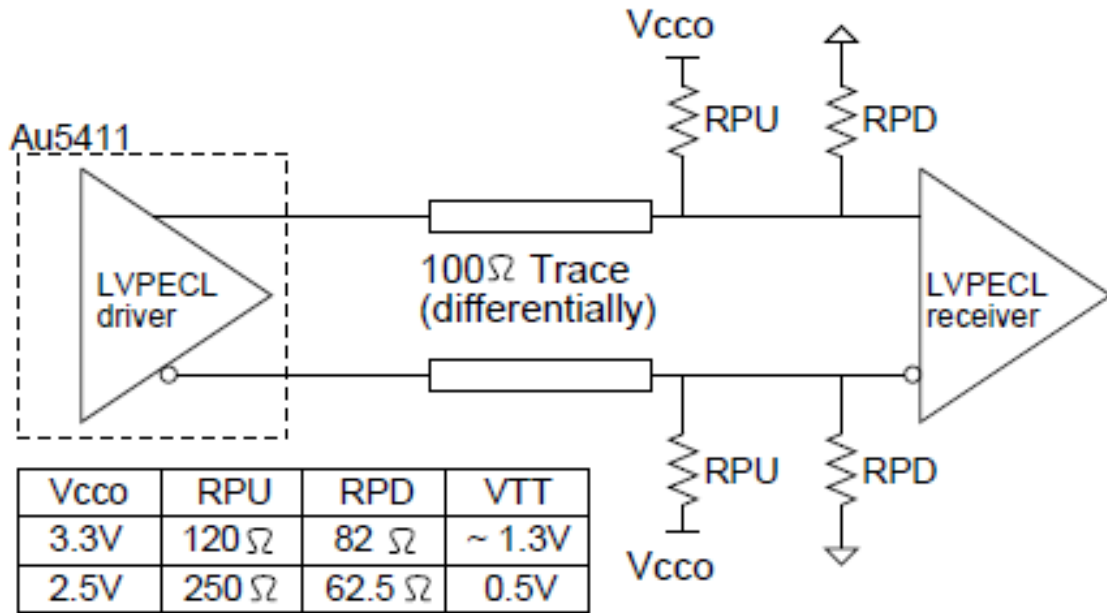


Figure 29 Termination scheme for DC coupled LVPECL, Thevenin equivalent

## 4.5 Termination of Output Drivers (AC coupled)

### 4.5.1 LVDS AC Coupled Output Termination

The load termination resistor should be placed before the AC coupling capacitors. The load termination resistor and the AC coupling capacitors should be placed close to the receiver. The termination scheme is shown in Figure 30. First figure shows Au5411 output driver configured in LVDS mode. The receiver in this case is shown as LVDS receiver. The second figure shows Au5411 output driver configured in LVDS mode and the receiver in this case is shown as CML receiver. As long as the LVDS swing is okay with the receiver the AC coupled output termination is same.

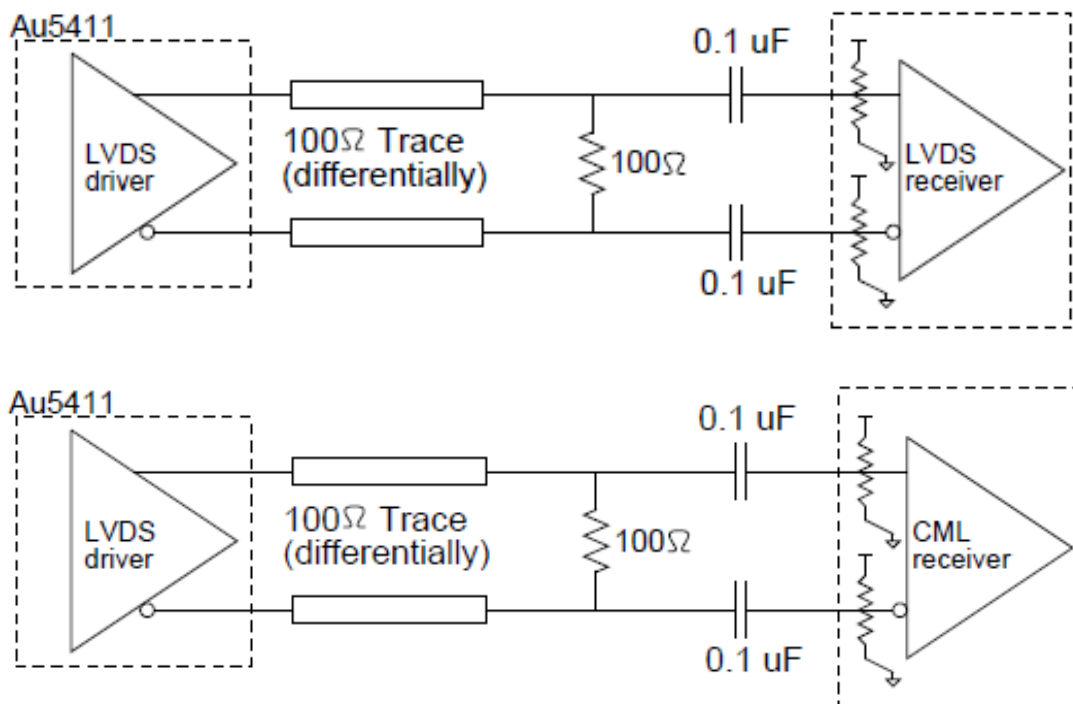


Figure 30 Termination scheme for AC coupled LVDS, driving LVDS receiver and CML receiver

### 4.5.2 LVPECL AC Coupled Output Termination

The LVPECL should have a DC path to ground. So the user must place a resistance  $R_T$ , close to the output driver. The LVPECL AC coupling and Thevenin equivalent  $V_{TT}$  termination scheme is shown in Figure 31. Au5411 swing reduces by about 20% as the effective load resistor is now the parallel combination of  $R_T$  at the driver side and  $50\ \Omega$  at the receiver side.

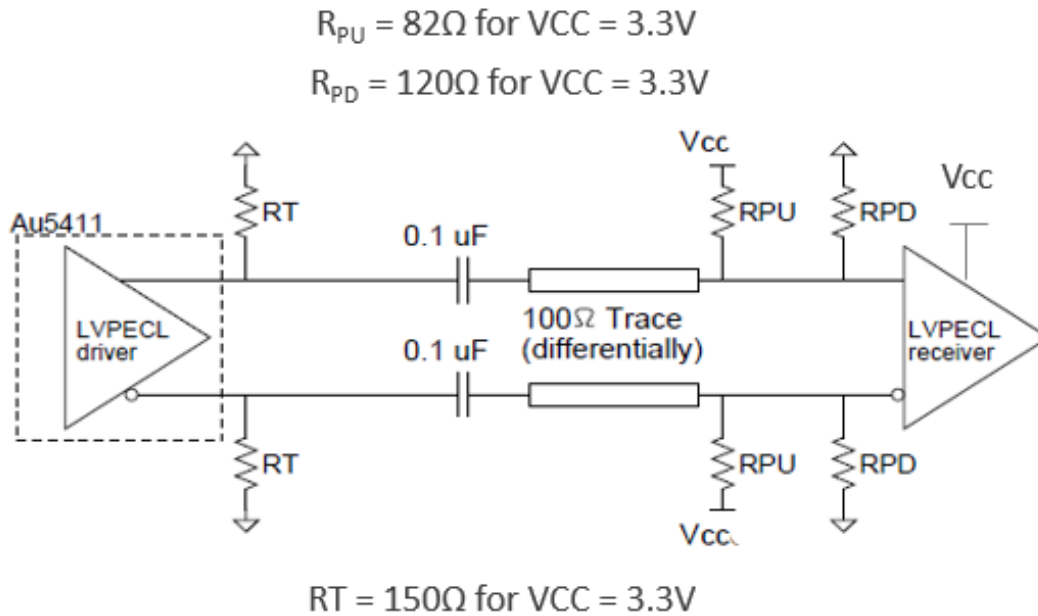


Figure 31 Termination scheme for AC coupled LVPECL, Thevenin Equivalent

The pull up resistance  $R_{PU}$  and pull down resistance  $R_{PD}$  sets the input common mode voltage for LVPECL receiver.

The value of the input common mode voltage can be estimated by the equation given below

$$V_{ICM} = \frac{V_{CC} * R_{PD}}{R_{PU} + R_{PD}} = \frac{3.3 * 120}{120 + 82} = 1.961V$$

The LVPECL driver of Au5411 has resistance  $R_T$  providing DC path for the output driver current in the LVPECL driver. The effective load impedance at the receiver side is formed by parallel combination of  $R_{PU}$ ,  $R_{PD}$ . The effective termination resistor value is given by the equation below

$$R_{termination} = \frac{R_{PU} * R_{PD}}{R_{PU} + R_{PD}} = \frac{120 * 82}{120 + 82} = 48.7\ \Omega$$

### 4.5.3 Termination of Output Drivers in LVPECL Mode, Single Ended, DC coupled

Single ended LVPECL operation is possible. The user can use a balun to convert differential output to single ended output. It is also possible to use the LVPECL driver as one or two separate 700 mV - PP signal. The unused output need to be terminated close to the output driver. These termination schemes are shown in Figure 32 and Figure 33.

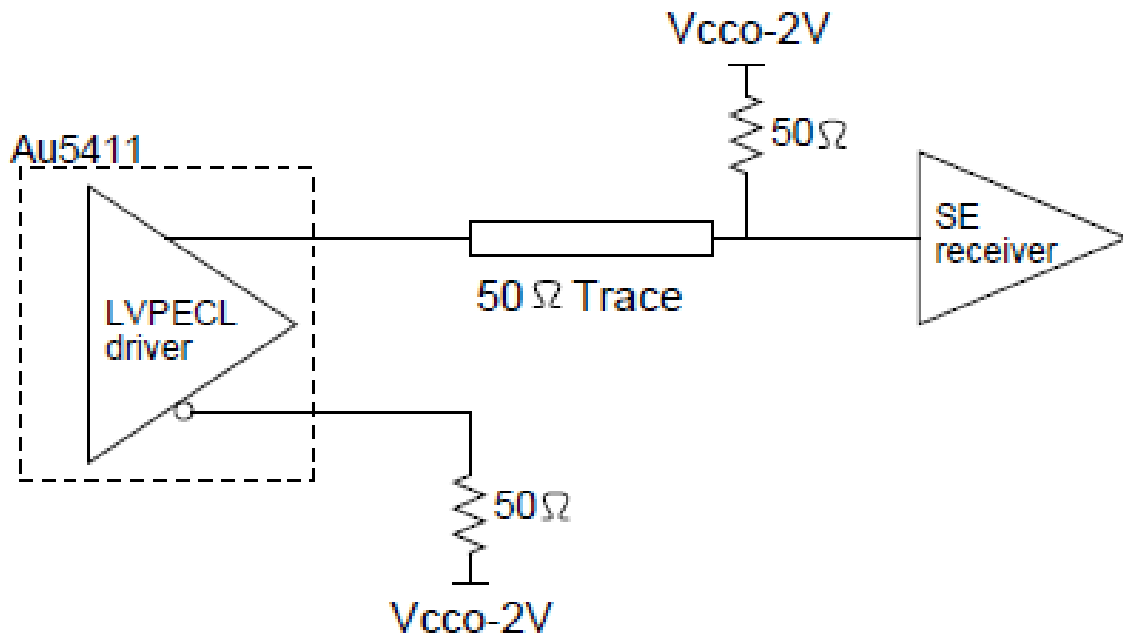


Figure 32 Termination scheme for DC coupled LVPECL, single ended

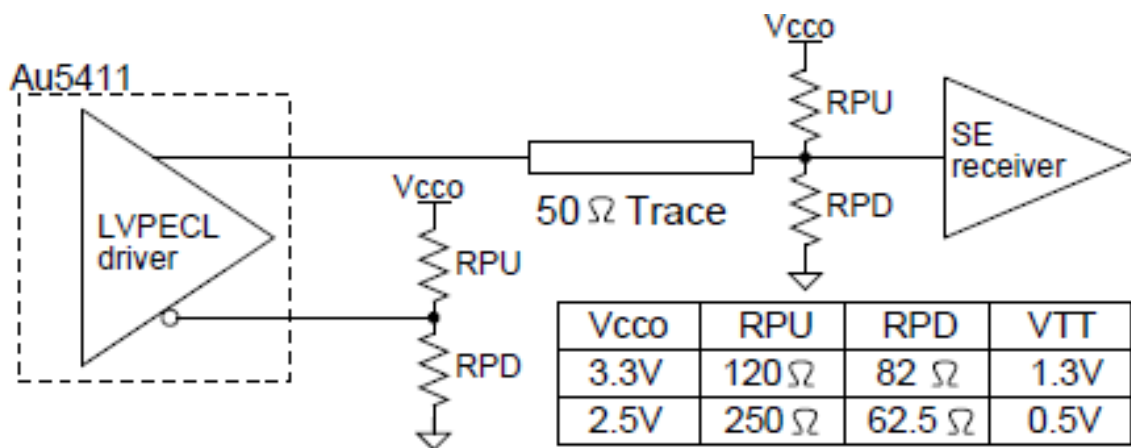


Figure 33 Termination scheme for DC coupled LVPECL, single ended, Thevenin equivalent

#### 4.5.4 Termination of Output Drivers in LVPECL Mode, Single Ended, AC coupled

LVPECL output driver needs a DC path to ground from its output. There for 160 Ω (if VCC = 3.3 V) resistor to ground is connected from the output of the LVPECL driver to ground. If VCC = 2.5 V, the DC path resistance should be 91 Ω. The 50 Ω load termination resistor must be placed close to input receiver and biased to a suitable voltage.

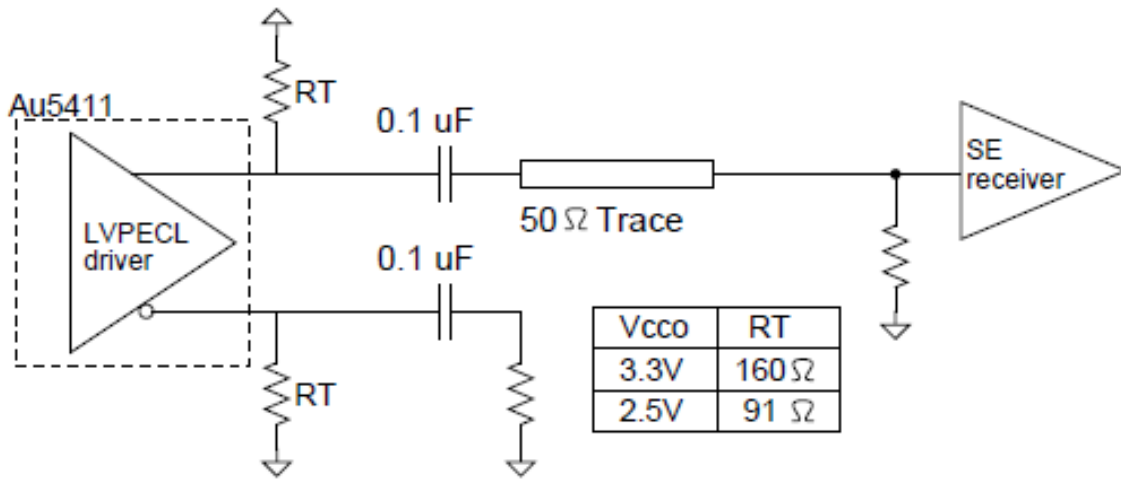


Figure 34 Termination scheme for AC coupled LVPECL, single ended

#### 4.5.5 Termination of Output Drivers in AC coupled HCSL mode

Termination resistor is 50  $\Omega$  to ground, close to the output driver. A series resistance  $R_s$  is sometimes used to limit the overshoot during fast transients. AC coupling capacitor of 0.1  $\mu\text{F}$  is used to couple the output HCSL signal in to the receiver. The same termination can be used for CML receiver.

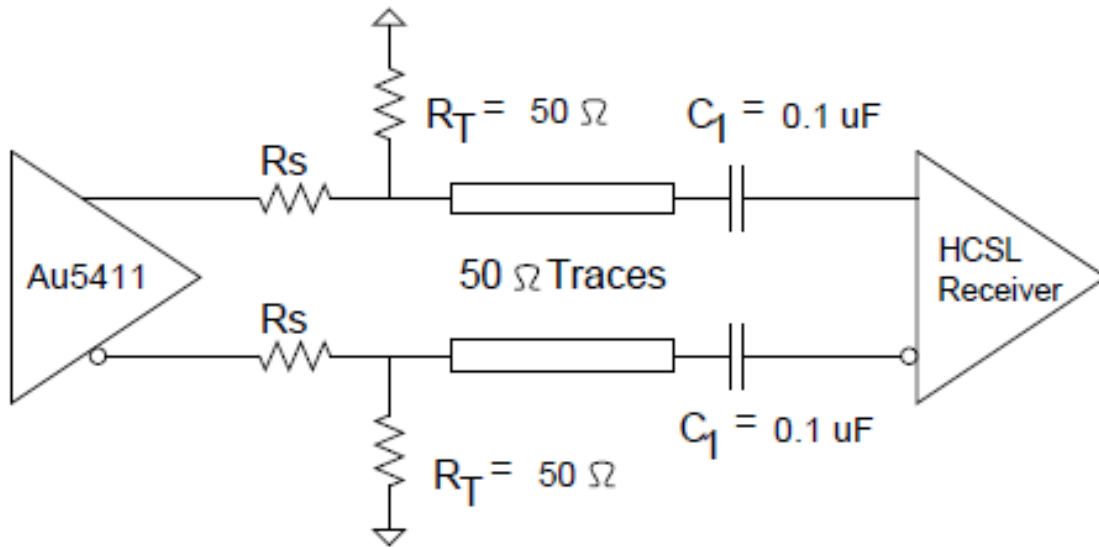


Figure 35 Output driver termination in HCSL AC coupled mode

## 5 Thermal Information

**Table 15 Thermal Metrics of Au5411**

| Thermal Metric   | Au5411<br>RHB<br>32 pins | Units |
|--|--------------------------|-------|
| $\theta_{JA}$ Junction to ambient thermal resistance, flow = 0 m/s | 36.3                     | °C/W  |
| $\theta_{JA}$ Junction to ambient thermal resistance, flow = 1 m/s | 31.6                     | °C/W  |
| $\theta_{JA}$ Junction to ambient thermal resistance, flow = 2 m/s | 30.4                     | °C/W  |
| $\theta_{JB}$ Junction to board                                    | 15.21                    | °C/W  |
| $\theta_{JC}$ Junction to case                                     | 18.90                    | °C/W  |
| $\psi_{JT}$ Junction to top characterization parameter             | 0.63                     | °C/W  |

## 6 HOT Swap Recommendations

### 6.1 Introduction

Hot-swap is a term used to refer to the insertion and removal of a daughter card from a backplane without powering down the system power. With today's high speed data and redundancy requirements, many systems are required to run continuously without being powered down. If special considerations are not taken, the device can be damaged.

### 6.2 Typical Differential Input Clock

For example, Figure 36 shows a typical LVPECL driver and differential input. If the power of the driver ( $V_{CCO}$ ) is turned on before the input supply ( $V_{CCI}$ ), there is a possibility that the input current could exceed the limit and damage diode D1.

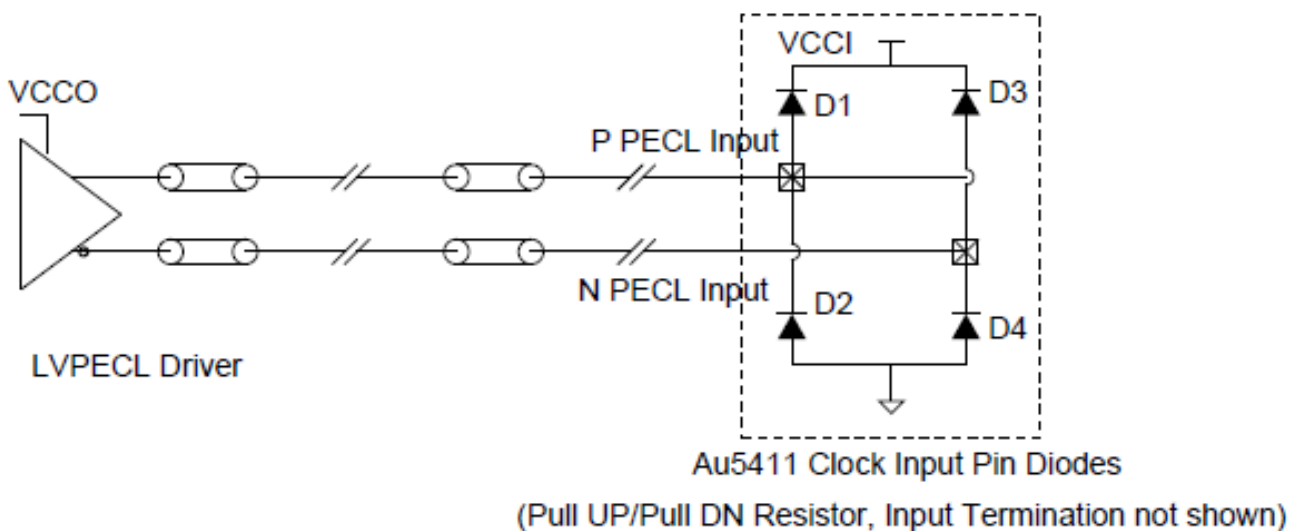


Figure 36 Typical input differential clock

To ensure the input current does not exceed its limit and damage the device, a current limiting resistor can be used. Below are examples of the most common termination topologies using a series current limiting resistor. Though it's not necessary, but if board space allows, some of the examples have an optional 100pf capacitor which assists with the integrity of the rise time. It is also recommended that the current limiting resistor be as close to the receiver as possible.

### 6.3 Input Clock Termination with Hot Swap Protection

#### 6.3.1 LVPECL Termination Example

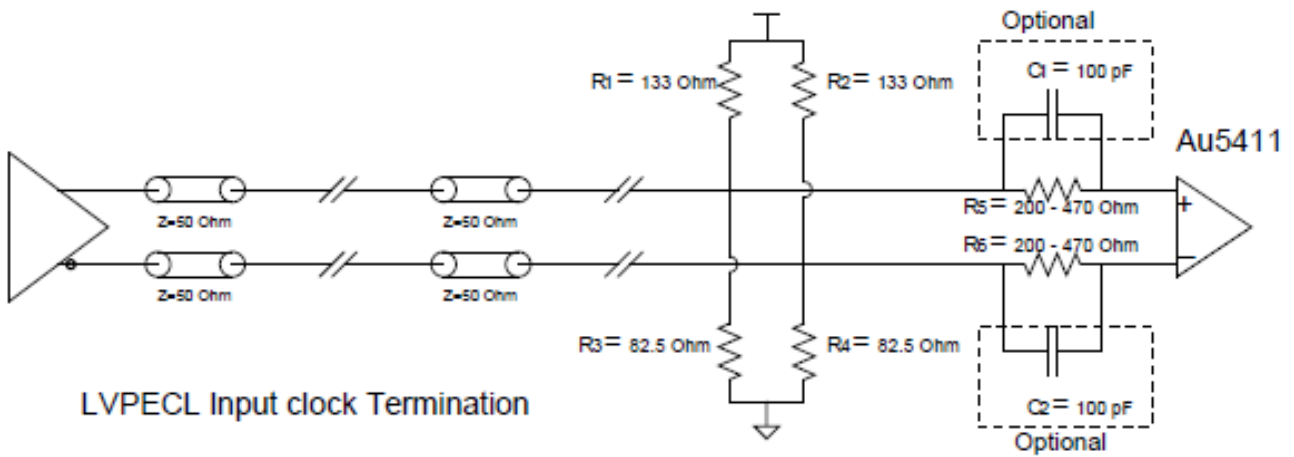


Figure 37 LVPECL termination with hot swap protection

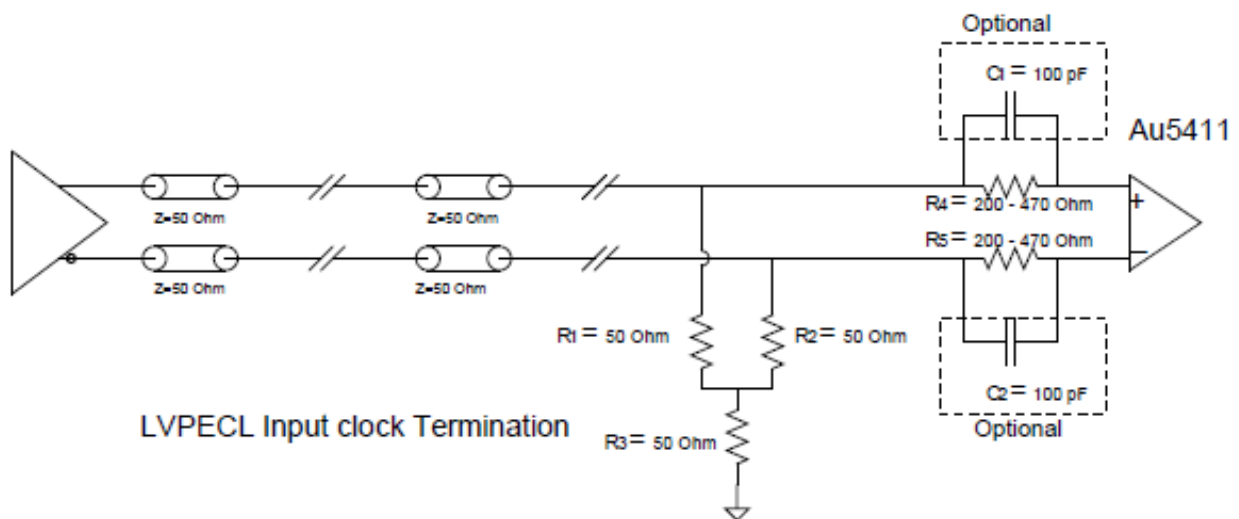


Figure 38 LVPECL termination with hot swap protection



### 6.3.2 LVDS Input Clock Termination Example

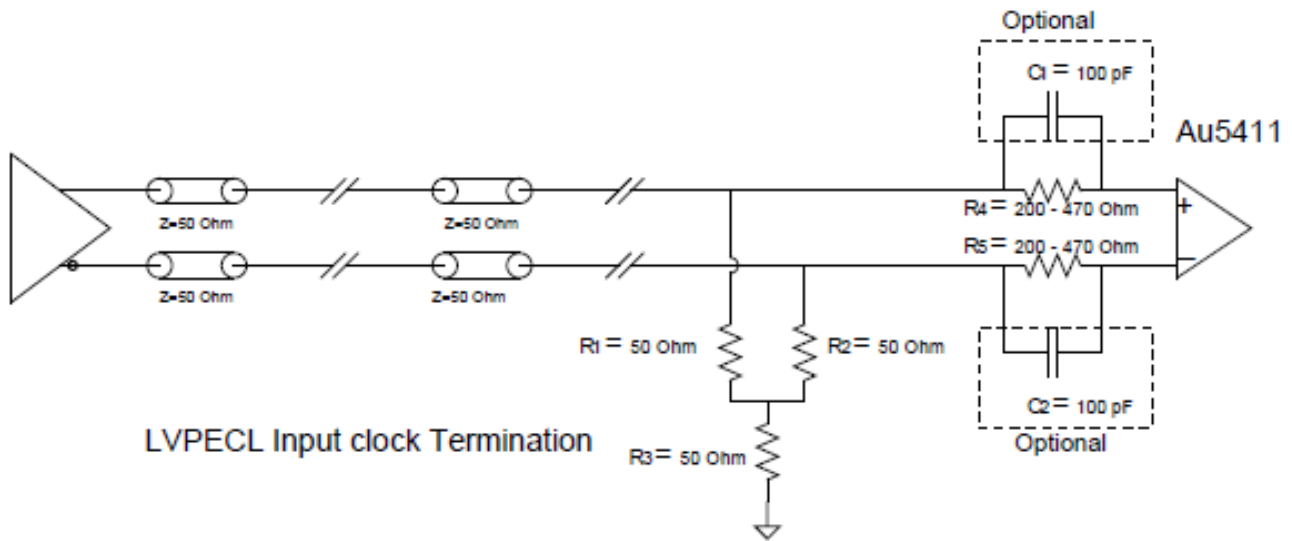


Figure 39 LVDC termination with hot swap protection

### 6.3.3 HCSL Input Clock Termination Example

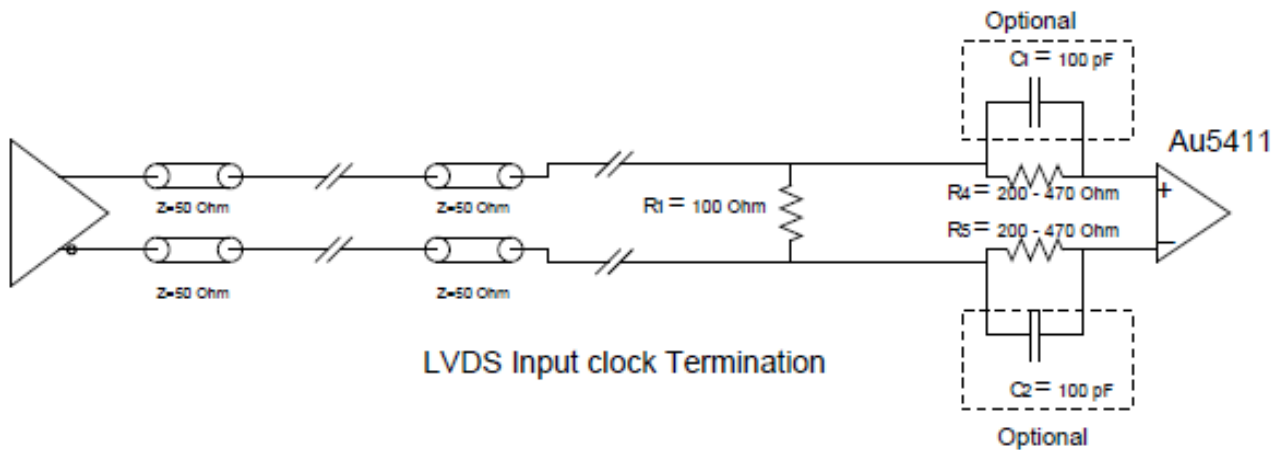


Figure 40 HCSL termination with hot swap protection

6.3.4 LVCMOS Input Clock Termination with Hot Swap Protection

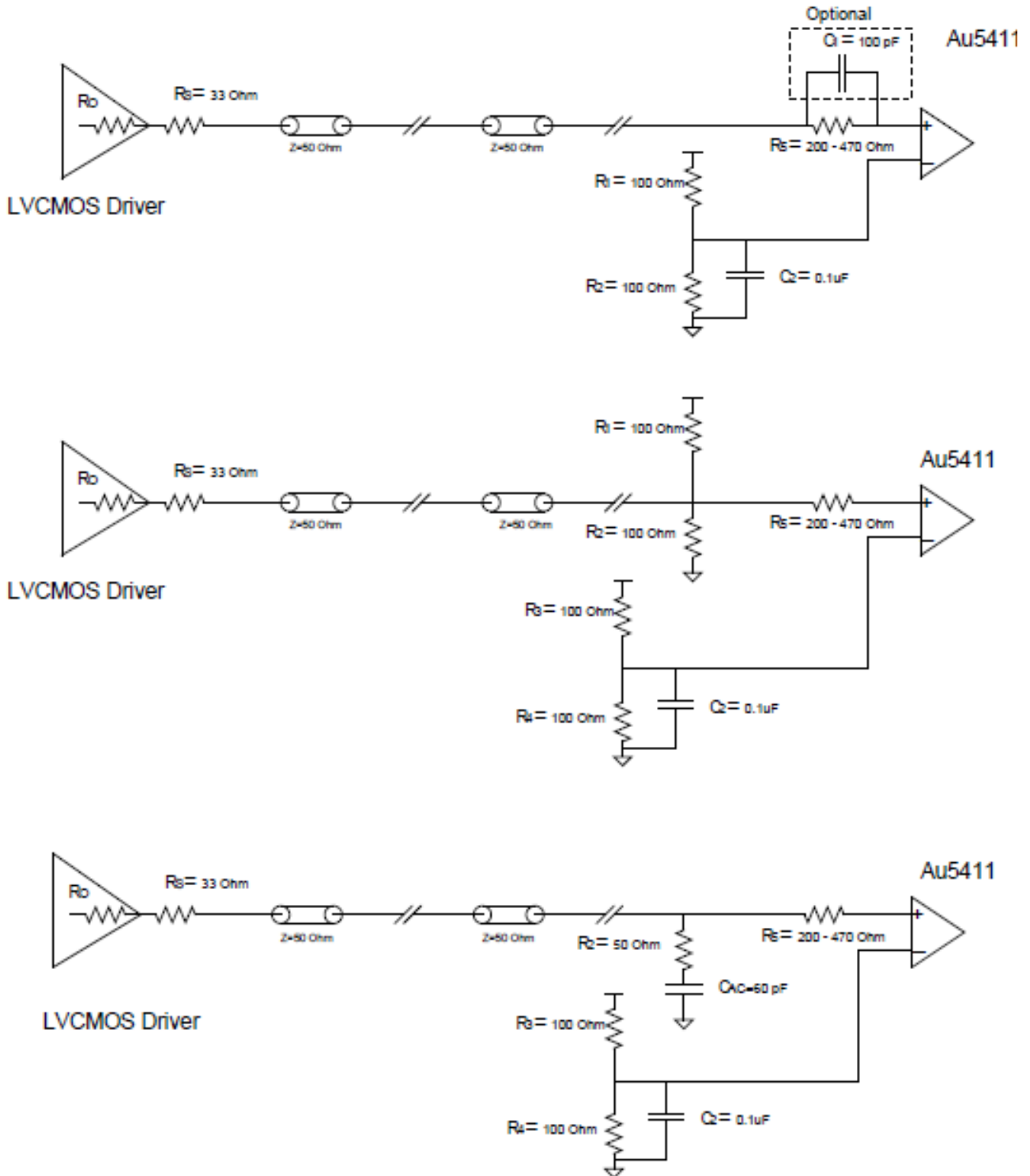


Figure 41 LVCMOS input clock termination with hot swap protection

### 6.4 LVCMOS Output Clock Termination with Hot Swap Protection

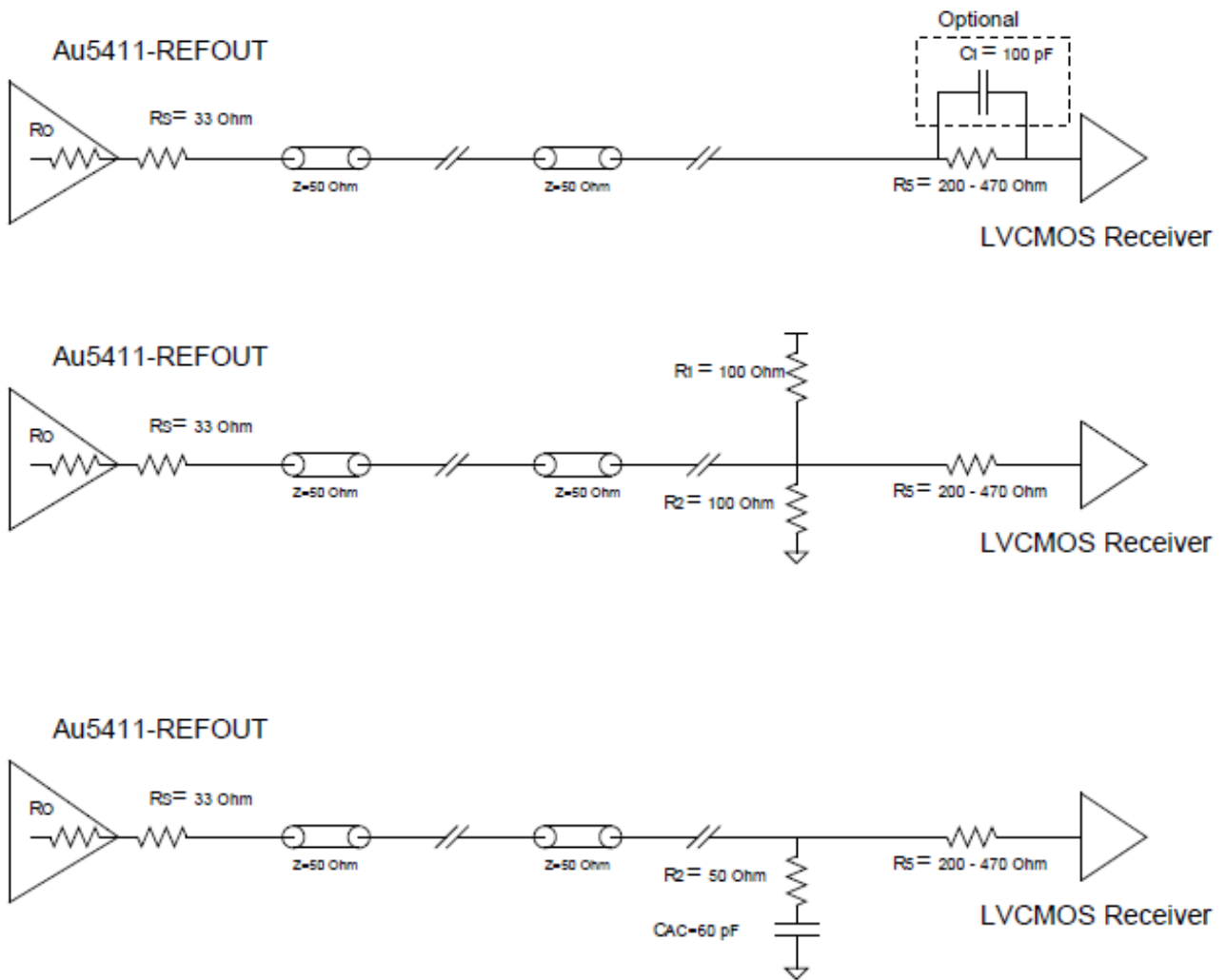


Figure 42 Different types of LVCMOS output clock termination with hot swap protection.

## 7 Parameter Measurement Information

### 7.1 Differential Input Level

The parameter definitions related to differential input level is shown below.

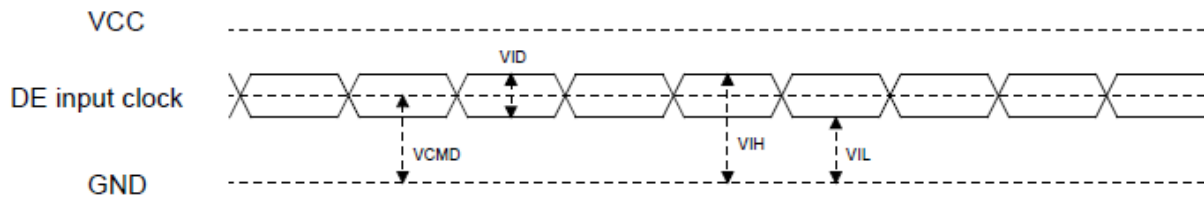


Figure 43 Parameters related to differential input level

### 7.2 Differential Output Level

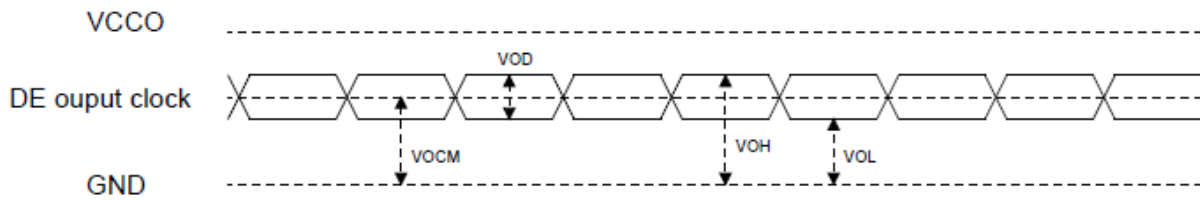


Figure 44 Parameters related to differential output clock levels

### 7.3 Skew and Input to Output Delay

The parameter definitions related to propagation delay and skew are shown below.

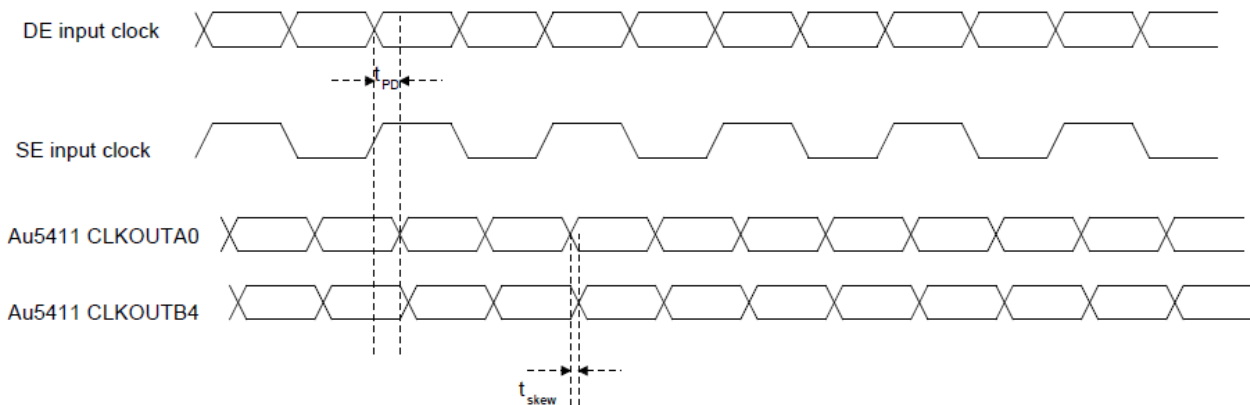


Figure 45 Parameter definitions of propagation delay and skew

### 7.4 Rise and Fall Times

The parameter definitions related to propagation rise and fall times are shown below.

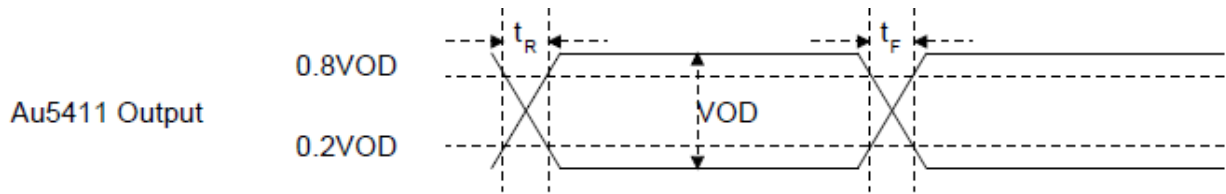


Figure 46 Parameter definitions related to rise and fall times

### 7.5 Isolation

Isolation is a measure of the coupling of clock toggling in unselected input clock path on the output clock. Let us say that CLOCK0 path is selected and there the clock frequency is 156.5 MHz at 0 dBm power. If a clock is toggling in CLOCK1 path at 156 MHz at 0 dBm, then we there may be a tone at an offset of 0.5 MHz from the carrier, in the output clock. The power of this tone with respect to the carrier is called isolation.

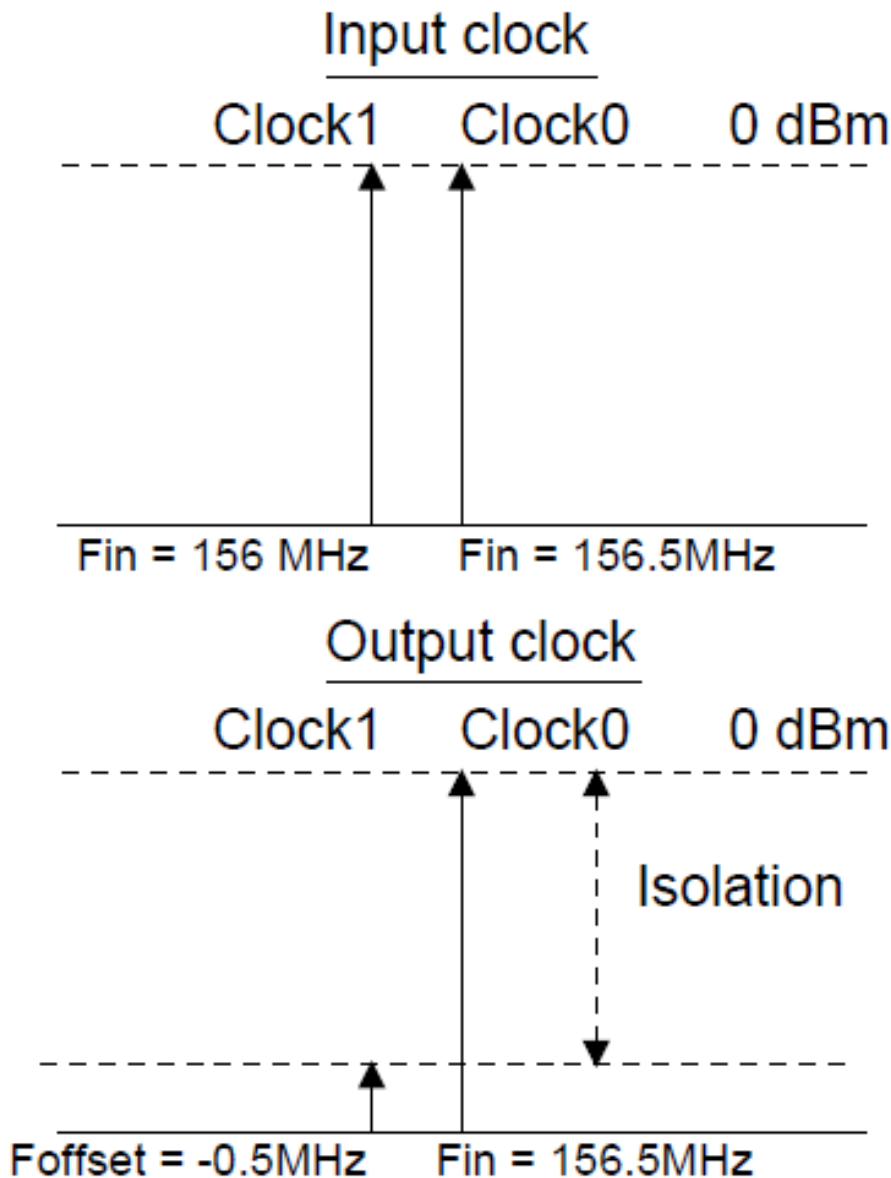


Figure 47 Parameter definition of isolation

### 7.6 Operation in Multiple VCCO Supply Domains

The VCCOA pins, 5 and 8 on the left side are shorted internally. These pins along with ODR CLKOUTA0 to CLKOUTA4 belong to a single supply domain. The VCCOB pins, 32 and 29 on the right side are shorted internally. These pins along with ODR CLKOUTB0 to CLKOUTB4 belong to a single supply domain. These two supply domains are totally independent of each other. Pin 5, 8 can be connected to say 3.3 V while pin 32, 29 can be connected to 2.5 V. In this example, CLKOUTA0 to CLKOUTA4 will be 3.3 V output driver. CLKOUTB0 to CLKOUTB4 will be 2.5 V output driver.

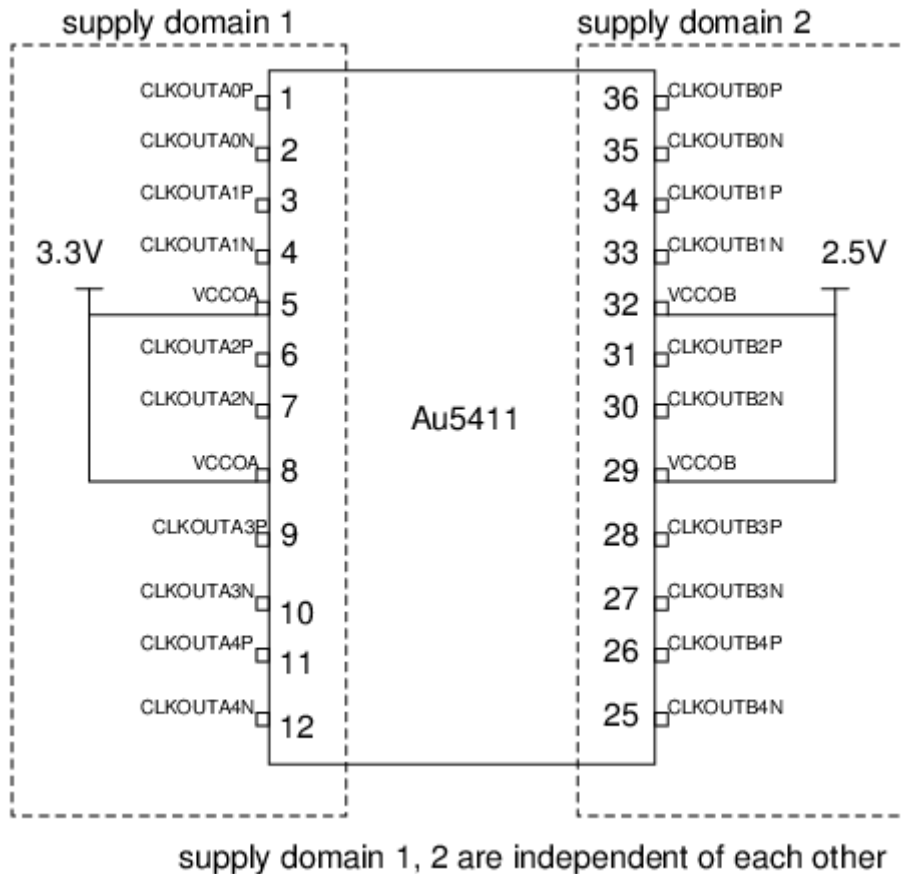
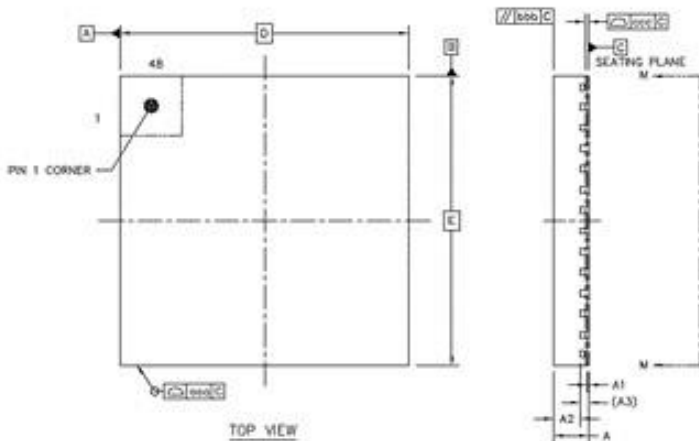
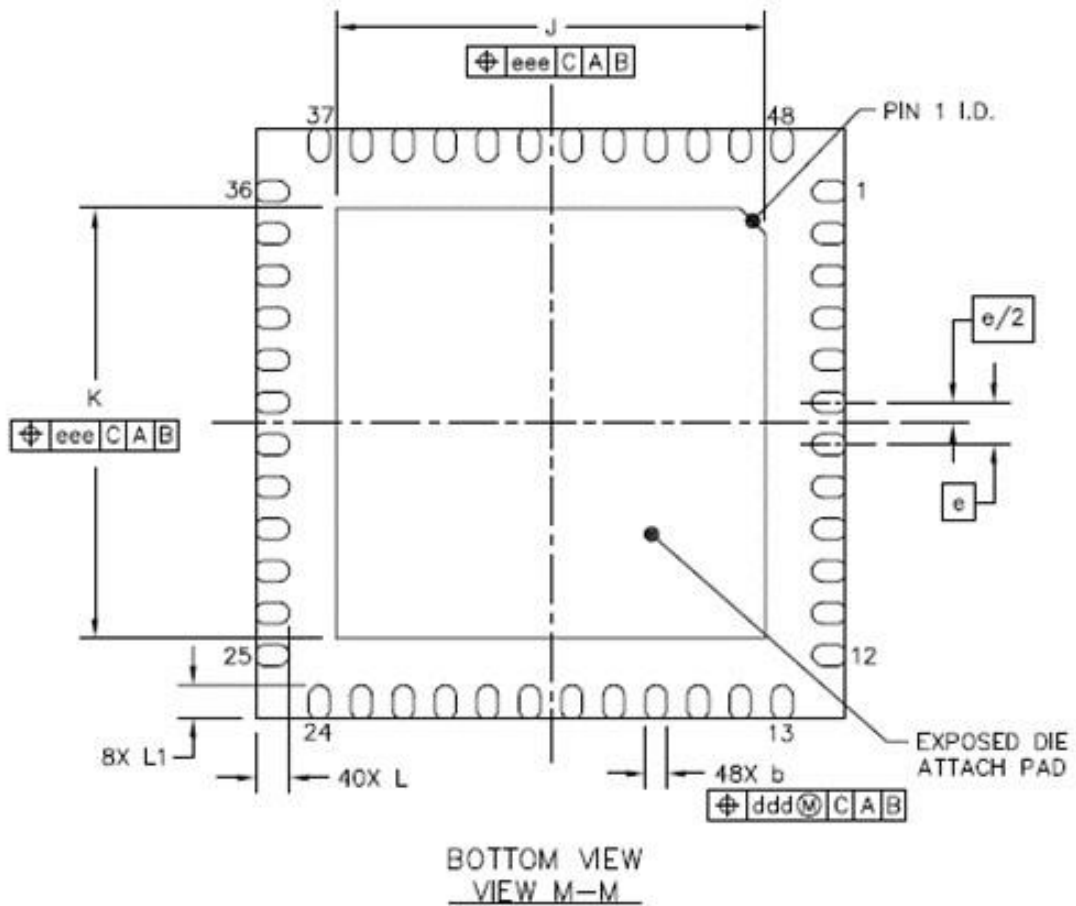


Figure 48: Multi Supply operation of Au5411

### 8 Package Information



|                        | SYMBOL | MIN     | NOM       | MAX  |
|------------------------|--------|---------|-----------|------|
| TOTAL THICKNESS        | A      | 0.8     | 0.85      | 0.9  |
| STAND OFF              | A1     | 0       | 0.035     | 0.05 |
| MOLD THICKNESS         | A2     | ---     | 0.65      | ---  |
| L/F THICKNESS          | A3     | ---     | 0.203 REF | ---  |
| LEAD WIDTH             | b      | 0.2     | 0.25      | 0.3  |
| BODY SIZE              | X D    | 7 BSC   |           |      |
|                        | Y E    | 7 BSC   |           |      |
| LEAD PITCH             | e      | 0.5 BSC |           |      |
| EP SIZE                | X J    | 5       | 5.1       | 5.2  |
|                        | Y K    | 5       | 5.1       | 5.2  |
| LEAD LENGTH            | L      | 0.35    | 0.4       | 0.45 |
|                        | L1     | 0.3     | 0.4       | 0.45 |
| PACKAGE EDGE TOLERANCE | aaa    | 0.1     |           |      |
| MOLD FLATNESS          | bbb    | 0.1     |           |      |
| COPLANARITY            | ccc    | 0.08    |           |      |
| LEAD OFFSET            | ddd    | 0.1     |           |      |
| EXPOSED PAD OFFSET     | eee    | 0.1     |           |      |
|                        |        |         |           |      |
|                        |        |         |           |      |
|                        |        |         |           |      |
|                        |        |         |           |      |

Figure 49 Au5411 48 pin, 7x7 QFN package dimensions

Notes:

- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only.
- This drawing is subject to change without notice.
- The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

## 9 Ordering Information

**Table 16 Ordering Information for Au5411**

| Ordering Part Number (OPN) | Marking | Package               | Shipping Package | Temp. Range     |
|----------------------------|---------|-----------------------|------------------|-----------------|
| Au5411A-QMR <sup>(1)</sup> | Au5411A | 48 QFN<br>7 mm x 7 mm | Tape and Reel    | -40 °C to 85 °C |
| Au5411A-QMT <sup>(1)</sup> | Au5411A | 48 QFN<br>7mm x 7mm   | Tray             | -40 °C to 85 °C |
| Au5411A-EVB                | —       | —                     | Evaluation Board | —               |

Notes:

1. Add an R at the end of the OPN to denote tape and reel ordering option. Add a T at the end of the OPN to denote tray ordering option.



## 10 Revision History

**Table 17 Revision History**

| Version | Date                       | Description  | Author    |
|---------|----------------------------|--|-----------|
| 0.1     | 31 May 2018                | Au5411 Datasheet<br>First Draft  | Aura Semi |
| 0.2     | 11 Jan 2019                | Removed '-' from part number<br>Added foot notes where ever applicable<br>Expanded input clock configurations<br>Expanded output clock configurations<br>Component values specified in application diagrams<br>Added diagram for REFOUT enable and disable   | Aura Semi |
| 0.3     | 16 Jan 2019                | Added VCCO voltage information for PSRR  | Aura Semi |
| 0.4     | 23 Jan 2019                | Added hot swap recommendations   | Aura Semi |
| 0.5     | 28 Jan 2019                | Added section on parameter definitions for more clarity on data sheet parameters   | Aura Semi |
| 0.6     | 20 Feb 2019                | Added diagram for HCSL AC coupled output termination   | Aura Semi |
| 0.7     | 04 Apr 2019                | Updated HCSL VOH/VOL limits  | Aura Semi |
| 0.8     | 05 May 2019                | Updated figure 29 to add Au5411 in LVDS mode driving CML receiver  | Aura Semi |
| 0.9     | 2 Jun 2019                 | Updated the chip current data sheet limits to center them.<br>LVPECL VOD lower limit changed to 475mV.<br>Added clarification on VIH, VIL in single ended DC case  | Aura Semi |
| 0.91    | 5 Jun 2019                 | Removed 1.8V support on VCC, VCCOA, VCCOB<br>Updated typical values of PSRR<br>Updated typical values of rise/fall times across LVPECL, LVDS, HCSL<br>Operation of Au5411 in multi supply domain scenario is added<br>Updated output duty cycle of LVCMOS driver for 200MHz < Fin < 250 MHz to 40 to 60%<br>Updated typical propagation delay across all output standards.<br>Added crystal mode jitter  | Aura Semi |
| 0.92    | 10 Jul 2019                | Upper limit of core current updated by 0.3mA<br>Core switching current value stated at 2100 MHz<br>Upper limit of HCSL, LVDS current updated by 1mA<br>Typical values of PN noise floor updated to match with char data<br>Max value of IN/OUT delay added as per char data<br>LVCMOS specification changed to match requirement of 50 Ω driver<br>Added Rs=0 in the application diagram and its description of LVCMOS<br>Updated LVPECL AC input termination<br>Changed Draft to Limited production release<br>Updated upper limit of LVPECL swing.<br>Updated ordering information<br>Added more explanation to crystal swing in AC coupled mode | Aura Semi |
| 0.93    | 7 <sup>th</sup> Sept 2020  | Ordering Information Table 16 Updated<br>Datasheet Updated with Aura Latest Format   | Aura Semi |
| 0.94    | 25 <sup>th</sup> Sept 2020 | Updated the Missing Package Dimension Table in Section 8: Package Information  | Aura Semi |

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## 11 Trademarks

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## 12 Contact Information

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