PCN Number: 201		20180913003		PCN Date:			September 18, 2018								
Title:	Title: Datasheet for TMS320C28341 - TMS320C28346														
Custon	ner Contact:	PCN I	Manager				De	ep	t:	Quality Services					
Propos	ed 1 st Ship Da	te:	March	18	3, 2019										
Change	е Туре:														
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Ass	sembly Process			\boxtimes	Data Sheet				Wafer	Bump Material					
	sembly Materials				Part number cha	inge			Wafer	Bump Process					
Me	chanical Specifi	catior	1		Test Site				Wafer	Fab Site					
Pac	cking/Shipping/	Label	ing		Test Process				Wafer	Fab Materials					
									Wafer	Fab Process					
				N	lotification De	etails									
Descri	ption of Chang	e:													
The pro	duct datasheet(s) is	being u	pda	ated as summarize	ed below.	The	e f	ollowin	ig change history					
provide	s further details														
The dat	asheet number	will h	e chanc	nin	٦										
	The datasheet number will be changing.														
THE dat	asricet namber	*******	c chang	, <u>s</u>											
		viii b	e chang	, <u>:</u>	1	TMS320C2	834	16,	TMS32	0C28345, TMS320C2834	14				
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•		ded section.		
:		ded section. Added section.		
•	Section 5.6 (Electrical Characteristics): Change	ged MAX IIL (Pin with pullup enabled) from -1	30 μA to -100 μA	33
:	Section 5.9.2 (Power Sequencing): Updated Section 5.9.2.1 (Power Management and Sur	"No voltage larger than a diode drop" parage pervisory Circuit Solutions): Updated section	rapn	39
•	Table 5-21 (High-Resolution PWM Character	istics at SYSCLKOUT = (150-300 MHz)): Upd	ated footnote	51
•	Section 5.9.4.5.1 (Master Mode Timing): Upd	ated sectionted section.		55
•	Section 5.9.4.6.2 (McBSP as SPI Master or S	Slave Timing): Replaced "For all SPI slave mod	des" paragraphs	- 1
	with "For all SPI slave modes" table footnot Table 5-36 (McBSP as SPI Master or Slave T	rites	= 0)): Added "For all	63
	SPI slave modes" footnote	Fiming Requirements (CLKSTP = 11b, CLKXP	= 0)); Added "For all	63
	SPI slave modes" footnote	Fiming Dequirements (CLVSTD = 10b, CLVVD	= 1)): Added "For all	64
•	SPI slave modes" footnote			65
•		Fiming Requirements (CLKSTP = 11b, CLKXP		66
				00
•	Section 5.9.6.1 (USEREADY = 0): Updated "X XRDACTIVE value from "≥ 5" to "≥ 6"	Triving register configuration restrictions" (at		68
•	Section 5.9.6.1 (USEREADY = 0): Updated "E XRDACTIVE value from "5" to "6"	examples of valid and invalid timing" table by o	hanging Valid	68
	Section 5.9.6.2 (Synchronous Mode (USEREA		ING register	00
	configuration restrictions" table by changing X			00
	"≥ 1" to "≥ 2" Section 5.9.6.2 (Synchronous Mode (USEREA			<u>69</u>
	invalid timing" table by changing Valid XRDAC			co
	to "2" Section 5.9.6.3 (Asynchronous Mode (USERE	ADY = 1, READYMODE = 1)); Updated "XTIN	MING register	69
	configuration restrictions" table by changing X	RDACTIVE value from "≥ 5" to "≥ 6"; XWRAC	TIVE value from	-
	"≥ 3" to "≥ 4"; and XWRTRAIL value from "0" t Section 5.9.6.3 (Asynchronous Mode (USERE			<u>70</u>
	invalid timing" table by changing Valid XRDAC	CTIVE value from "5" to "6" and Valid XWRAC	TIVE value from "3"	-11
	to "4" Section 5.9.6.4 (XINTF Signal Alignment to XC			$\frac{70}{72}$
	Section 5.9.6.4: Updated "For the case where	XCLKOUT = one-half" paragraph		72
•	Section 6.1.9 (Security): Updated "Custom se			
	Section 6.1.9: Added Code Security Module D Table 6-3 (ePWM1-4 Control and Status Regis			88
	TZCLR, and TZFRC.			97
	Table 6-4 (ePWM5-9 Control and Status Red	gisters): Added reference to footnote for TZSEL	TZCTI TZEINT	
	TZCLR, and TZFRC.	PI) Module (SPI-A, SPI-D)): Updated "Rising e	.,,,	98
•	Section 6.2.11 (Serial Peripheral Interface (S	PI) Module (SPI-A, SPI-D)): Updated "Rising e	edge with phase	118
•	Figure 6-32 (Watchdog Module): Updated fig	ure		152
•		Layout): Added section.		154
•		ort): Added section.		
:	Figure 8-1 (Example of C2834x Device Nome	onenclature): Updated figure.	••••••	156
	Section 8.3 (Tools and Software): Added sec	tion		157
•	Section 8.4 (Documentation Support): Update	ed section		159
•	Section 9 (Mechanical, Packaging, and Orde	rable Information): Added section		163
<u>Th</u>	e datasheet number will be changing.			_
D	evice Family	Change From:	Change To:	1
_	MS320C28341 - TMS320C28346	SPRS516D	SPRS516E	
- .				
Ι'n	ese changes may be reviewed at the o	jarasheet links provided.		

http://www.ti.com/product/TMS320C28341

Reason for Change:

To more accurately reflect device characteristics.

Anticipated impact on Fit, Form, Function, Quality or Reliability (positive / negative):

Electrical specification performance changes as indicated above.

Changes to product identification resulting from this PCN:

None.

Product Affected:

TMS320C28341ZHHT	TMS320C28342ZFET	TMS320C28343ZFEQ	TMS320C28343ZHHT
TMS320C28344ZFET	TMS320C28345ZFET	TMS320C28345ZHHT	TMS320C28346ZFEQ
TMS320C28346ZFET			

For questions regarding this notice, e-mails can be sent to the regional contacts shown below or your local Field Sales Representative.

Location	E-Mail
USA	PCNAmericasContact@list.ti.com
Europe	PCNEuropeContact@list.ti.com
Asia Pacific	PCNAsiaContact@list.ti.com
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