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•	Deleted higher order poles information	
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•	Added PLL2 DLD programming information and updated the PLLx DLD flowchart graphic	
•	Changed PLL1_STORAGE_CELL description from 40-bit thermometer code to 6-bit decimal value	
•	Clarified CTRL_VCXO represented as PLL1_STORAGE_CELL value	
•	Changed section from: Low Skew Mode to: Zero Delay Mode (ZDM)	
•	Changed CLKout7 to CLKout6 and CLKout8 to CLKout9 for zero delay feedback clocks.	
•	Changed Set Prop/Store-CP from "fast lock" value to "non-fast lock" value at end of flowchart	
•	Deleted references to tunable crystal	
•	Deleted use of external VCO for PLL2	
•	Added register 0x85, 0x86, 0xF6, and 0xAD for PLL2 DLD to recommended programming sequence	58
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•	Changed PLL2_PROP from 8 bit to 6 bit field in register map	
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•	Changed PLL2_PROP field size from 8 bits to 6 bits in register definition	
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•	Added definition and requirement for setting PLL2_LD_WNDW_SIZE_INITIAL = 0 in register 0x86 definition	

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The datasheet number will be changing.							
Device Family Change From: Change To:							
LMK04616 SNAS663A SNAS663B							
http://www.ti.com/product/LMK04616							
Reason for Change:							
To accurately reflect device characteristics.							
Anticipated impact on Fit, Form, Function, Quality or Reliability (positive / negative):							
Electrical specification performance changes as indicated above.							
Changes	to product ide	entification re	esulting fr	om this PCN	l:		
None.							
Product A	ffected:						
LMK04616ZCRR LMK04616ZCRT							

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