



P-CHANNEL ENHANCEMENT MODE MOSFET

Product Summary

BV _{DSS}	R _{DS(ON)} Max	I _D Max T _A = +25°C
	4.0mΩ @ V _{GS} = -10V	-16.2A
-30V	6.5mΩ @ V _{GS} = -4.5V	-12.8A

Description and Applications

This MOSFET is designed to minimize the on-state resistance (R_{DS(ON)}) yet maintain superior switching performance, which makes it ideal for high-efficiency power management applications.

- Backlighting
- Power Management Functions
- DC-DC Converters

Features and Benefits

- Low On-Resistance
- Low Input Capacitance
- Fast Switching Speed
- ESD Protected Gate
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- Qualified to AEC-Q101 Standards for High Reliability

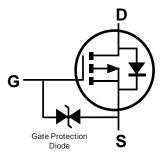
Mechanical Data

- Case: SO-8
- Case Material: Molded Plastic, "Green" Molding Compound.
 UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections Indicator: See Diagram Below
- Terminals: Finish—Matte Tin Annealed Over Copper Lead Frame.
 Solderable per MIL-STD-202, Method 208 23
- Weight: 0.074 grams (Approximate)

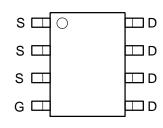




Top View



Internal Schematic



Top View Pin Configuration

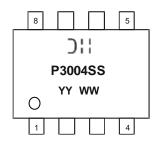
Ordering Information (Note 4)

Part Number	Case	Packaging
DMP3004SSS-13	SO-8	2500/Tape & Reel

Notes:

- 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
- 2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- 4. For packaging details, see https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information



];; = Manufacturer's Marking P3004SS = Product Type Marking Code YYWW = Date Code Marking YY or YY= Year (ex: 17 = 2017) WW = Week (01 to 53)



Maximum Ratings (@ $T_A = +25^{\circ}C$, unless otherwise specified.)

Characteristic			Symbol	Value	Unit	
Drain-Source Voltage	V_{DSS}	-30	V			
Gate-Source Voltage			V_{GSS}	±20	V	
Continuous Drain Compant V 40V (Nata C)	Steady State	$T_A = +25$ °C $T_A = +70$ °C	ı	-16.2 -13.0	Α	
Continuous Drain Current, V _{GS} = 10V (Note 6)	t < 10s	$T_A = +25$ °C $T_A = +70$ °C	l _D	-23.4 -18.7		
Maximum Continuous Body Diode Forward Currer	Is	-1.8	Α			
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1	I _{DM}	-110	Α			
Avalanche Current, L=0.1mH (Note 7)	I _{AS}	-44	Α			
Avalanche Energy, L=0.1mH (Note 7)	Eas	98	mJ			

Thermal Characteristics

Characteristic		Symbol	Value	Unit	
Total Power Dissipation (Note 5)	T _A = +25°C	P_{D}	1.2	W	
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	D	103	- °C/W	
Thermal Resistance, Junction to Ambient (Note 5)	t<10s	$R_{\Theta JA}$	50		
Total Power Dissipation (Note 6)	T _A = +25°C	P_{D}	1.6	W	
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	D	79	°C/W	
Thermal Resistance, Junction to Ambient (Note 6)	t < 10s	$R_{\Theta JA}$	38		
Thermal Resistance, Junction to Case (Note 6)		$R_{\Theta JC}$	11	°C/W	
Operating and Storage Temperature Range		T _{J,} T _{STG}	-55 to +150	°C	

Electrical Characteristics (T_A = +25°C, unless otherwise specified.)

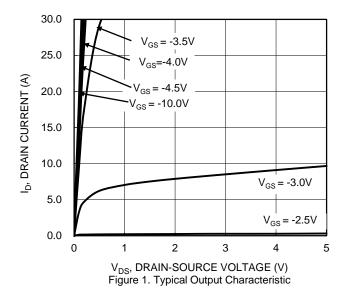
Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition	
OFF CHARACTERISTICS (Note 8)							
Drain-Source Breakdown Voltage	BV _{DSS}	-30	_	_	٧	$V_{GS} = 0V, I_D = -250\mu A$	
Zero Gate Voltage Drain Current	I _{DSS}		_	-1	μΑ	$V_{DS} = -30V$, $V_{GS} = 0V$	
Gate-Source Leakage	I _{GSS}	_	_	±10	μA	$V_{GS} = \pm 20V, V_{DS} = 0V$	
ON CHARACTERISTICS (Note 8)	ON CHARACTERISTICS (Note 8)						
Gate Threshold Voltage	V _{GS(TH)}	-1.0	_	-2.5	V	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	
Static Drain-Source On-Resistance	J		3.2	4.0	mΩ	V _{GS} = -10V, I _D = -20A	
Static Dialii-Source Oil-Resistance	R _{DS(ON)}	1	5.2	6.5	11122	$V_{GS} = -4.5V, I_D = -15A$	
Diode Forward Voltage	V_{SD}		-0.7	-1.2	V	V _{GS} = 0V, I _S = -1A	
DYNAMIC CHARACTERISTICS (Note 9)	DYNAMIC CHARACTERISTICS (Note 9)						
Input Capacitance	C _{iss}		7693	_	pF	., ., ., .,	
Output Capacitance	Coss		1426	_	pF	$V_{DS} = -15V, V_{GS} = 0V,$ f = 1.0MHz	
Reverse Transfer Capacitance	C _{rss}	1	966	_	pF	1 = 1.01/11/2	
Gate Resistance	R_g		5.4	_	Ω	$V_{DS} = 0V, V_{GS} = 0V, f = 1.0MHz$	
Total Gate Charge (V _{GS} = -4.5V)	Qg		73	_	nC		
Total Gate Charge (V _{GS} = -10V)	Qg	_	156	_	nC	1577 1 000	
Gate-Source Charge	Q _{gs}	_	23	_	nC	$V_{DS} = -15V, I_{D} = -20A$	
Gate-Drain Charge	Q _{gd}		34	_	nC		
Turn-On Delay Time	t _{D(ON)}		8.3	_	ns		
Turn-On Rise Time	t _R	-	6.8	_	ns	$V_{DD} = -15V, V_{GS} = -10V,$	
Turn-Off Delay Time	t _{D(OFF)}	_	267	_	ns	$R_g = 1\Omega$, $I_D = -20A$	
Turn-Off Fall Time	t _F	_	223	_	ns		
Reverse Recovery Time	t _{RR}	_	31	_	ns	1 400 dl/dt 4000/u-	
Reverse Recovery Charge	Q _{RR}	_	25	_	nC	$I_F = -10A$, $dI/dt = 100A/\mu s$	

Notes:

- 5. Device mounted on FR-4 PC board, with minimum recommended pad layout, single sided.
 6. Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate.
- 7. I_{AS} and E_{AS} rating are based on low frequency and duty cycles to keep $T_J = +25^{\circ}C$. 8. Short duration pulse test used to minimize self-heating effect.
- 9. Guaranteed by design. Not subject to product testing.







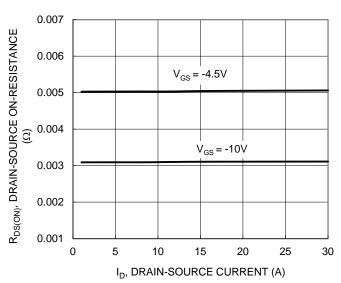


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

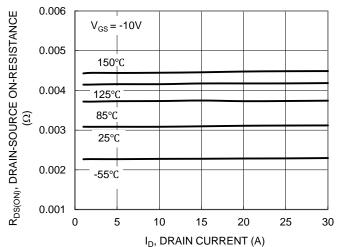
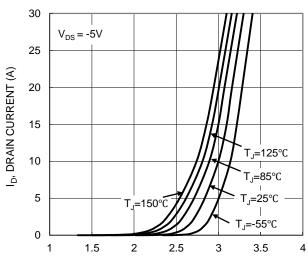


Figure 5. Typical On-Resistance vs. Drain Current and Junction Temperature



V_{GS}, GATE-SOURCE VOLTAGE (V) Figure 2. Typical Transfer Characteristic

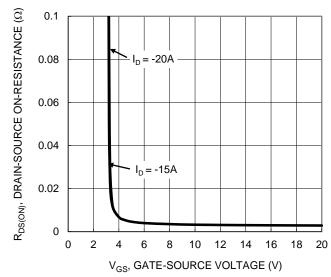
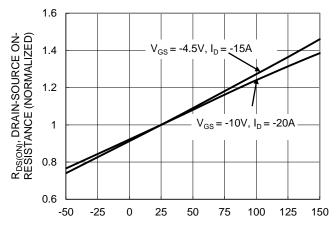


Figure 4. Typical Transfer Characteristic



T_J, JUNCTION TEMPERATURE (°C) Figure 6. On-Resistance Variation with Junction Temperature



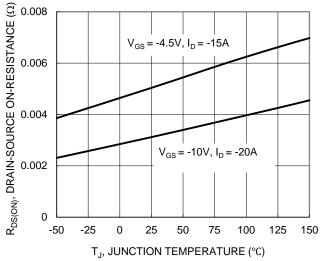
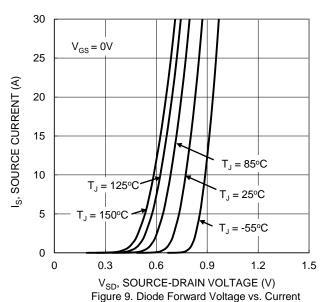


Figure 7. On-Resistance Variation with Junction Temperature

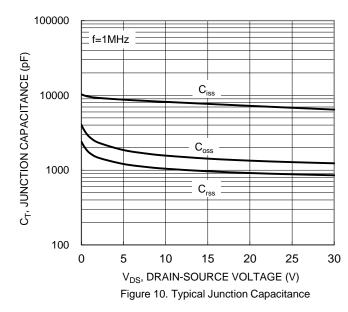


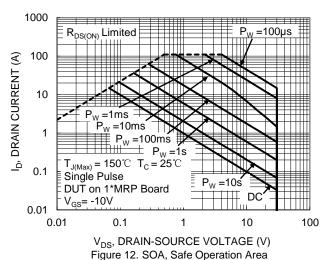
8 6 V_{GS} (V) 4 $V_{DS} = -15V, I_{D} = -20A$ 2 20 40 60 0 80 100 120 140 160 Qg (nC)

Figure 11. Gate Charge

2.5 $V_{\text{GS}(\text{TH})},$ GATE THRESHOLD VOLTAGE (V) 2.2 $I_D = -1 \text{mA}$ 1.9 $I_{D} = -250 \mu A$ 1.6 1.3 -25 25 50 75 125 150 -50 100 T_J, JUNCTION TEMPERATURE (°C)

Figure 8. Gate Threshold Variation vs. Junction Temperature





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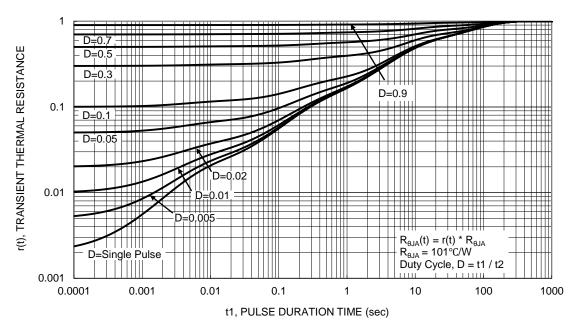
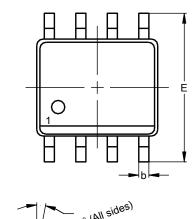


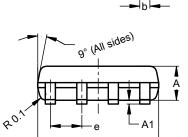
Figure 13. Transient Thermal Resistance

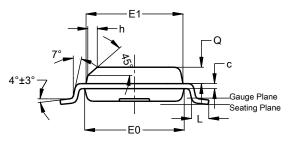


Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.







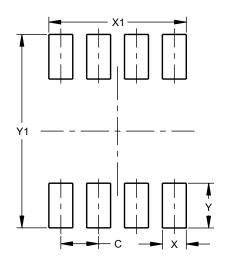
SO-8

SO-8

SO-8					
Dim	Min	Max	Тур		
Α	1.40	1.50	1.45		
A1	0.10	0.20	0.15		
b	0.30	0.50	0.40		
С	0.15	0.25	0.20		
D	4.85	4.95	4.90		
Е	5.90	6.10	6.00		
E1	3.80	3.90	3.85		
E0	3.85	3.95	3.90		
е			1.27		
h	-		0.35		
L	0.62	0.82	0.72		
ø	0.60	0.70	0.65		
All Dimensions in mm					

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.



Dimensions	Value (in mm)
С	1.27
Х	0.802
X1	4.612
Y	1.505
V1	6.50

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