Data Sheet | July 5, 2007 | FN7185.3

30MHz Rail-to-Rail Input-Output Op Amps

The EL5210 and EL5410 are low power, high voltage rail-to-rail input-output amplifiers. The EL5210 contains two amplifiers in one package and the EL5410 contains four amplifiers. Operating on supplies ranging from 5V to 15V, while consuming only 2.5mA per amplifier, the EL5410 and EL5210 have a bandwidth of 30MHz (-3dB). They also provide common mode input ability beyond the supply rails, as well as rail-to-rail output capability. This enables these amplifiers to offer maximum dynamic range at any supply voltage.

The EL5410 and EL5210 also feature fast slewing and settling times, as well as a high output drive capability of 30mA (sink and source). These features make these amplifiers ideal for high speed filtering and signal conditioning application. Other applications include battery power, portable devices, and anywhere low power consumption is important.

The EL5410 is available in a space-saving 14 Ld TSSOP package, as well as the industry-standard 14 Ld SOIC. The EL5210 is available in the 8 Ld MSOP and 8 Ld SOIC packages. Both feature a standard operational amplifier pin out. These amplifiers operate over a temperature range of -40°C to +85°C.

Features

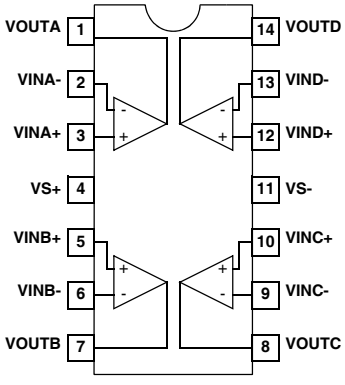
- 30MHz -3dB bandwidth
- Supply voltage = 4.5V to 16.5V
- Low supply current (per amplifier) = 2.5mA
- High slew rate = 33V/µs
- Unity-gain stable
- Beyond the rails input capability
- Rail-to-rail output swing
- Available in both standard and space-saving fine pitch packages
- Pb-free plus anneal available (RoHS compliant)

Applications

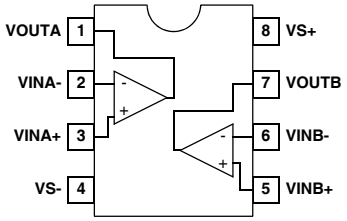
- Driver for A-to-D Converters
- Data Acquisition
- Video Processing
- Audio Processing
- Active Filters
- Test Equipment
- Battery Powered Applications
- Portable Equipment

Pinouts

EL5410
(14 LD TSSOP, SOIC)
TOP VIEW



EL5210
(8 LD MSOP, SOIC)
TOP VIEW



Ordering Information

PART NUMBER	PART MARKING	PACKAGE	PKG. DWG. #
EL5210CS	5210CS	8 Ld SOIC	MDP0027
EL5210CS-T7*	5210CS	8 Ld SOIC	MDP0027
EL5210CS-T13*	5210CS	8 Ld SOIC	MDP0027
EL5210CSZ (Note)	5210CSZ	8 Ld SOIC (Pb-free)	MDP0027
EL5210CSZ-T7* (Note)	5210CSZ	8 Ld SOIC (Pb-free)	MDP0027
EL5210CSZ-T13* (Note)	5210CSZ	8 Ld SOIC (Pb-free)	MDP0027
EL5210CY	J	8 Ld MSOP	MDP0043
EL5210CY-T7*	J	8 Ld MSOP	MDP0043
EL5210CY-T13*	J	8 Ld MSOP	MDP0043
EL5210CYZ (Note)	BATAA	8 Ld MSOP (Pb-free)	MDP0043
EL5210CYZ-T7* (Note)	BATAA	8 Ld MSOP (Pb-free)	MDP0043
EL5210CYZ-T13* (Note)	BATAA	8 Ld MSOP (Pb-free)	MDP0043
EL5410CS	5410CS	14 Ld SOIC	MDP0027
EL5410CS-T7*	5410CS	14 Ld SOIC	MDP0027
EL5410CS-T13*	5410CS	14 Ld SOIC	MDP0027
EL5410CSZ (Note)	5410CSZ	14 Ld SOIC (Pb-free)	MDP0027
EL5410CSZ-T7* (Note)	5410CSZ	14 Ld SOIC (Pb-free)	MDP0027
EL5410CSZ-T13* (Note)	5410CSZ	14 Ld SOIC (Pb-free)	MDP0027
EL5410CR	5410CR	14 Ld TSSOP	MDP0044
EL5410CR-T7*	5410CR	14 Ld TSSOP	MDP0044
EL5410CR-T13*	5410CR	14 Ld TSSOP	MDP0044
EL5410CRZ (Note)	5410CRZ	14 Ld TSSOP (Pb-free)	M14.173
EL5410CRZ-T7* (Note)	5410CRZ	14 Ld TSSOP (Pb-free)	M14.173
EL5410CRZ-T13* (Note)	5410CRZ	14 Ld TSSOP (Pb-free)	M14.173

*"-T7" or "-T13" suffix is for tape and reel. Please refer to TB347 for details on reel specifications.

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Absolute Maximum Ratings (T_A = +25°C)

Supply Voltage between V_S+ and V_S- . . . . . .+18V
Input Voltage . . . . . V_S- - 0.5V, V_S + 0.5V
Maximum Continuous Output Current 30mA

Thermal Information

Storage Temperature . . . . . .-65°C to +150°C
Operating Temperature . . . . . .-40°C to +85°C
Power Dissipation . . . . . See Curves
Maximum Die Temperature . . . . . .+125°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

Electrical Specifications

V_S+ = +5V, V_S- = -5V, R_L = 1kΩ and C_L = 12pF to 0V, T_A = +25°C unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITION	MIN (Note 4)	TYP	MAX (Note 4)	UNIT
INPUT CHARACTERISTICS						
V_{OS}	Input Offset Voltage	V_{CM} = 0V		3	15	mV
TCV_{OS}	Average Offset Voltage Drift (Note 1)			7		µV/°C
I_B	Input Bias Current	V_{CM} = 0V		2	60	nA
R_{IN}	Input Impedance			1		GW
C_{IN}	Input Capacitance			2		pF
CMIR	Common-Mode Input Range		-5.5		+5.5	V
CMRR	Common-Mode Rejection Ratio	for V_{IN} from -5.5V to 5.5V	50	70		dB
A_{VOL}	Open-Loop Gain	-4.5V ≤ V_{OUT} ≤ 4.5V	65	80		dB
OUTPUT CHARACTERISTICS						
V_{OL}	Output Swing Low	I_L = -5mA		-4.9	-4.8	V
V_{OH}	Output Swing High	I_L = 5mA	4.8	4.9		V
I_{SC}	Short Circuit Current			±120		mA
I_{OUT}	Output Current			±30		mA
POWER SUPPLY PERFORMANCE						
PSRR	Power Supply Rejection Ratio	V_S is moved from ±2.25V to ±7.75V	60	80		dB
I_S	Supply Current (Per Amplifier)	No Load		2.5	3.75	mA
DYNAMIC PERFORMANCE						
SR	Slew Rate (Note 2)	-4.0V ≤ V_{OUT} ≤ 4.0V, 20% to 80%		33		V/µs
t_S	Settling to +0.1% (A_V = +1)	(A_V = +1), V_O = 2V Step		140		ns
BW	-3dB Bandwidth			30		MHz
GBWP	Gain-Bandwidth Product			20		MHz
PM	Phase Margin			50		°
CS	Channel Separation	f = 5MHz		110		dB
d_G	Differential Gain (Note 3)	R_F = R_G = 1kΩ and V_{OUT} = 1.4V		0.12		%
d_P	Differential Phase (Note 3)	R_F = R_G = 1kΩ and V_{OUT} = 1.4V		0.17		°

Electrical Specifications $V_S+ = 5V$, $V_S- = 0V$, $R_L = 1k\Omega$ and $C_L = 12pF$ to 2.5V, $T_A = +25°C$ unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITION	MIN (Note 4)	TYP	MAX (Note 4)	UNIT
INPUT CHARACTERISTICS						
V_{OS}	Input Offset Voltage	$V_{CM} = 2.5V$		3	15	mV
TCV_{OS}	Average Offset Voltage Drift (Note 1)			7		µV/°C
I_B	Input Bias Current	$V_{CM} = 2.5V$		2	60	nA
R_{IN}	Input Impedance			1		GW
C_{IN}	Input Capacitance			2		pF
CMIR	Common-Mode Input Range		-0.5		+5.5	V
CMRR	Common-Mode Rejection Ratio	for V_{IN} from -0.5V to 5.5V	45	66		dB
A_{VOL}	Open-Loop Gain	$0.5V \le V_{OUT} \le 4.5V$	65	80		dB
OUTPUT CHARACTERISTICS						
V_{OL}	Output Swing Low	$I_L = -5mA$		100	200	mV
V_{OH}	Output Swing High	$I_L = 5mA$	4.8	4.9		V
I_{SC}	Short Circuit Current			±120		mA
I_{OUT}	Output Current			±30		mA
POWER SUPPLY PERFORMANCE						
PSRR	Power Supply Rejection Ratio	V_S is moved from 4.5V to 15.5V	60	80		dB
I_S	Supply Current (Per Amplifier)	No Load		2.5	3.75	mA
DYNAMIC PERFORMANCE						
SR	Slew Rate (Note 2)	$1V \le V_{OUT} \le 4V$, 20% to 80%		33		V/µs
t_S	Settling to +0.1% ($A_V = +1$)	($A_V = +1$), $V_O = 2V$ Step		140		ns
BW	-3dB Bandwidth			30		MHz
GBWP	Gain-Bandwidth Product			20		MHz
PM	Phase Margin			50		°
CS	Channel Separation	f = 5MHz		110		dB
d_G	Differential Gain (Note 3)	$R_F = R_G = 1k\Omega$ and $V_{OUT} = 1.4V$		0.30		%
d_P	Differential Phase (Note 3)	$R_F = R_G = 1k\Omega$ and $V_{OUT} = 1.4V$		0.66		°

Electrical Specifications $V_S+ = 15V$, $V_S- = 0V$, $R_L = 1k\Omega$ and $C_L = 12pF$ to 7.5V, $T_A = +25°C$ unless otherwise specified.

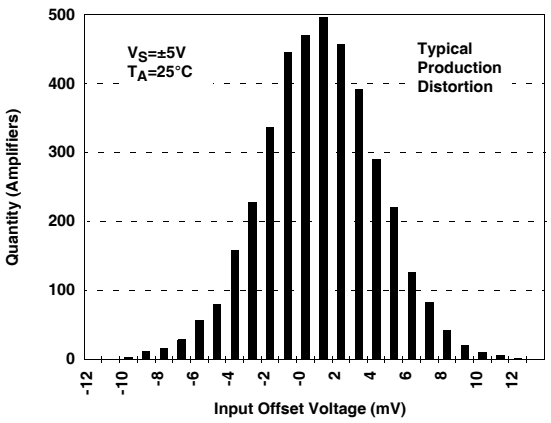
PARAMETER	DESCRIPTION	CONDITION	MIN (Note 4)	TYP	MAX (Note 4)	UNIT
INPUT CHARACTERISTICS						
V_{OS}	Input Offset Voltage	$V_{CM} = 7.5V$		3	15	mV
TCV_{OS}	Average Offset Voltage Drift (Note 1)			7		µV/°C
I_B	Input Bias Current	$V_{CM} = 7.5V$		2	60	nA
R_{IN}	Input Impedance			1		GW
C_{IN}	Input Capacitance			2		pF
CMIR	Common-Mode Input Range		-0.5		+15.5	V
CMRR	Common-Mode Rejection Ratio	for V_{IN} from -0.5V to 15.5V	53	72		dB
A_{VOL}	Open-Loop Gain	$0.5V \le V_{OUT} \le 14.5V$	65	80		dB
OUTPUT CHARACTERISTICS						
V_{OL}	Output Swing Low	$I_L = -7.5mA$		170	350	mV
V_{OH}	Output Swing High	$I_L = 7.5mA$	14.65	14.83		V
I_{SC}	Short Circuit Current			±120		mA
I_{OUT}	Output Current			±30		mA
POWER SUPPLY PERFORMANCE						
PSRR	Power Supply Rejection Ratio	V_S is moved from 4.5V to 15.5V	60	80		dB
I_S	Supply Current (Per Amplifier)	No Load		2.5	3.75	mA
DYNAMIC PERFORMANCE						
SR	Slew Rate (Note 2)	$1V \le V_{OUT} \le 14V$, 20% to 80%		33		V/µs
t_S	Settling to +0.1% ($A_V = +1$)	($A_V = +1$), $V_O = 2V$ Step		140		ns
BW	-3dB Bandwidth			30		MHz
GBWP	Gain-Bandwidth Product			20		MHz
PM	Phase Margin			50		°
CS	Channel Separation	f = 5MHz		110		dB
d_G	Differential Gain (Note 3)	$R_F = R_G = 1k\Omega$ and $V_{OUT} = 1.4V$		0.10		%
d_P	Differential Phase (Note 3)	$R_F = R_G = 1k\Omega$ and $V_{OUT} = 1.4V$		0.11		°

NOTES:

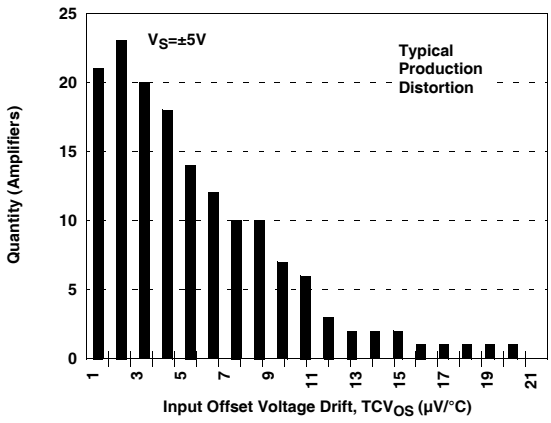
1. Measured over operating temperature range
2. Slew rate is measured on rising and falling edges
3. NTSC signal generator used
4. Parts are 100% tested at +25°C. Over temperature limits established by characterization and are not production tested.

Typical Performance Curves

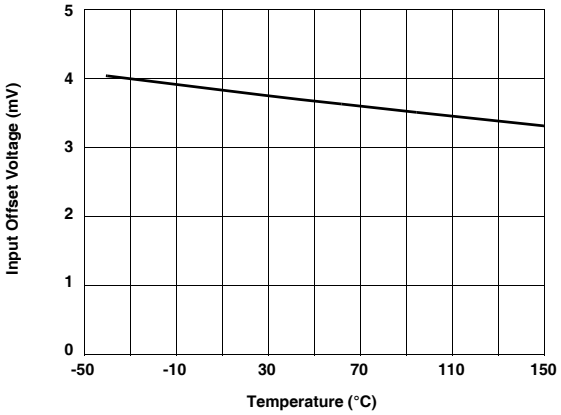
EL5410 Input Offset Voltage Distribution



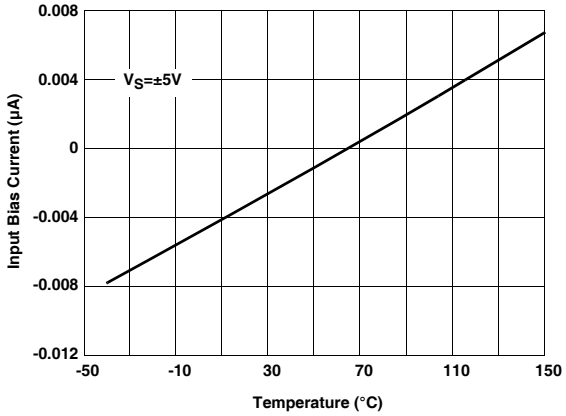
EL5410 Input Offset Voltage Drift



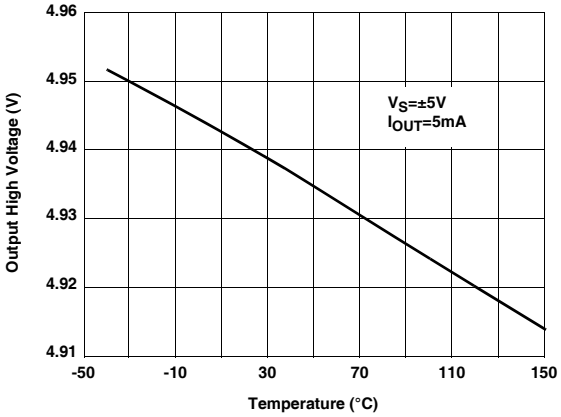
Input Offset Voltage vs Temperature



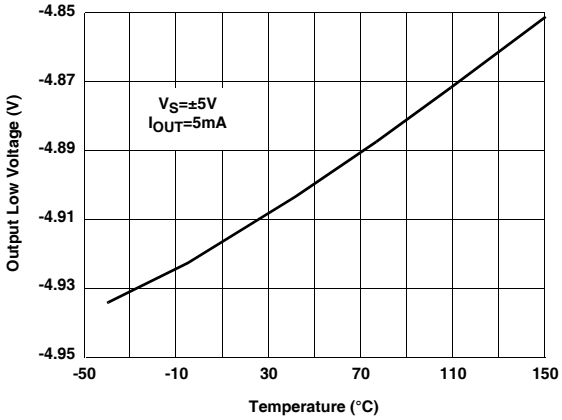
Input Bias Current vs Temperature



Output High Voltage vs Temperature

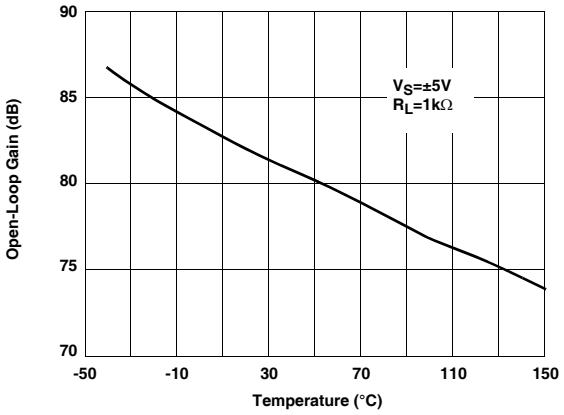


Output Low Voltage vs Temperature

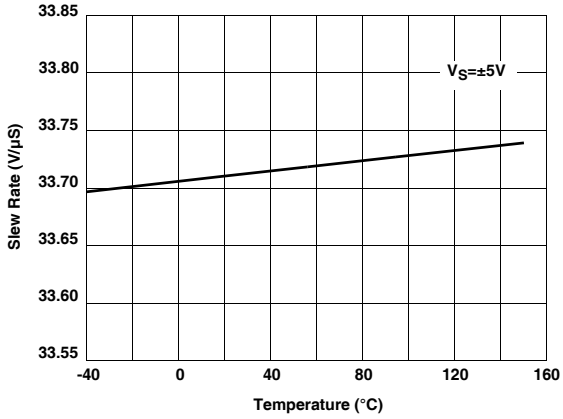


Typical Performance Curves (Continued)

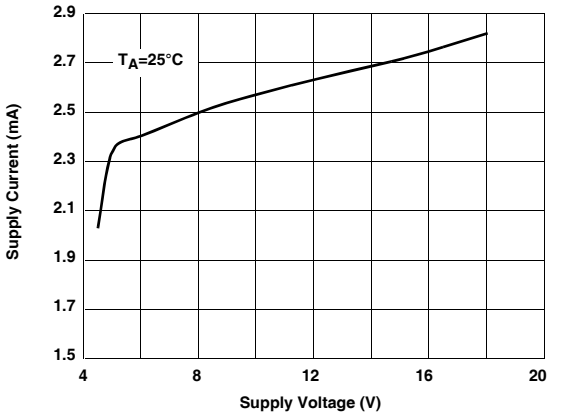
Open-Loop Gain vs Temperature



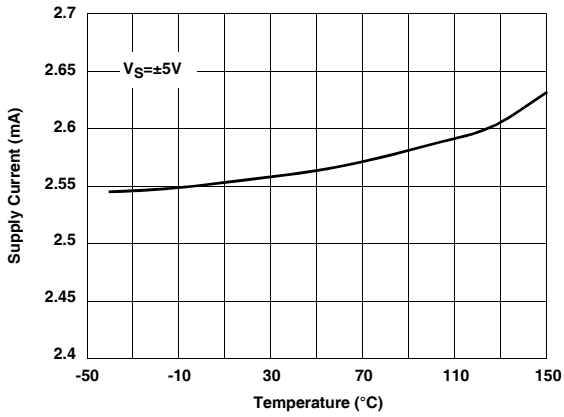
Slew Rate vs Temperature



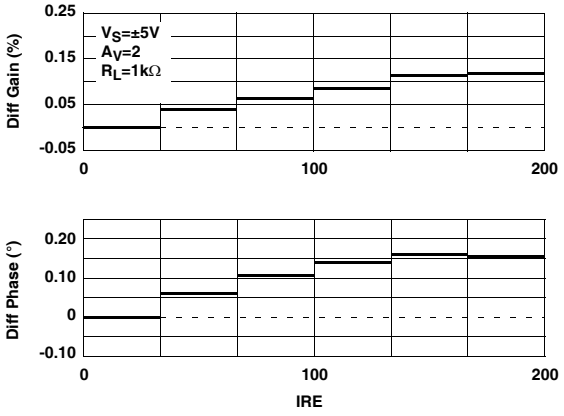
EL5410 Supply Current per Amplifier vs Supply Voltage



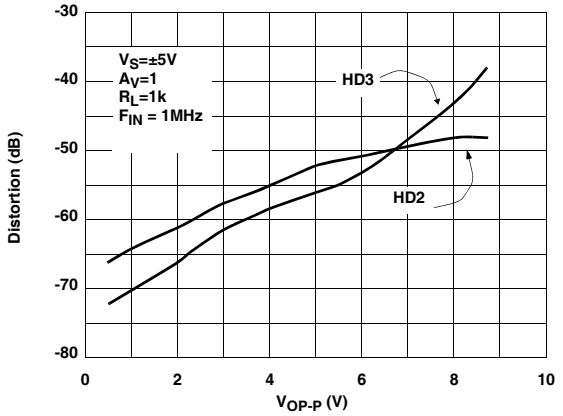
EL5410 Supply Current per Amplifier vs Temperature



Differential Gain and Phase

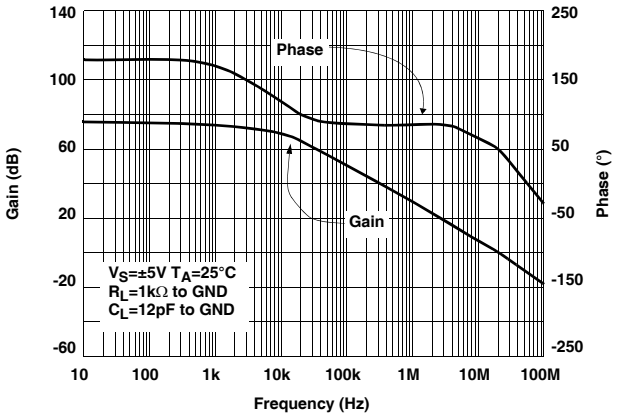


Harmonic Distortion vs V_{OP-P}

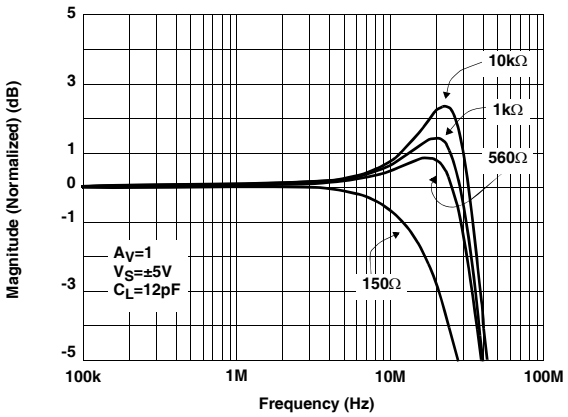


Typical Performance Curves (Continued)

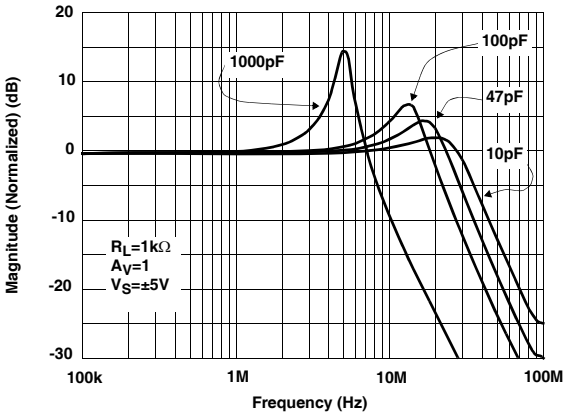
Open Loop Gain and Phase vs Frequency



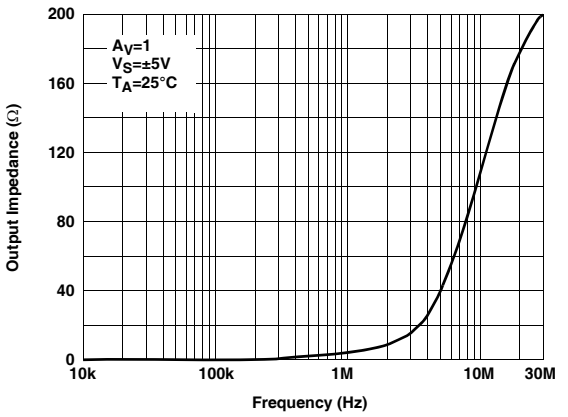
Frequency Response for Various R_L



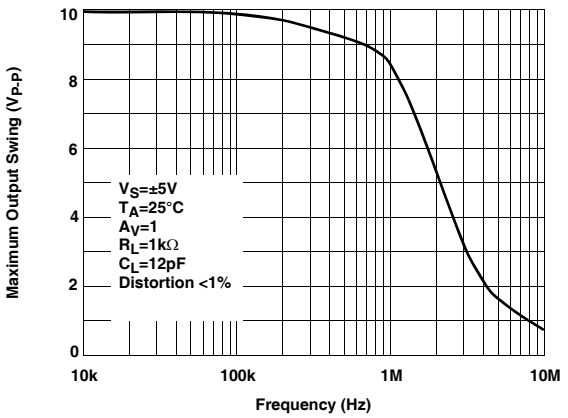
Frequency Response for Various C_L



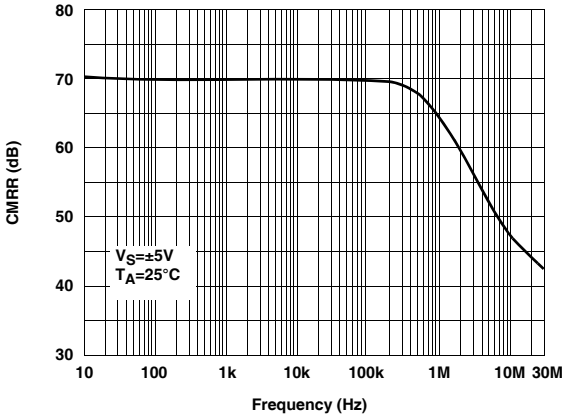
Closed Loop Output Impedance vs Frequency



Maximum Output Swing vs Frequency

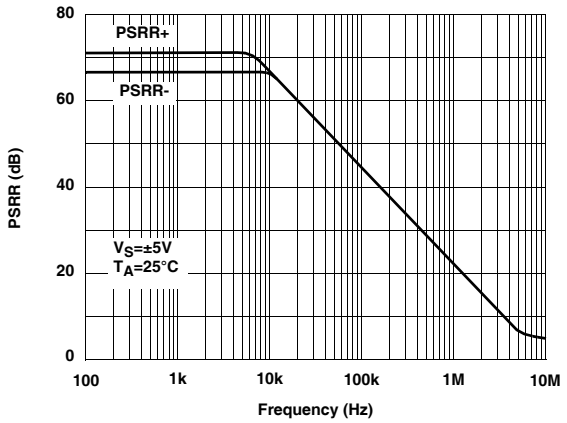


CMRR vs Frequency

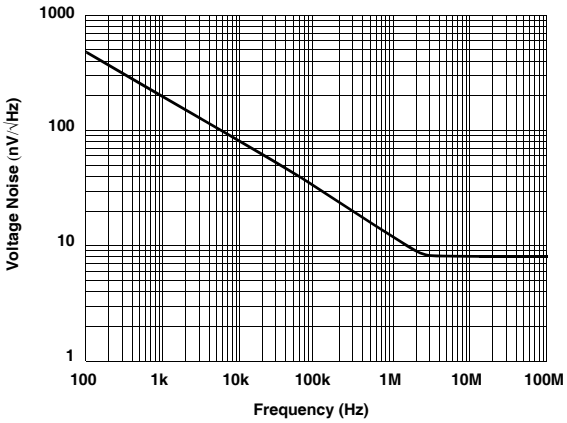


Typical Performance Curves (Continued)

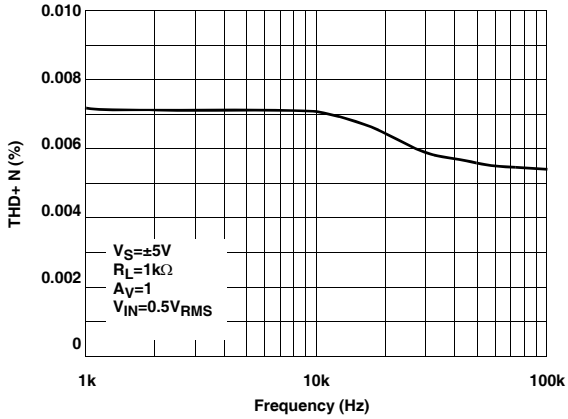
PSRR vs Frequency



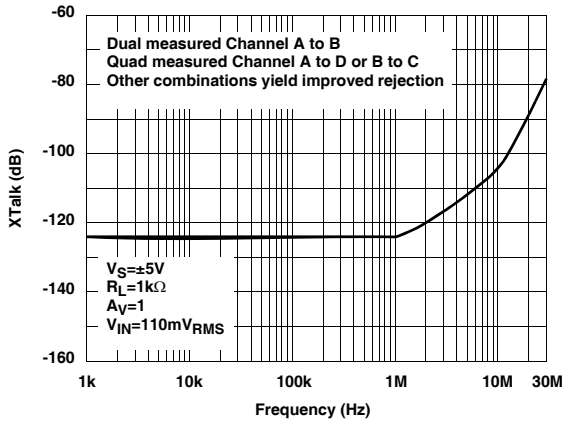
Input Voltage Noise Spectral Density vs Frequency



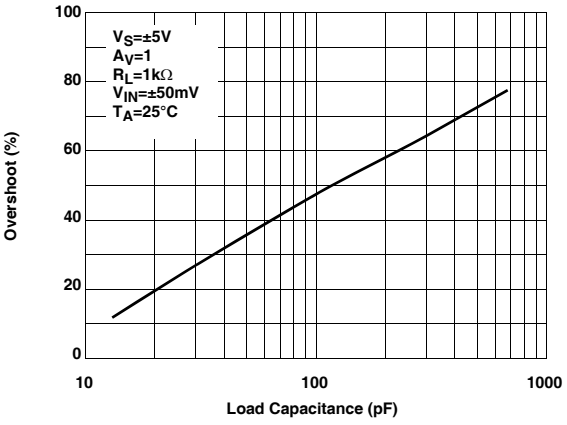
Total Harmonic Distortion + Noise vs Frequency



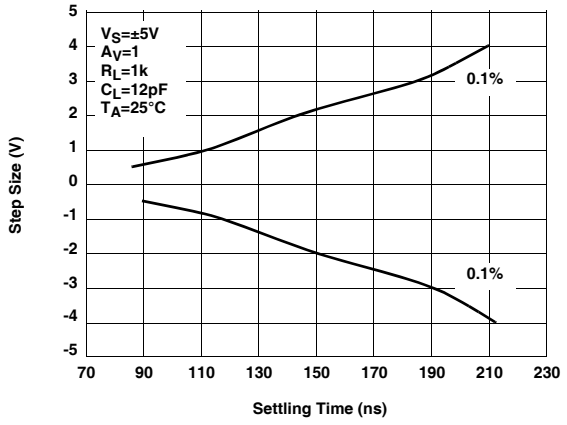
Channel Separation vs Frequency Response



Small-Signal Overshoot vs Load Capacitance

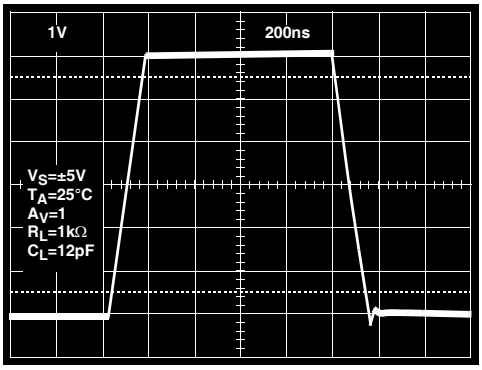


Settling Time vs Step Size

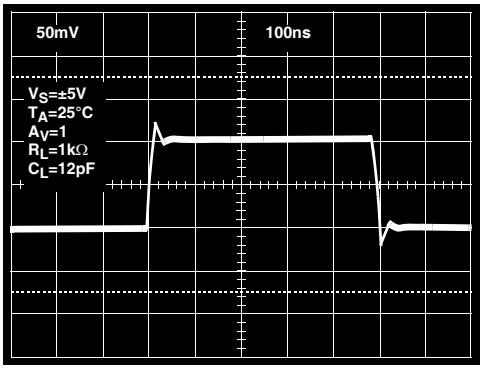


Typical Performance Curves (Continued)

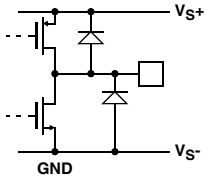
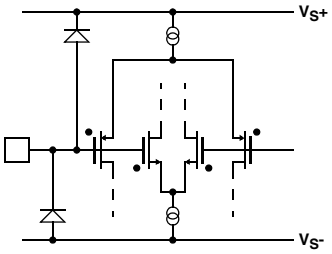
Large Signal Transient Response



Small Signal Transient Response



Pin Descriptions

EL5210	EL5410	Name	Function	Equivalent Circuit
1	1	V_{OUTA}	Amplifier A Output	 Circuit 1
2	2	V_{INA}-	Amplifier A Inverting Input	 Circuit 2
3	3	V_{INA}+	Amplifier A Non-Inverting Input	(Reference Circuit 2)
8	4	V_S+	Positive Power Supply	
5	5	V_{INB}+	Amplifier B Non-Inverting Input	(Reference Circuit 2)
6	6	V_{INB}-	Amplifier B Inverting Input	(Reference Circuit 2)
7	7	V_{OUTB}	Amplifier B Output	(Reference Circuit 1)
	8	V_{OUTC}	Amplifier C Output	(Reference Circuit 1)
	9	V_{INC}-	Amplifier C Inverting Input	(Reference Circuit 2)
	10	V_{INC}+	Amplifier C Non-Inverting Input	(Reference Circuit 2)
4	11	V_S-	Negative Power Supply	
	12	V_{IND}+	Amplifier D Non-Inverting Input	(Reference Circuit 2)
	13	V_{IND}-	Amplifier D Inverting Input	(Reference Circuit 2)
	14	V_{OUTD}	Amplifier D Output	(Reference Circuit 1)

Applications Information

Product Description

The EL5210 and EL5410 voltage feedback amplifiers are fabricated using a high voltage CMOS process. They exhibit Rail-to-Rail input and output capability, are unity gain stable and have low power consumption (2.5mA per amplifier). These features make the EL5210 and EL5410 ideal for a wide range of general-purpose applications. Connected in voltage follower mode and driving a load of 1kΩ and 12pF, the EL5210 and EL5410 have a -3dB bandwidth of 30MHz while maintaining a 33V/µS slew rate. The EL5210 is a dual amplifier while the EL5410 is a quad amplifier.

Operating Voltage, Input, and Output

The EL5210 and EL5410 are specified with a single nominal supply voltage from 5V to 15V or a split supply with its total range from 5V to 15V. Correct operation is guaranteed for a supply range of 4.5V to 16.5V. Most EL5210 and EL5410 specifications are stable over both the full supply range and operating temperatures of -40°C to +85°C. Parameter variations with operating voltage and/or temperature are shown in the typical performance curves.

The input common-mode voltage range of the EL5210 and EL5410 extends 500mV beyond the supply rails. The output swings of the EL5210 and EL5410 typically extend to within 100mV of positive and negative supply rails with load currents of 5mA. Decreasing load currents will extend the output voltage range even closer to the supply rails. Figure 1 shows the input and output waveforms for the device in the unity-gain configuration. Operation is from ±5V supply with a 1kΩ load connected to GND. The input is a $10V_{P-P}$ sinusoid. The output voltage is approximately $9.8V_{P-P}$.

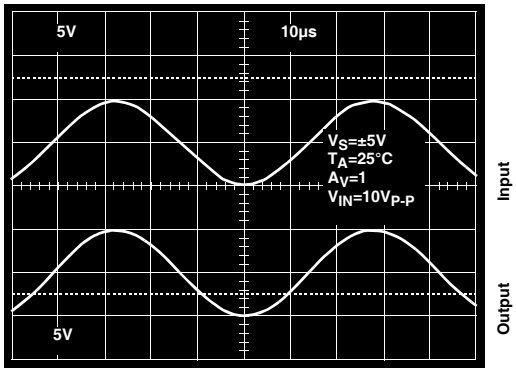


FIGURE 1. OPERATION WITH RAIL-TO-RAIL INPUT AND OUTPUT

Short Circuit Current Limit

The EL5210 and EL5410 will limit the short circuit current to ±120mA if the output is directly shorted to the positive or the negative supply. If an output is shorted indefinitely, the power dissipation could easily increase such that the device may be damaged. Maximum reliability is maintained if the output continuous current never exceeds ±30mA. This limit is set by the design of the internal metal interconnects.

Output Phase Reversal

The EL5210 and EL5410 are immune to phase reversal as long as the input voltage is limited from V_S- -0.5V to V_S+ +0.5V. Figure 2 shows a photo of the output of the device with the input voltage driven beyond the supply rails. Although the device's output will not change phase, the input's overvoltage should be avoided. If an input voltage exceeds supply voltage by more than 0.6V, electrostatic protection diodes placed in the input stage of the device begin to conduct and overvoltage damage could occur.

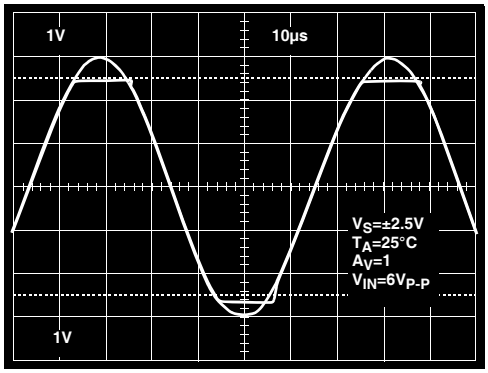


FIGURE 2. OPERATION WITH BEYOND-THE-RAILS INPUT

Power Dissipation

With the high-output drive capability of the EL5210 and EL5410 amplifiers, it is possible to exceed the 125°C 'absolute-maximum junction temperature' under certain load current conditions. Therefore, it is important to calculate the maximum junction temperature for the application to determine if load conditions need to be modified for the amplifier to remain in the safe operating area.

The maximum power dissipation allowed in a package is determined according to:

$$P_{DMAX} = \frac{T_{JMAX} - T_{AMAX}}{\Theta_{JA}}$$

Where:

T_{JMAX} = Maximum Junction Temperature

T_{AMAX}= Maximum Ambient Temperature

Θ_{JA} = Thermal Resistance of the Package

P_{DMAX} = Maximum Power Dissipation in the Package.

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the loads, or:

$$P_{DMAX} = \Sigma i[V_S \times I_{SMAX} + (V_S + - V_{OUT}i) \times I_{LOAD}i]$$

when sourcing, and

$$P_{DMAX} = \Sigma i[V_S \times I_{SMAX} + (V_{OUT}i - V_S\text{-}) \times I_{LOAD}i]$$

when sinking.

Where:

i = 1 to 2 for Dual and 1 to 4 for Quad

V_S = Total Supply Voltage

I_{SMAX} = Maximum Supply Current Per Amplifier

$V_{OUT}i$ = Maximum Output Voltage of the Application

$I_{LOAD}i$ = Load current

If we set the two P_{DMAX} equations equal to each other, we can solve for $R_{LOAD}i$ to avoid device overheat. Figure 3 and Figure 4 provide a convenient way to see if the device will overheat. The maximum safe power dissipation can be found graphically, based on the the package type and the ambient temperature. By using the previous equation, it is a simple matter to see if P_{DMAX} exceeds the device's power derating curves. To ensure proper operation, it is important to observe the recommended derating curves shown in Figure 3 and Figure 4.

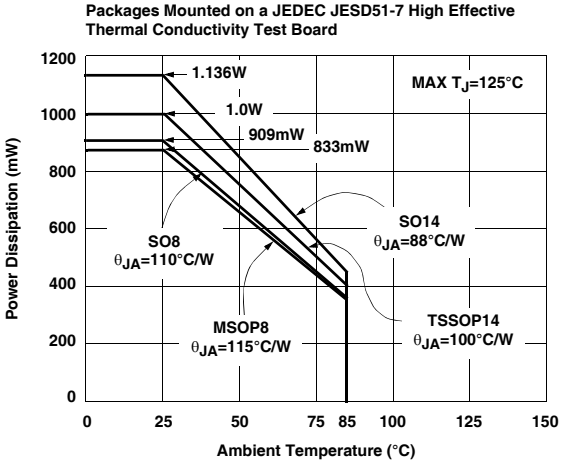


FIGURE 3. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

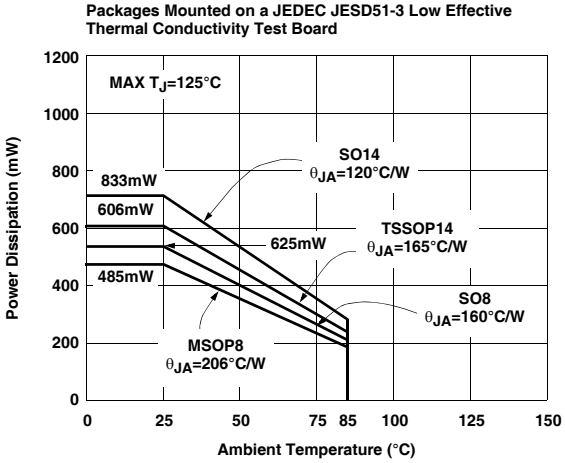


FIGURE 4. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Unused Amplifiers

It is recommended that any unused amplifiers in a dual and a quad package be configured as a unity gain follower. The inverting input should be directly connected to the output and the non-inverting input tied to the ground plane.

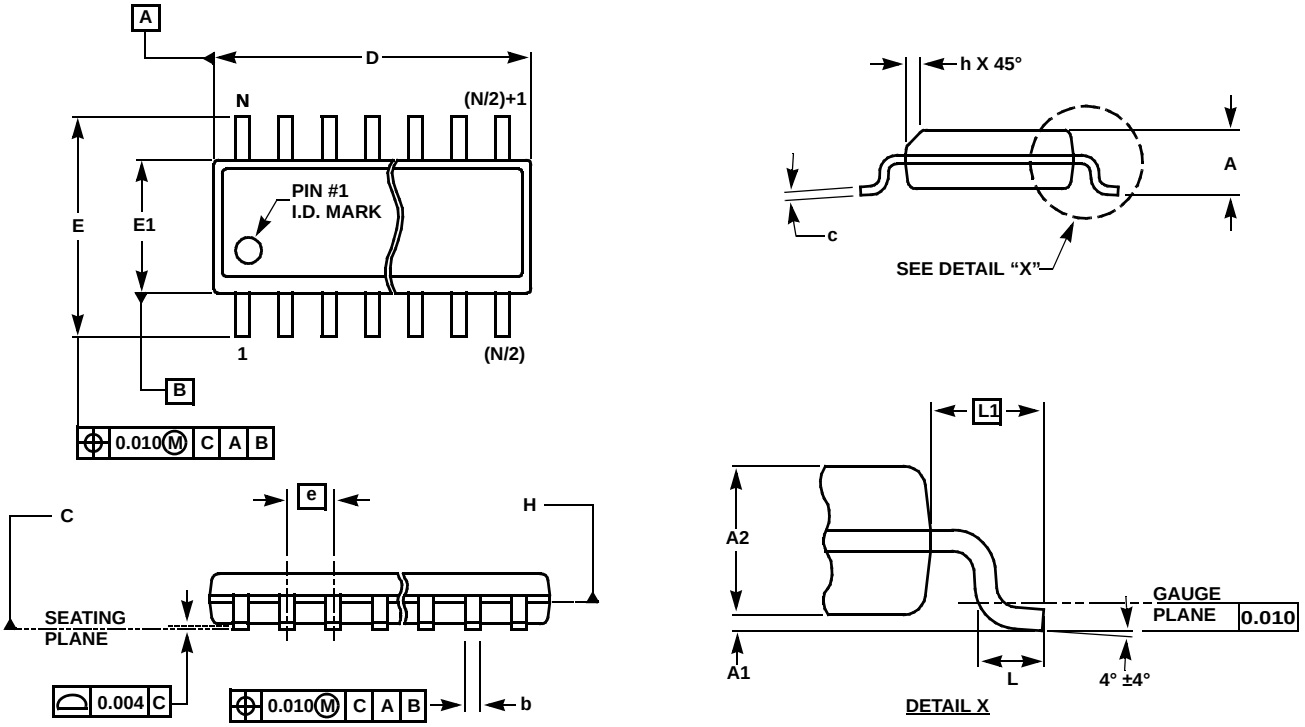
Driving Capacitive Loads

The EL5210 and EL5410 can drive a wide range of capacitive loads. As load capacitance increases, however, the -3dB bandwidth of the device will decrease and the peaking increase. The amplifiers drive 10pF loads in parallel with 1kΩ with just 1.2dB of peaking, and 100pF with 6.5dB of peaking. If less peaking is desired in these applications, a small series resistor (usually between 5Ω and 50Ω) can be placed in series with the output. However, this will obviously reduce the gain slightly. Another method of reducing peaking is to add a "snubber" circuit at the output. A snubber is a shunt load consisting of a resistor in series with a capacitor. Values of 150Ω and 10nF are typical. The advantage of a snubber is that it does not draw any DC load current or reduce the gain.

Power Supply Bypassing and Printed Circuit Board Layout

The EL5210 and EL5410 can provide gain at high frequency. As with any high-frequency device, good printed circuit board layout is necessary for optimum performance. Ground plane construction is highly recommended, lead lengths should be as short as possible and the power supply pins must be well bypassed to reduce the risk of oscillation. For normal single supply operation, where the V_S- pin is connected to ground, a 0.1µF ceramic capacitor should be placed from V_S+ to pin to V_S- pin. A 4.7µF tantalum capacitor should then be connected in parallel, placed in the region of the amplifier. One 4.7µF capacitor may be used for multiple devices. This same capacitor combination should be placed at each supply pin to ground if split supplies are to be used.

Small Outline Package Family (SO)



MDP0027

SMALL OUTLINE PACKAGE FAMILY (SO)

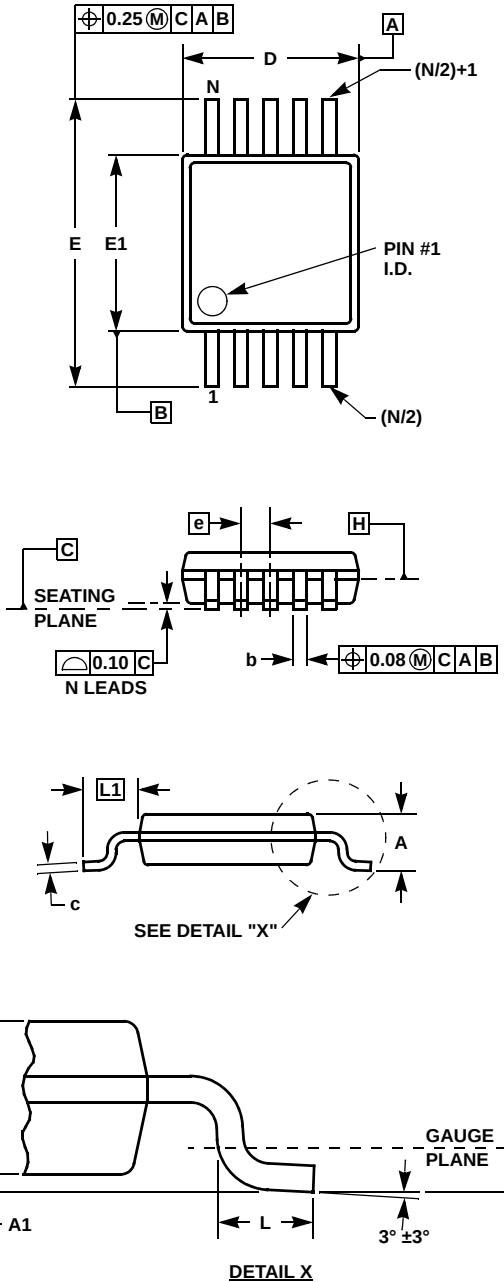
SYMBOL	INCHES							TOLERANCE	NOTES
	SO-8	SO-14	SO16 (0.150")	SO16 (0.300") (SOL-16)	SO20 (SOL-20)	SO24 (SOL-24)	SO28 (SOL-28)		
A	0.068	0.068	0.068	0.104	0.104	0.104	0.104	MAX	-
A1	0.006	0.006	0.006	0.007	0.007	0.007	0.007	±0.003	-
A2	0.057	0.057	0.057	0.092	0.092	0.092	0.092	±0.002	-
b	0.017	0.017	0.017	0.017	0.017	0.017	0.017	±0.003	-
c	0.009	0.009	0.009	0.011	0.011	0.011	0.011	±0.001	-
D	0.193	0.341	0.390	0.406	0.504	0.606	0.704	±0.004	1, 3
E	0.236	0.236	0.236	0.406	0.406	0.406	0.406	±0.008	-
E1	0.154	0.154	0.154	0.295	0.295	0.295	0.295	±0.004	2, 3
e	0.050	0.050	0.050	0.050	0.050	0.050	0.050	Basic	-
L	0.025	0.025	0.025	0.030	0.030	0.030	0.030	±0.009	-
L1	0.041	0.041	0.041	0.056	0.056	0.056	0.056	Basic	-
h	0.013	0.013	0.013	0.020	0.020	0.020	0.020	Reference	-
N	8	14	16	16	20	24	28	Reference	-

Rev. M 2/07

NOTES:

1. Plastic or metal protrusions of 0.006" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994

Mini SO Package Family (MSOP)



MDP0043

MINI SO PACKAGE FAMILY

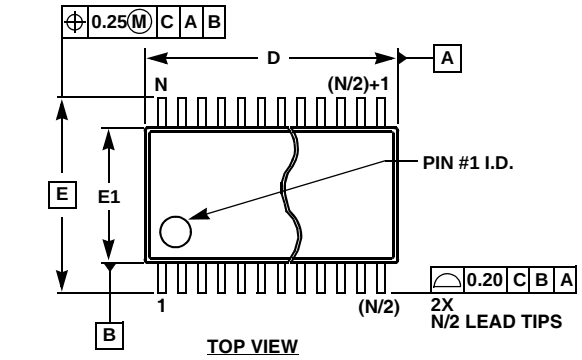
SYMBOL	MILLIMETERS		TOLERANCE	NOTES
	MSOP8	MSOP10		
A	1.10	1.10	Max.	-
A1	0.10	0.10	±0.05	-
A2	0.86	0.86	±0.09	-
b	0.33	0.23	+0.07/-0.08	-
c	0.18	0.18	±0.05	-
D	3.00	3.00	±0.10	1, 3
E	4.90	4.90	±0.15	-
E1	3.00	3.00	±0.10	2, 3
e	0.65	0.50	Basic	-
L	0.55	0.55	±0.15	-
L1	0.95	0.95	Basic	-
N	8	10	Reference	-

Rev. D 2/07

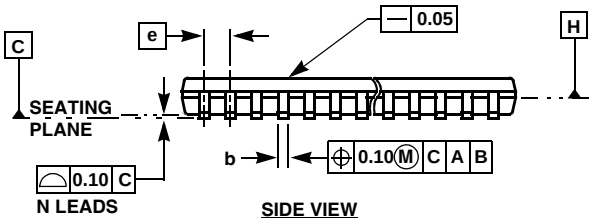
NOTES:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25mm maximum per side are not included.
3. Dimensions “D” and “E1” are measured at Datum Plane “H”.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.

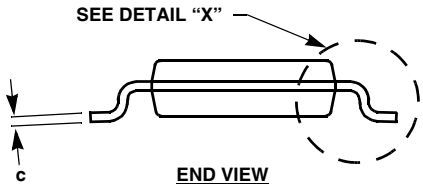
Thin Shrink Small Outline Package Family (TSSOP)



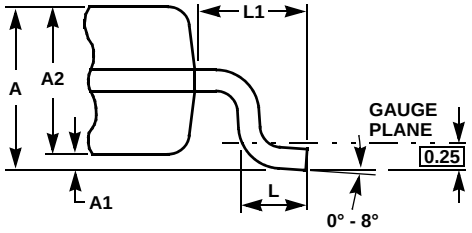
TOP VIEW



SIDE VIEW



END VIEW



DETAIL X

MDP0044

THIN SHRINK SMALL OUTLINE PACKAGE FAMILY

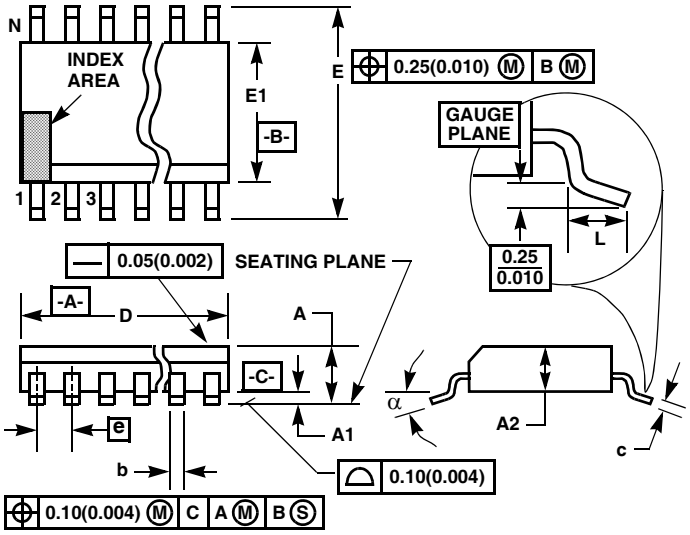
SYMBOL	MILLIMETERS					TOLERANCE
	14 LD	16 LD	20 LD	24 LD	28 LD	
A	1.20	1.20	1.20	1.20	1.20	Max
A1	0.10	0.10	0.10	0.10	0.10	±0.05
A2	0.90	0.90	0.90	0.90	0.90	±0.05
b	0.25	0.25	0.25	0.25	0.25	+0.05/-0.06
c	0.15	0.15	0.15	0.15	0.15	+0.05/-0.06
D	5.00	5.00	6.50	7.80	9.70	±0.10
E	6.40	6.40	6.40	6.40	6.40	Basic
E1	4.40	4.40	4.40	4.40	4.40	±0.10
e	0.65	0.65	0.65	0.65	0.65	Basic
L	0.60	0.60	0.60	0.60	0.60	±0.15
L1	1.00	1.00	1.00	1.00	1.00	Reference

Rev. F 2/07

NOTES:

1. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.
2. Dimension “E1” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm per side.
3. Dimensions “D” and “E1” are measured at dAtum Plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.

Thin Shrink Small Outline Plastic Packages (TSSOP)



NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-153-AC, Issue E.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E1” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of “b” dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact. (Angles in degrees)

M14.173

14 LEAD THIN SHRINK SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.047	-	1.20	-
A1	0.002	0.006	0.05	0.15	-
A2	0.031	0.041	0.80	1.05	-
b	0.0075	0.0118	0.19	0.30	9
c	0.0035	0.0079	0.09	0.20	-
D	0.195	0.199	4.95	5.05	3
E1	0.169	0.177	4.30	4.50	4
e	0.026 BSC		0.65 BSC		-
E	0.246	0.256	6.25	6.50	-
L	0.0177	0.0295	0.45	0.75	6
N	14		14		7
α	0^o	8^o	0^o	8^o	-

Rev. 2 4/06