MIC2205

2 MHz PWM Synchronous Buck Regulator with LDO Standby Mode

Feature

- 2.7 to 5.5V Supply Voltage
- Light Load LDO Mode
  - 18 µA Quiescent Current
  - Low Noise, 75 μV_{RMS}
- 2 MHz PWM Mode
  - Output Current to 600 mA
  - >95% Efficiency
  - 100% Maximum Duty Cycle
- Adjustable Output Voltage Option Down to 1V
  - Fixed Output Voltage Options Available
- Ultra-Fast Transient Response
- Stable with 1 µF Ceramic Output Capacitor
- Fully Integrated MOSFET Switches
- Micropower Shutdown
- Thermal Shutdown and Current Limit Protection
- Pb-Free 3 mm x 3 mm VDFN Package
- –40°C to +125°C Junction Temperature Range

Applications

- Cellular Phones
- PDAs
- USB Peripherals

General Description

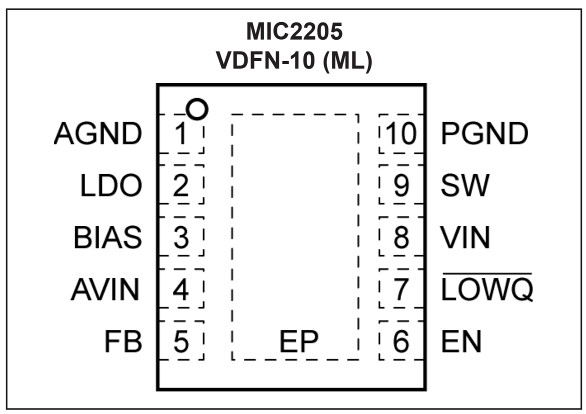
The MIC2205 is a high efficiency 2 MHz PWM synchronous buck (step-down) regulator that features an LDO standby mode that draws only 18 µA of quiescent current. The MIC2205 allows an ultra-low noise, small size, and high efficiency solution for portable power applications.

In PWM mode, the MIC2205 operates with a constant frequency 2 MHz PWM control. Under light load conditions, such as in system sleep or standby modes, the PWM switching operation can be disabled to reduce switching losses. In this light load mode, the LDO maintains the output voltage and draws only 18 µA of quiescent current. The LDO mode of operation saves battery life while not introducing spurious noise and high ripple as experienced with pulse skipping or bursting mode regulators.

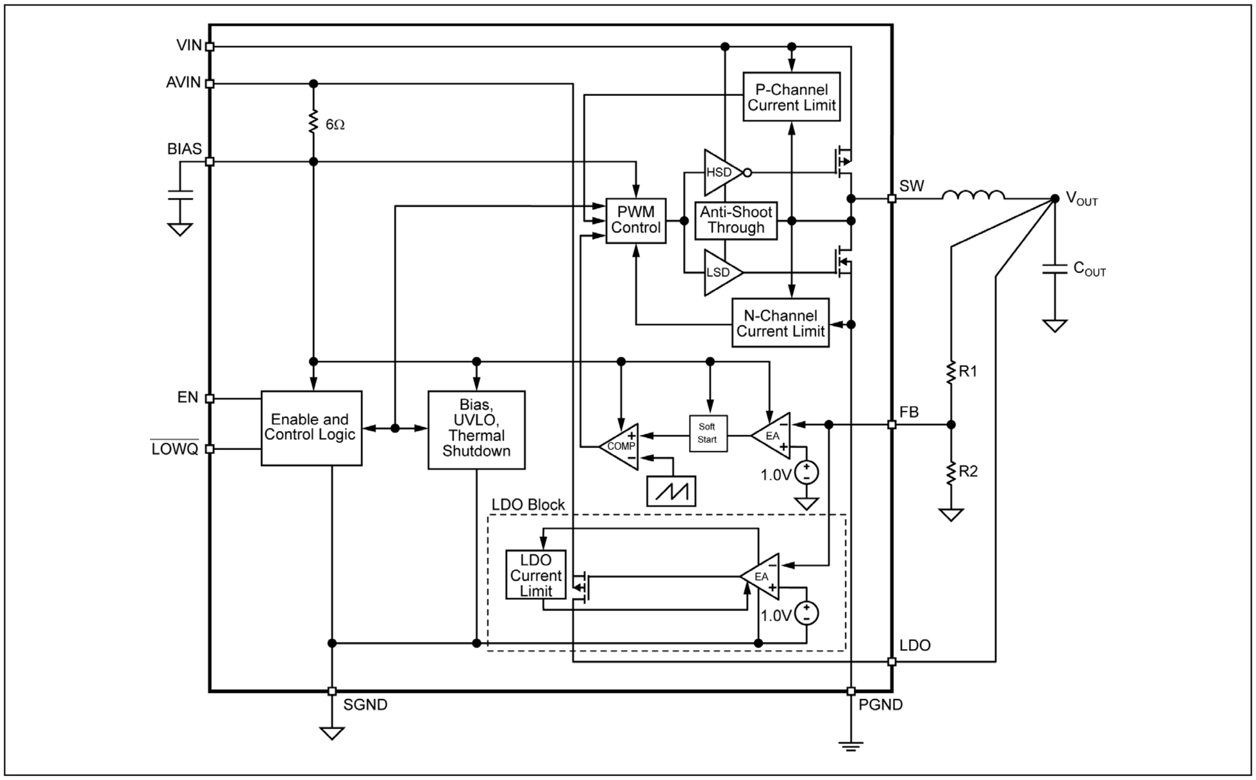
The MIC2205 operates from 2.7V to 5.5V input and features internal power MOSFETs that can supply up to 600 mA output current in PWM mode. It can operate with a maximum duty cycle of 100% for use in low dropout conditions.

The MIC2205 is available in a 3 mm x 3 mm VDFN-10L package with an operating junction temperature range from –40°C to +125°C.

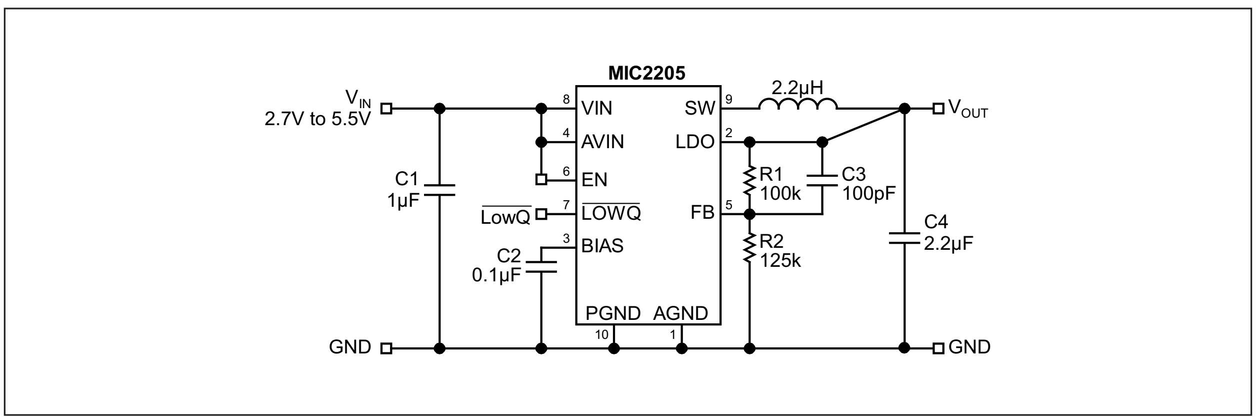
Package Type



Functional Block Diagram



Typical Application



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1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage (V_{IN}) .... +6V
Output Switch Voltage (V_{SW}) .... +6V
Output Switch Current (I_{SW}) 2A
Logic Input Voltage (V_{EN}, V_{LOWQ}) .... –0.3V to V_{IN}
Storage Temperature (T_S) .... –60°C to +150°C
ESD Rating (Note 1) .... 3 kV

Operating Ratings ‡

Supply Voltage (V_{IN}) .... +2.7V to +5.5V
Logic Input Voltage (V_{EN}, V_{LOWQ}) .... –0.3V to V_{IN}
Junction Temperature (T_J) .... –40°C to +125°C
Package Thermal Resistance
VDFN-10 (θ_{JA}) .... 60°C/W

† Notice: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability. Specifications are for packaged product only.

‡ Notice: The device is not guaranteed to function outside its operating ratings.

Note 1: Devices are ESD sensitive. Handling precautions recommended. Human body model: 1.5 kΩ in series with 100 pF.

ELECTRICAL CHARACTERISTICS (Note 2)

Electrical Characteristics: V_{IN}= V_{EN} = V_{LOWQ} = 3.6V; L = 2.2 µH; T_A = 25°C, **Bold** values indicate –40°C ≤ T_A ≤ +125°C; unless otherwise noted.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Supply Voltage Range	—	**2.7**	—	**5.5**	V	—
Undervoltage Lockout Threshold	—	2.45	2.55	2.65	V	Turn-On
UVLO Hysteresis	—	—	100	—	mV	—
Quiescent Current, PWM mode	—	—	690	**900**	µA	V_{FB} = 0.9 * V_{NOM} (not switching)
Quiescent Current, LDO mode	—	—	16	**29**	µA	V_{LOWQ} = 0V; I_{OUT} = 0 mA
Shutdown Current	—	—	0.01	**5**	µA	V_{EN} = 0V
[Adjustable] Feedback Voltage	—	0.99 **0.98**	1	1.01 **1.02**	V	±1% ±2% (over temperature)
[Fixed Output] Voltages	—	**–1** –2	—	+1 **+2**	%	Nominal V_{OUT} tolerance
FB pin input current	—	—	1	—	nA	—
Current Limit in PWM Mode	—	**0.75**	1	**1.85**	A	V_{FB} = 0.9 * V_{NOM}
Output Voltage Line Regulation	—	—	0.13	—	%	V_{OUT} > 2V; VIN = V_{OUT} + 300 mV to 5.5V; I_{LOAD} = 100 mA V_{OUT} < 2V; V_{IN} = 2.7V to 5.5V; I_{LOAD} = 100 mA
Output Voltage Load Regulation, PWM Mode	—	—	0.2	**0.5**	%	20 mA < I_{LOAD} < 300 mA
Output Voltage Load Regulation, LDO Mode	—	—	0.1	**0.2**	%	100 µA < I_{LOAD} < 50 mA V_{LOWQ} = 0V
Maximum Duty Cycle	—	**100**	—	—	%	V_{FB} ≤ 0.4V

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ELECTRICAL CHARACTERISTICS (Note 2)

Electrical Characteristics: V_{IN}= V_{EN} = V_{LOWQ} = 3.6V; L = 2.2 µH; T_A = 25°C, **Bold** values indicate –40°C ≤ T_A ≤ +125°C; unless otherwise noted.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
PWM Switch-On Resistance	—	—	0.4	—	Ω	I_{SW} = 50 mA V_{FB} = 0.7V_{FB_NOM} (High Side Switch)
	—	—	0.4	—		I_{SW} = -50 mA V_{FB} = 1.1V_{FB_NOM} (Low Side Switch)
Oscillator Frequency	—	**1.8**	2	**2.2**	MHz	—
$\overline{\text{LOWQ}}$ Threshold Voltage	—	**0.5**	0.85	**1.3**	V	—
$\overline{\text{LOWQ}}$ Input Current	—	—	0.1	**2**	µA	—
Enable Threshold	—	**0.5**	0.85	**1.3**	V	—
Enable Input Current	—	—	0.1	**2**	µA	—
LDO Dropout Voltage (Note 1)	—	—	110	—	mV	I_{OUT} = 50 mA
Output Voltage Noise	—	—	75	—	µVrms	$\overline{\text{LOWQ}}$ = 0V; C_{OUT} = 2.2 µF, 10 Hz to 100 kHz
LDO Current Limit	—	**60**	120	—	mA	$\overline{\text{LOWQ}}$ = 0V; V_{OUT} = 0V (LDO Mode)
Overtemperature Shutdown	—	—	160	—	°C	—
Overtemperature Hysteresis	—	—	20	—	°C	—

Note 1: Dropout voltage is defined as the input-to-output differential at which the output voltage drops 2% below its nominal value that is initially measured at a 1V differential. For outputs below 2.7V, the dropout voltage is the input-to-output voltage differential with a minimum input voltage of 2.7V

2: Specification for packaged product only.

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TEMPERATURE SPECIFICATIONS (Note 1)

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Storage Temperature	T_S	–60	—	+150	°C	—
Junction Temperature Range	T_J	–40	—	+125	°C	—
Package Thermal Resistances						
Thermal Resistance 10-Lead VDFN	θ_{JA}	—	—	60	°C/W	—

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperatures above +125°C can impact the device reliability.

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

PWM Mode

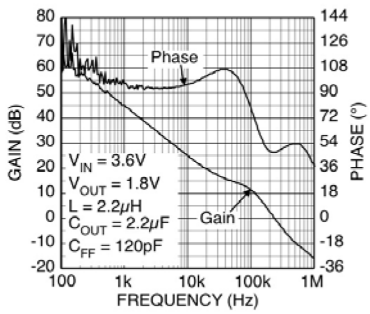

FIGURE 2-1: *Bode Plot.*

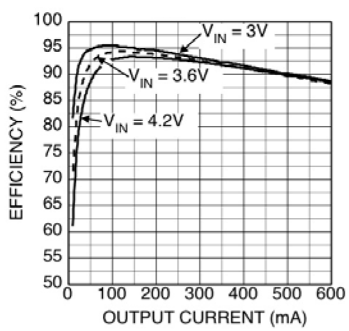

FIGURE 2-2: *2.5 V_{OUT} Efficiency.*

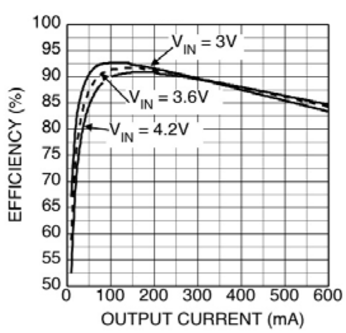

FIGURE 2-3: *1.8 V_{OUT} Efficiency.*

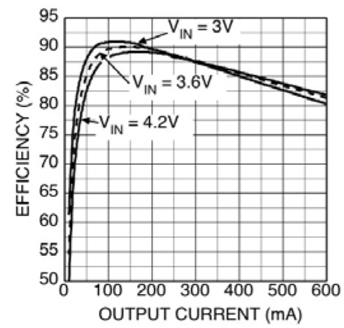

FIGURE 2-4: *1.5 V_{OUT} Efficiency.*

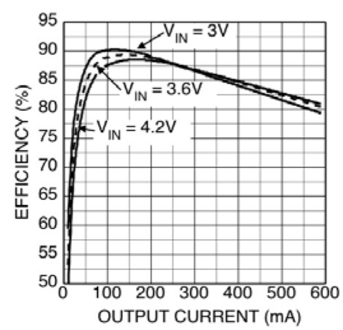

FIGURE 2-5: *1.38 V_{OUT} Efficiency.*

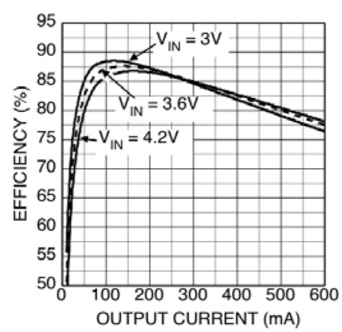

FIGURE 2-6: *1.2 V_{OUT} Efficiency.*

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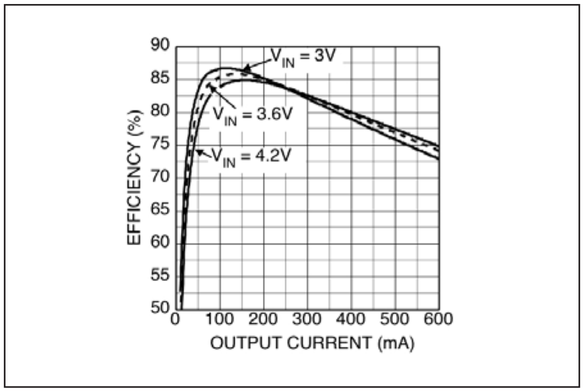

FIGURE 2-7: *1.0 V_{OUT} Efficiency.*

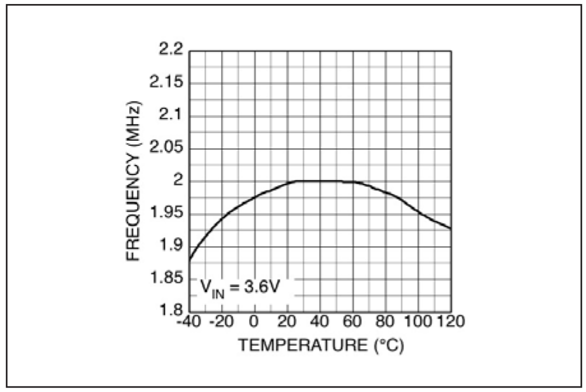

FIGURE 2-10: *Frequency vs. Temperature.*

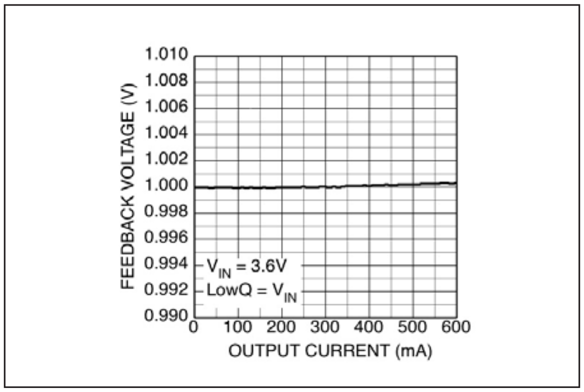

FIGURE 2-8: *Load Regulation.*

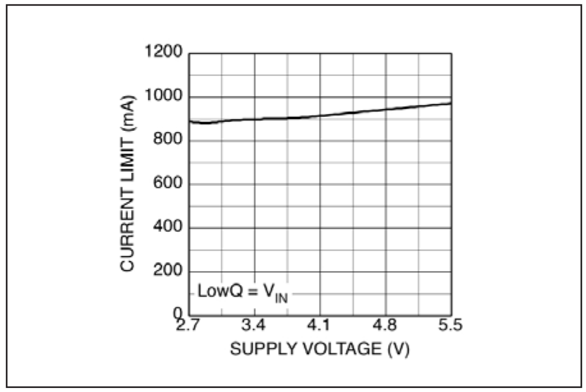

FIGURE 2-11: *Peak Current Limit vs. Voltage.*

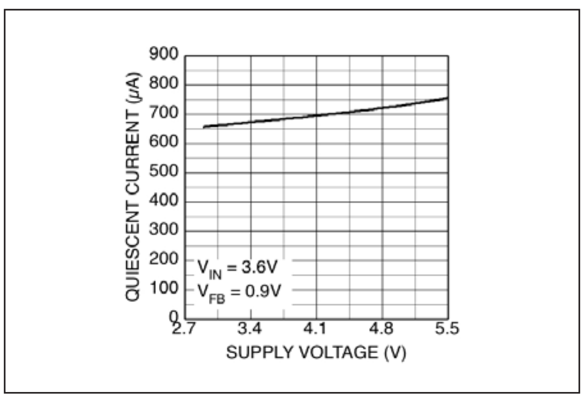

FIGURE 2-9: *Quiescent Current vs. Supply Voltage.*

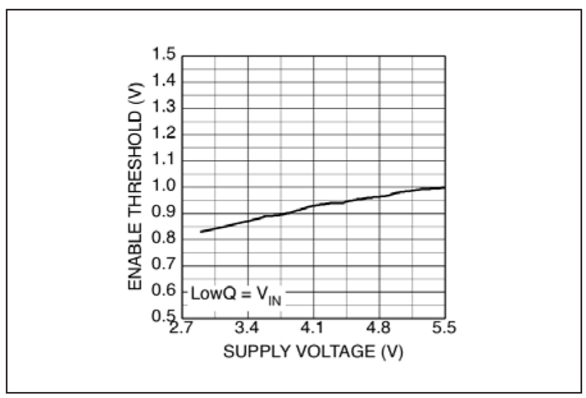

FIGURE 2-12: *Enable Threshold vs. Voltage.*

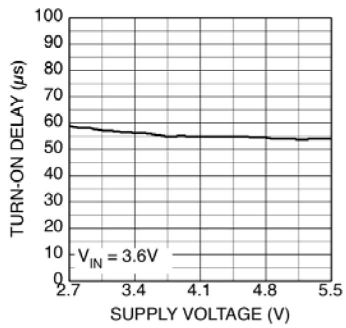

FIGURE 2-13: Turn-On Time vs. Supply Voltage.

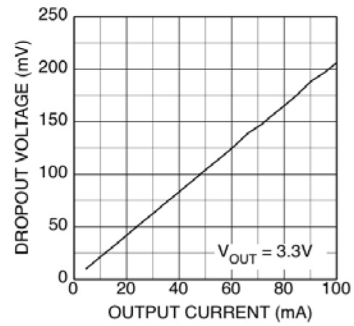

FIGURE 2-16: Dropout vs. Output Current.

LDO Mode

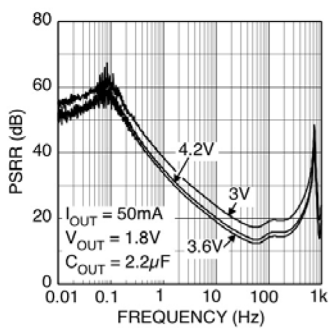

FIGURE 2-14: PSRR.

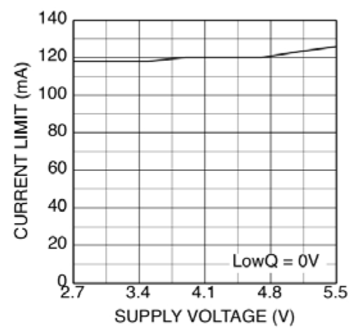

FIGURE 2-17: Current Limit vs. Supply Voltage.

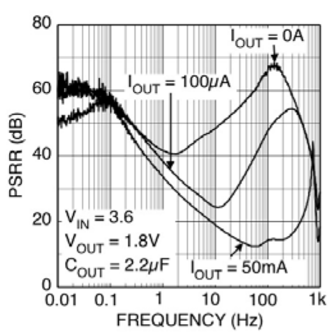

FIGURE 2-15: PSRR.

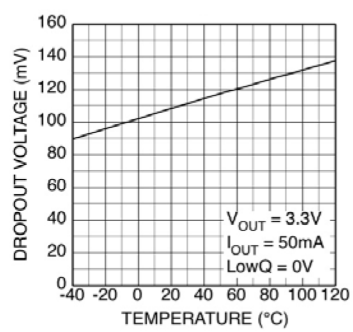

FIGURE 2-18: Dropout Voltage vs. Temperature.

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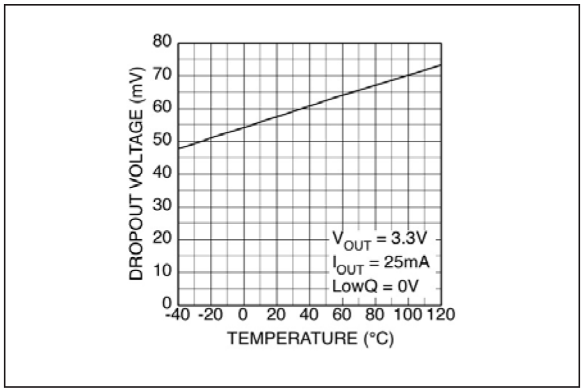

FIGURE 2-19: *Dropout Voltage vs. Temperature.*

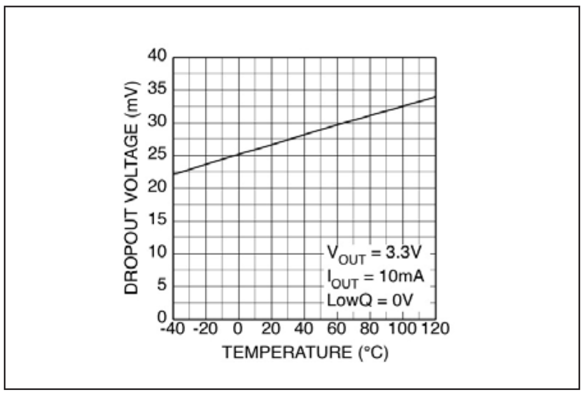

FIGURE 2-20: *Dropout Voltage vs. Temperature.*

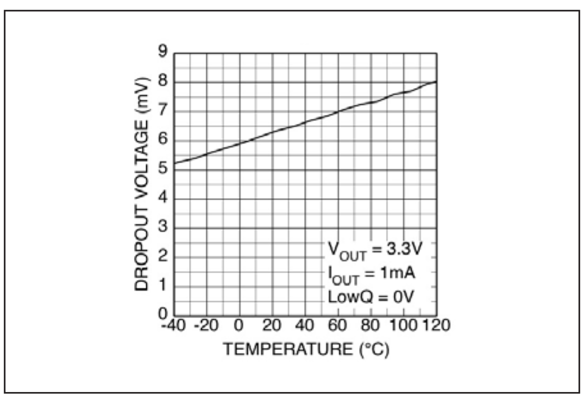

FIGURE 2-21: *Dropout Voltage vs. Temperature.*

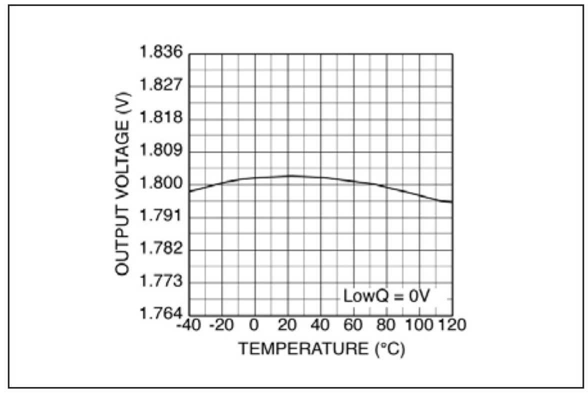

FIGURE 2-22: *Output Voltage vs. Temperature.*

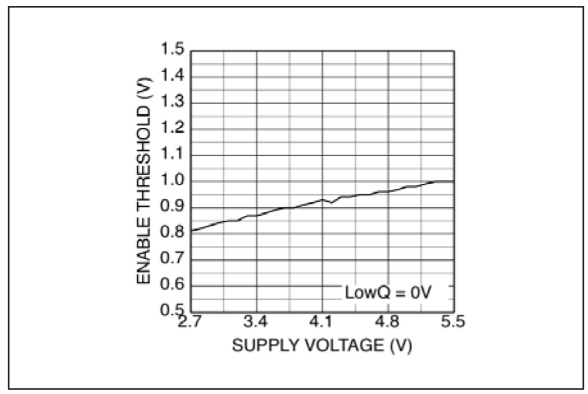

FIGURE 2-23: *Enable Threshold Voltage vs. Supply Voltage.*

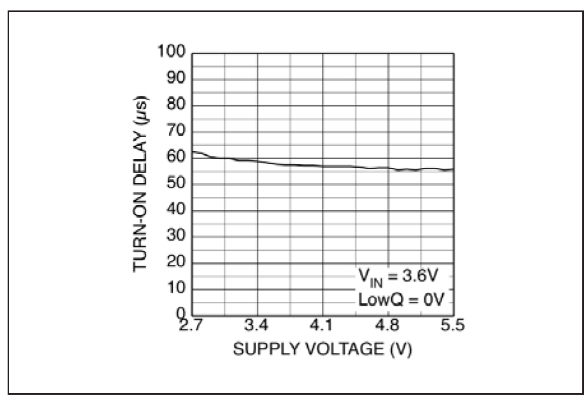

FIGURE 2-24: *Turn-On Time vs. Supply Voltage.*

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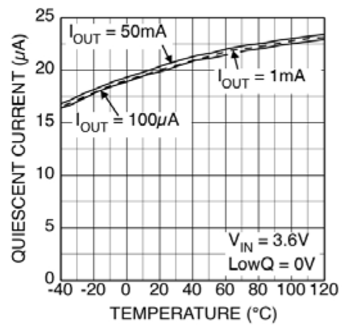

FIGURE 2-25: *Quiescent Current vs. Temperature.*

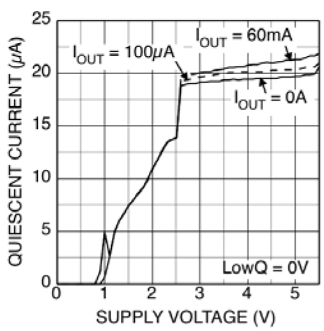

FIGURE 2-26: *Quiescent Current vs. Temperature.*

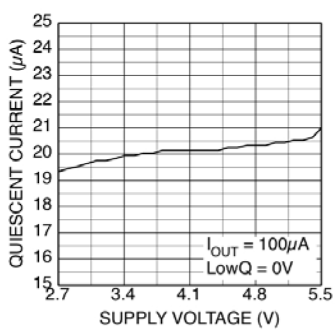

FIGURE 2-27: *Quiescent Current vs. Supply Voltage.*

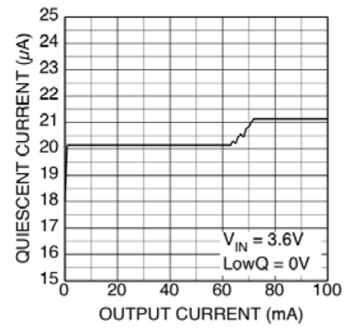

FIGURE 2-28: *Quiescent Current vs. Output Current.*

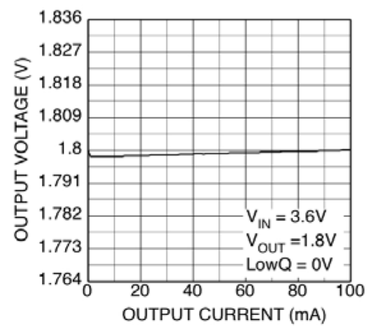

FIGURE 2-29: *Output Voltage vs. Output Current.*

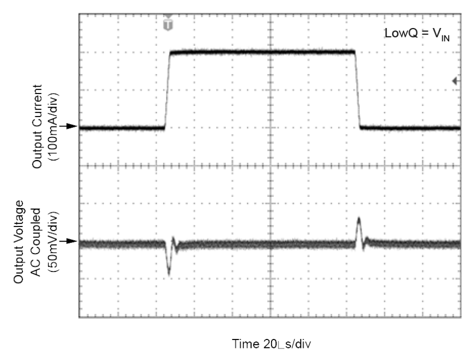

FIGURE 2-30: *Load Transient PWM Mode.*

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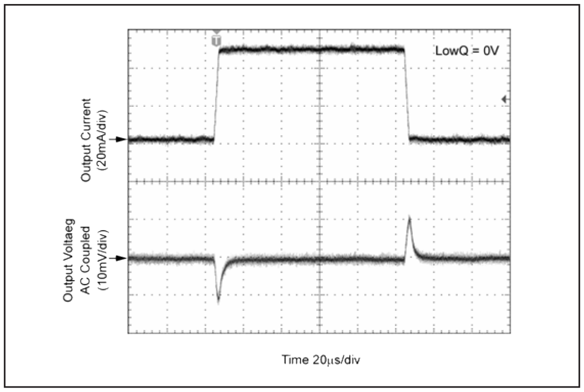

FIGURE 2-31: *Load Transient LDO Mode.*

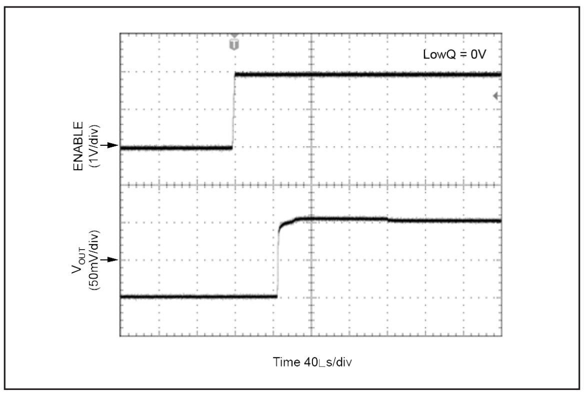

FIGURE 2-32: *Enable Transient PWM Mode.*

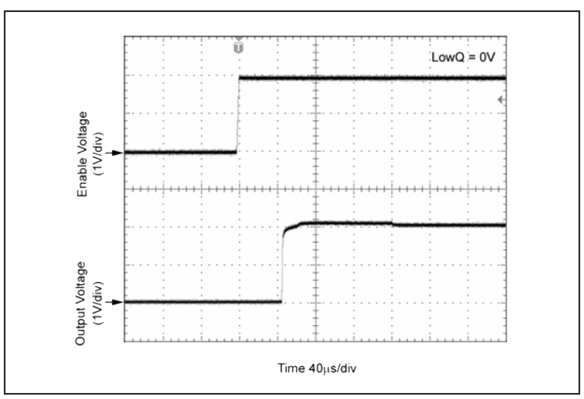

FIGURE 2-33: *Enable Transient LDO Mode.*

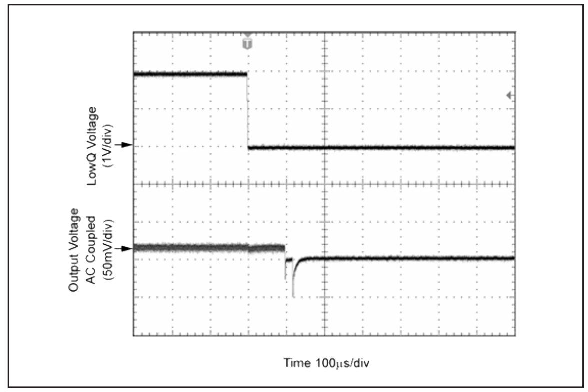

FIGURE 2-34: *PWM Mode to LDO Mode Transient.*

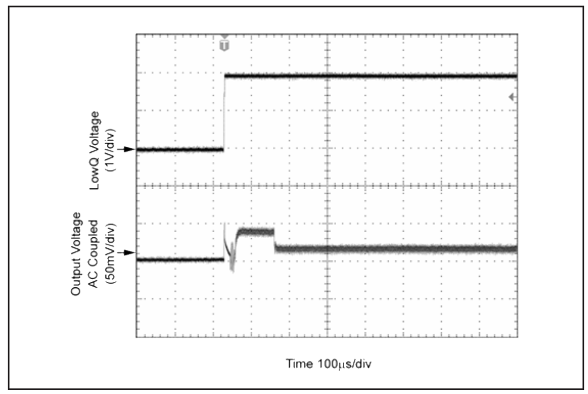

FIGURE 2-35: *LDO Mode to PWM Mode Transient.*

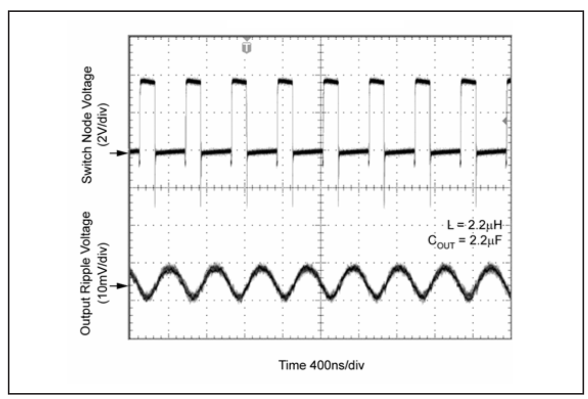

FIGURE 2-36: *PWM Waveform.*

3.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	AGND	Analog (Signal) Ground.
2	LDO	LDO (Output): Connect to V_{OUT} for LDO mode operation.
3	BIAS	Internal circuit bias supply. Must be de-coupled to signal ground with a 0.1 µF capacitor and should not be loaded.
4	AVIN	Analog Supply Voltage (Input): Supply voltage for the analog control circuitry and LDO input power. Requires bypass capacitor to GND.
5	FB	Feedback. Input to the error amplifier. For the adjustable option, connect to the external resistor divider network to set the output voltage. For fixed output voltage options, connect the feed forward capacitor between this pin and V_{OUT}; the internal resistor network sets the output voltage.
6	EN	Enable (Input). Logic low will shut down the device, reducing the quiescent current to less than 5 µA.
7	$\overline{LOWQ}$	Enable LDO Mode (Input): Logic low enables the internal LDO and disables the PWM operation. Logic high enables the PWM mode and disables the LDO mode.
8	VIN	Supply Voltage (Input): Supply voltage for the internal switches and drivers.
9	SW	Switch (Output): Internal power MOSFET output switches.
10	PGND	Power Ground.
EP	GND	Ground, backside pad.

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4.0 FUNCTIONAL DESCRIPTION

4.1 VIN

VIN provides power to the MOSFETs for the switch mode regulator section, along with the current limiting sensing. Due to the high switching speeds, a 1 µF capacitor is recommended close to VIN and the power ground (PGND) pin for bypassing.

4.2 AVIN

Analog V_{IN} (AVIN) provides power to the LDO section and the bias through an internal 6Ω resistor. AVIN and VIN must be tied together. Careful layout should be considered to ensure high frequency switching noise caused by VIN is reduced before reaching AVIN.

4.3 LDO

The LDO pin is the output of the linear regulator and should be connected to the output. In LOWQ mode ($\overline{LOWQ}$ < 1.5V), the LDO provides the output voltage. In PWM mode ($\overline{LOWQ}$ > 1.5V) the LDO pin is high impedance.

4.4 EN

The enable pin provides a logic level control of the output. In the off state, supply current of the device is greatly reduced (typically <1 µA). Also, in the off state, the output drive is placed in a tri-stated condition, where both the high side P-channel MOSFET and the low-side N-channel are in an off or non-conducting state. Do not drive the enable pin above the supply voltage.

4.5 $\overline{LOWQ}$

The $\overline{LOWQ}$ pin provides a logic level control between the internal PWM mode and the low noise linear regulator mode. With $\overline{LOWQ}$ pulled low (<0.5V), quiescent current of the device is greatly reduced by switching to a low noise linear regulator mode that has a typical I_Q of 18 µA. In linear (LDO) mode the output can deliver 60 mA of current to the output. By placing $\overline{LOWQ}$ high (>1.5V), this transitions the device into a constant frequency PWM buck regulator mode. This allows the device the ability to efficiently deliver up to 600 mA of output current at the same output voltage.

4.6 BIAS

The BIAS pin supplies the power to the internal power to the control and reference circuitry. The bias is powered from AVIN through an internal 6Ω resistor. A small 0.1 µF capacitor is recommended for bypassing.

4.7 FB

The feedback pin (FB) provides the control path to control the output. For adjustable versions, a resistor divider connecting the feedback to the output is used to adjust the desired output voltage. The output voltage is calculated as shown in Equation 4-1.

EQUATION 4-1:

$$V_{OUT} = V_{REF} \times \left(\frac{R1}{R2} + 1\right)$$

Where:

V_{REF} = 1.0V

A feed-forward capacitor is recommended for most designs using the adjustable output voltage option. To reduce battery current draw, a 100 kΩ feedback resistor is recommended from the output to the FB pin (R1). Also, a feed-forward capacitor should be connected between the output and feedback (across R1). The large resistor value and the parasitic capacitance of the FB pin can cause a high frequency pole that can reduce the overall system phase margin. By placing a feed-forward capacitor, these effects can be significantly reduced. Feed-forward capacitance (C_{FF}) can be calculated as shown in Equation 4-2.

EQUATION 4-2:

$$C_{FF} = \frac{1}{2\pi \times R1 \times 160kHz}$$

For fixed options a feed-forward capacitor from the output to the FB pin is required. Typically a 100 pF small ceramic capacitor is recommended.

4.8 SW

The switch (SW) pin connects directly to the inductor and provides the switching current necessary to operate in PWM mode. Due to the high speed switching on this pin, the switch node should be routed away from sensitive nodes and it should be as small as possible.

4.9 PGND

Power ground (PGND) is the ground path for the high current PWM mode. The current loop for the power ground should be as small as possible and separate from the Analog ground (AGND) loop.

4.10 SGND

Signal ground (SGND) is the ground path for the biasing and control circuitry. The current loop for the signal ground should be separate from the Power ground (PGND) loop.

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5.0 APPLICATIONS INFORMATION

The MIC2205 is a 600 mA PWM power supply that utilizes a LOWQ light load mode to maximize battery efficiency in light load conditions. This is achieved with a $\overline{\text{LOWQ}}$ control pin that when pulled low, shuts down all the biasing and drive current for the PWM regulator, drawing only 18 µA of operating current. This allows the output to be regulated through the LDO output, capable of providing 60 mA of output current. This method has the advantage of producing a clean, low current, ultra low noise output in LOWQ mode. During LOWQ mode, the SW node becomes high impedance, blocking current flow. Other methods of reducing quiescent current, such as pulse frequency modulation (PFM) or bursting techniques, create large amplitude, low frequency ripple voltages that can be detrimental to system operation.

When more than 60 mA is required, the $\overline{\text{LOWQ}}$ pin can be forced high, causing the MIC2205 to enter PWM mode. In this case, the LDO output makes a hand-off to the PWM regulator with virtually no variation in output voltage. The LDO output then turns off allowing up to 600 mA of current to be efficiently supplied through the PWM output to the load.

5.1 Input Capacitor

A minimum 1 µF ceramic is recommended on the VIN pin for bypassing. X5R or X7R dielectrics are recommended for the input capacitor. Y5V dielectrics lose most of their capacitance over temperature and are therefore, not recommended.

A minimum 1 µF is recommended close to the VIN and PGND pins for high frequency filtering. Smaller case size capacitors are recommended due to their lower ESR and ESL.

5.2 Output Capacitor

Even though the MIC2205 is optimized for a 2.2 µF output capacitor, output capacitance can be varied from 1 µF to 4.7 µF. The MIC2205 utilizes type III internal compensation and utilizes an internal high frequency zero to compensate for the double pole roll off of the LC filter. For this reason, larger output capacitors can create instabilities. X5R or X7R dielectrics are recommended for the output capacitor. Y5V dielectrics lose most of their capacitance over temperature and are therefore, not recommended.

In addition to a 2.2 µF, a small 10 nF is recommended close to the load for high frequency filtering. Smaller case size capacitors are recommended due to there lower ESR and ESL.

5.3 Inductor Selection

The MIC2205 is designed for use with a 2.2 µH inductor. Proper selection should ensure the inductor can handle the maximum average and peak currents required by the load. Maximum current ratings of the inductor are generally given in two methods; permissible DC current and saturation current. Permissible DC current can be rated either for a 40°C temperature rise or a 10% to 20% loss in inductance. Ensure that the inductor selected can handle the maximum operating current. When saturation current is specified, make sure that there is enough margin that the peak current will not saturate the inductor. Peak inductor current can be calculated as shown in Equation 5-1.

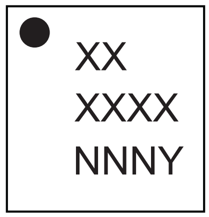
EQUATION 5-1:

$$I_{PK} = I_{OUT} + \frac{V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)}{2 \times f \times L}$$

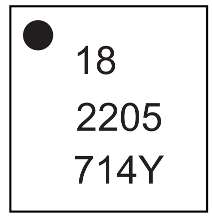
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

10-Lead VDFN*



Example



Legend:	XX...X	Product code or customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
	●, ▲, ▼	Pin one index is identified by a dot, delta up, or delta down (triangle mark).

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

Underbar (_) and/or Overbar (‾) symbol may not be to scale.

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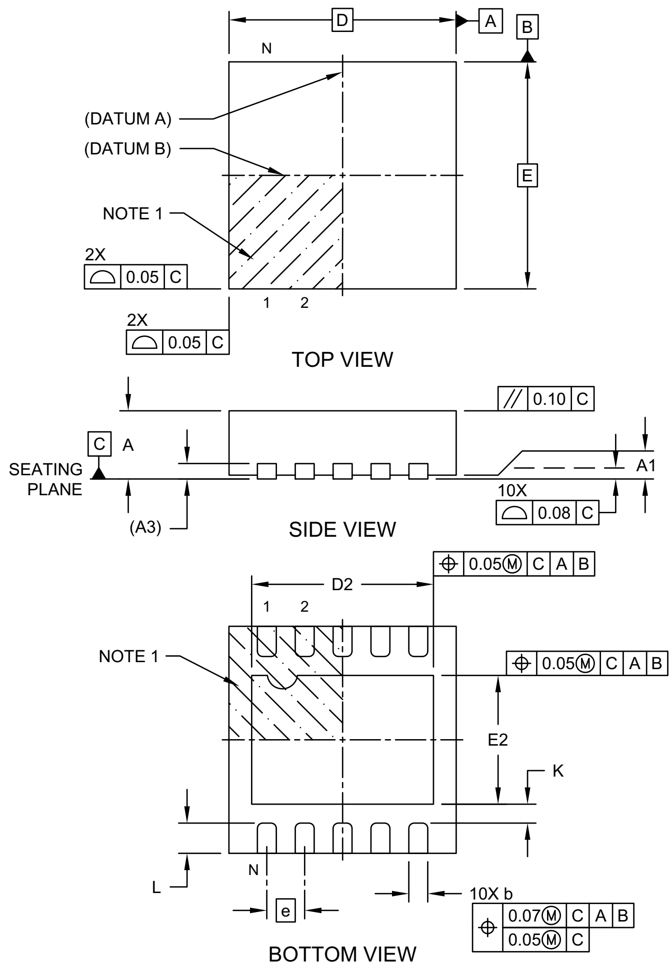
10-Lead VDFN (ML) Package Outline and Recommended Land Pattern

10-Lead Very Thin Plastic Dual Flat, No Lead Package (JFA) - 3x3x0.9 mm Body [VDFN]
Micrel Legacy Package DFN33-10LD-PL-1

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-1019-JFA Rev A Sheet 1 of 2

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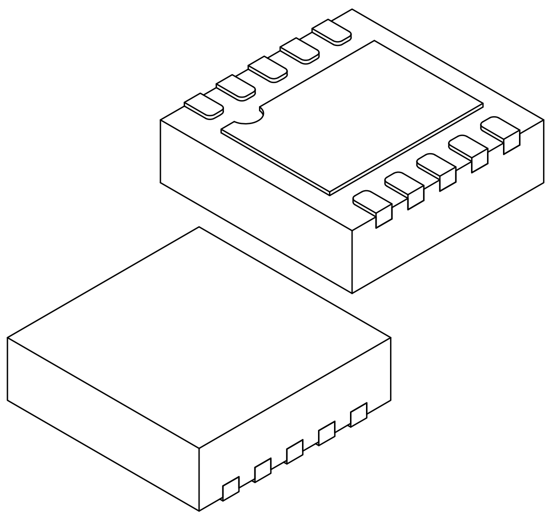
10-Lead VDFN (ML) Recommended Land Pattern

10-Lead Very Thin Plastic Dual Flat, No Lead Package (JFA) - 3x3x0.9 mm Body [VDFN]
Micrel Legacy Package DFN33-10LD-PL-1

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		10	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		3.00 BSC	
Exposed Pad Length	D2	2.35	2.40	2.45
Overall Width	E		3.00 BSC	
Exposed Pad Width	E2	1.65	1.70	1.75
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.35	0.40	0.45
Terminal-to-Exposed-Pad	K	0.20	–	–

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

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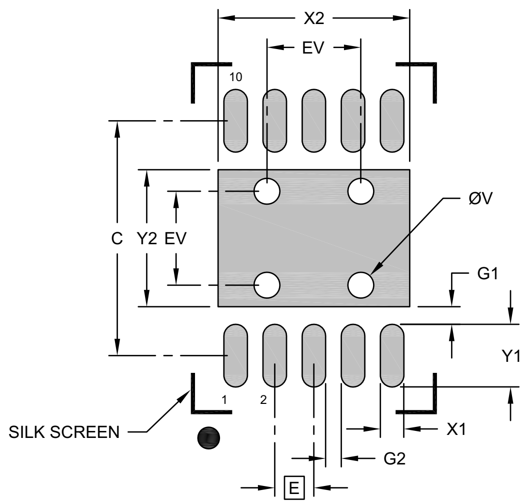
10-Lead VDFN (ML) Recommended Land Pattern

10-Lead Very Thin Plastic Dual Flat, No Lead Package (JFA) - 3x3x0.9 mm Body [VDFN]
Micrel Legacy Package DFN33-10LD-PL-1

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	X2			2.45
Optional Center Pad Length	Y2			1.75
Contact Pad Spacing	C		3.00	
Contact Pad Width (Xnn)	X1			0.30
Contact Pad Length (Xnn)	Y1			0.80
Contact Pad to Center Pad (Xnn)	G1	0.23		
Contact Pad to Contact Pad (Xnn)	G2	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-3019-JFA Rev A

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NOTES:

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APPENDIX A: REVISION HISTORY

Revision A (May 2019)

- Converted Micrel document MIC2205 to Microchip data sheet DS20006177A.
- Minor text changes throughout.

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NOTES:

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	–X.XX	X	XX	–XX
Device	Output Voltage	Junction Temperature Range	Package	Media Type

Device:	MIC2205:	2 MHz PWM Synchronous Buck Regulator with LDO Standby Mode
Output Voltage:	Blank =	Adjustable
	1.3 =	1.3V
	1.38 =	1.38V
	1.5 =	1.5V
	1.58 =	1.58V
	1.8 =	1.8V
	1.85 =	1.85V
Junction Temperature Range:	Y =	–40°C to +125°C, RoHS Compliant
Package:	ML =	10-Lead 3 mm x 3 mm x 0.9 mm VDFN
Media Type:	TR =	5,000/Reel

Note: Other voltage options available. Contact your Microchip Sales Office.

Examples:

a) MIC2205YML-TR: 2 MHz PWM Synchronous Buck Regulator with LDO Standby Mode, Adjustable Output Voltage, –40°C to +125°C Temp. Range, RoHS Compliant, 10-Lead 3 mm x 3 mm VDFN Package, 5000/Reel

b) MIC2205-1.3YML-TR: 2 MHz PWM Synchronous Buck Regulator with LDO Standby Mode, 1.3V Fixed Output Voltage, –40°C to +125°C Temp. Range, RoHS Compliant, 10-Lead 3 mm x 3 mm VDFN Package, 5000/Reel

c) MIC2205-1.38YML-TR: 2 MHz PWM Synchronous Buck Regulator with LDO Standby Mode, 1.38V Fixed Output Voltage, –40°C to +125°C Temp. Range, RoHS Compliant, 10-Lead 3 mm x 3 mm VDFN Package, 5000/Reel

d) MIC2205-1.58YML-TR: 2 MHz PWM Synchronous Buck Regulator with LDO Standby Mode, 1.58V Fixed Output Voltage, –40°C to +125°C Temp. Range, RoHS Compliant, 10-Lead 3 mm x 3 mm VDFN Package, 5000/Reel

e) MIC2205-1.8YML-TR: 2 MHz PWM Synchronous Buck Regulator with LDO Standby Mode, 1.8V Fixed Output Voltage, –40°C to +125°C Temp. Range, RoHS Compliant, 10-Lead 3 mm x 3 mm VDFN Package, 5000/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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