MMBT4403WT1G

Switching Transistor

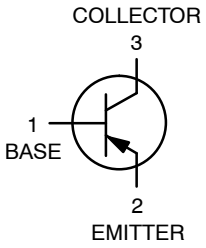
PNP Silicon

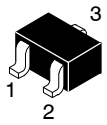
Features

- Moisture Sensitivity Level: 1
- ESD Rating: Human Body Model; 4 kV,
  Machine Model; 400 V
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

ON Semiconductor®

http://onsemi.com





SC−70
CASE 419
STYLE 3

MAXIMUM RATINGS

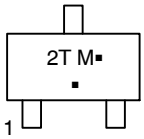
Rating	Symbol	Value	Unit
Collector−Emitter Voltage	V_{CEO}	−40	Vdc
Collector−Base Voltage	V_{CBO}	−40	Vdc
Emitter−Base Voltage	V_{EBO}	−5.0	Vdc
Collector Current − Continuous	I_C	−600	mAdc

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation FR−5 Board T_A = 25°C	P_D	150	mW
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	833	°C/W
Junction and Storage Temperature	T_J, T_{stg}	−55 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

MARKING DIAGRAM



2T = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation may vary depending upon manufacturing location.

ORDERING INFORMATION

Device	Package	Shipping†
MMBT4403WT1G	SC−70 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector−Emitter Breakdown Voltage (Note 1) (I_C = −1.0 mAdc, I_B = 0)	$V_{(BR)CEO}$	−40	−	Vdc
Collector−Base Breakdown Voltage (I_C = −0.1 mAdc, I_E = 0)	$V_{(BR)CBO}$	−40	−	Vdc
Emitter−Base Breakdown Voltage (I_E = −0.1 mAdc, I_C = 0)	$V_{(BR)EBO}$	−5.0	−	Vdc
Base Cutoff Current (V_{CE} = −35 Vdc, V_{EB} = −0.4 Vdc)	I_{BEV}	−	−0.1	μAdc
Collector Cutoff Current (V_{CE} = −35 Vdc, V_{EB} = −0.4 Vdc)	I_{CEX}	−	−0.1	μAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = −0.1 mAdc, V_{CE} = −1.0 Vdc) (I_C = −1.0 mAdc, V_{CE} = −1.0 Vdc) (I_C = −10 mAdc, V_{CE} = −1.0 Vdc) (I_C = −150 mAdc, V_{CE} = −2.0 Vdc) (Note 1) (I_C = −500 mAdc, V_{CE} = −2.0 Vdc) (Note 1)	h_{FE}	 30 60 100 100 20	 − − − 300 −	−
Collector−Emitter Saturation Voltage (Note 1) (I_C = −150 mAdc, I_B = −15 mAdc) (I_C = −500 mAdc, I_B = −50 mAdc)	$V_{CE(sat)}$	 − −	 −0.4 −0.75	Vdc
Base−Emitter Saturation Voltage (Note 1) (I_C = −150 mAdc, I_B = −15 mAdc) (I_C = −500 mAdc, I_B = −50 mAdc)	$V_{BE(sat)}$	 −0.75 −	 −0.95 −1.3	Vdc
SMALL−SIGNAL CHARACTERISTICS				
Current−Gain − Bandwidth Product (I_C = −20 mAdc, V_{CE} = −10 Vdc, f = 100 MHz)	f_T	200	−	MHz
Collector−Base Capacitance (V_{CB} = −10 Vdc, I_E = 0, f = 1.0 MHz)	C_{cb}	−	8.5	pF
Emitter−Base Capacitance (V_{BE} = −0.5 Vdc, I_C = 0, f = 1.0 MHz)	C_{eb}	−	30	pF
Input Impedance (I_C = −1.0 mAdc, V_{CE} = −10 Vdc, f = 1.0 kHz)	h_{ie}	1.5	15	kΩ
Voltage Feedback Ratio (I_C = −1.0 mAdc, V_{CE} = −10 Vdc, f = 1.0 kHz)	h_{re}	0.1	8.0	X 10^{-4}
Small−Signal Current Gain (I_C = −1.0 mAdc, V_{CE} = −10 Vdc, f = 1.0 kHz)	h_{fe}	60	500	−
Output Admittance (I_C = −1.0 mAdc, V_{CE} = −10 Vdc, f = 1.0 kHz)	h_{oe}	1.0	100	μmhos
SWITCHING CHARACTERISTICS				
Delay Time	(V_{CC} = −30 Vdc, V_{EB} = −2.0 Vdc, I_C = −150 mAdc, I_{B1} = −15 mAdc)	t_d	−	15	ns
Rise Time		t_r	−	20	
Storage Time	(V_{CC} = −30 Vdc, I_C = −150 mAdc, I_{B1} = I_{B2} = −15 mAdc)	t_s	−	225	ns
Fall Time		t_f	−	30	

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

SWITCHING TIME EQUIVALENT TEST CIRCUIT

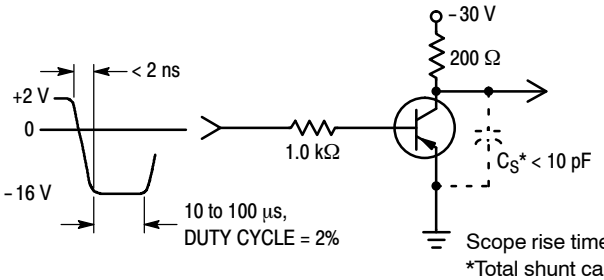
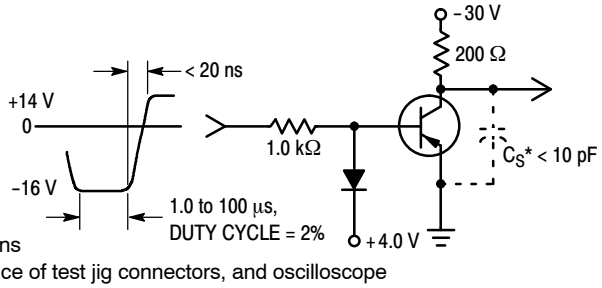


Figure 1. Turn−On Time



*Total shunt capacitance of test jig connectors, and oscilloscope

Figure 2. Turn−Off Time

TRANSIENT CHARACTERISTICS

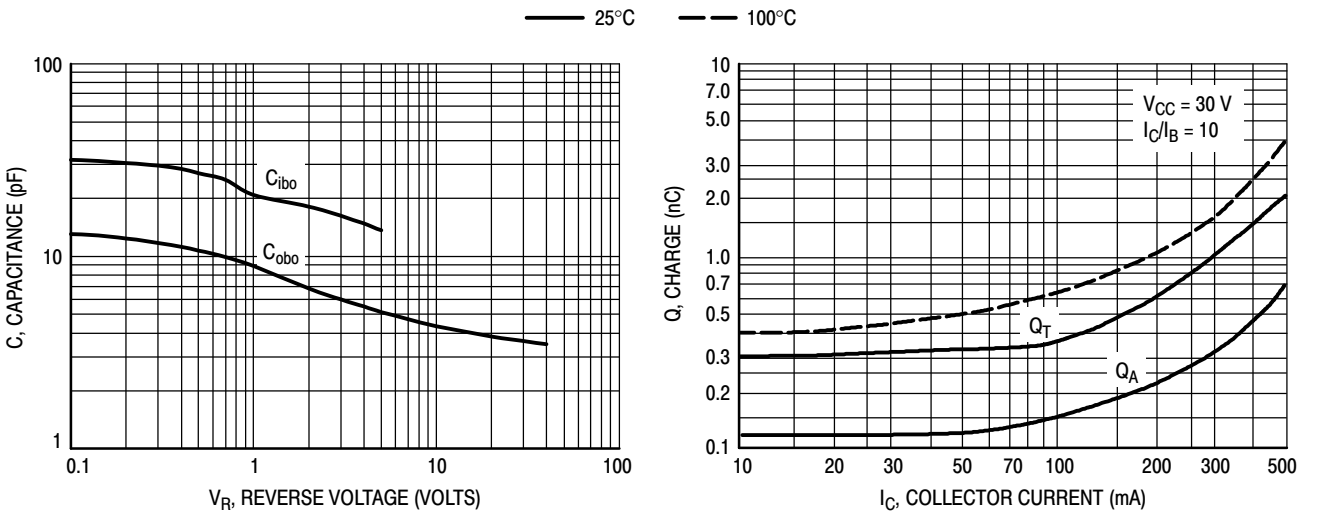


Figure 3. Capacitances

Figure 4. Charge Data

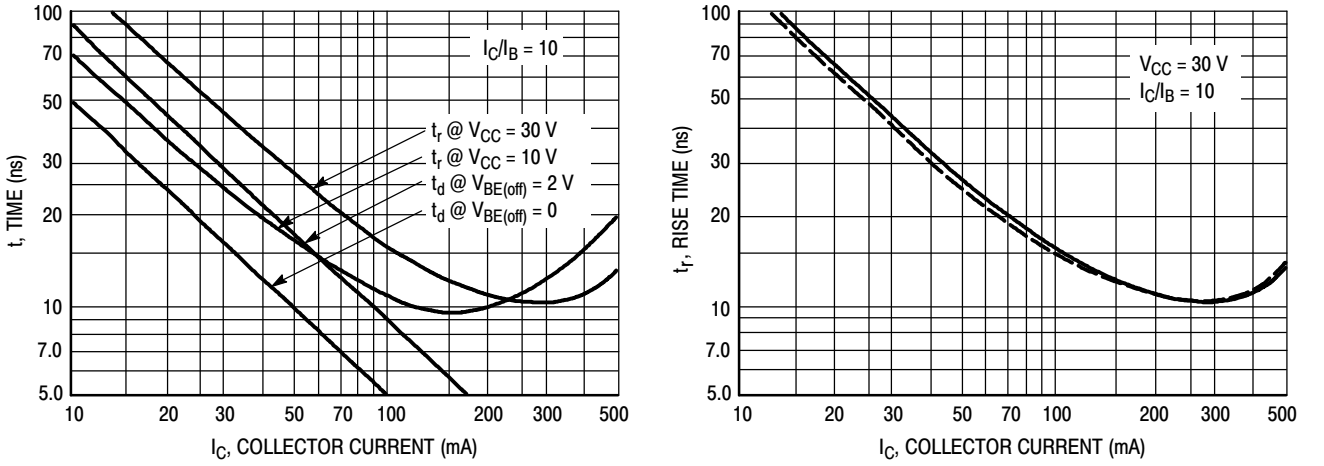


Figure 5. Turn−On Time

Figure 6. Rise Time

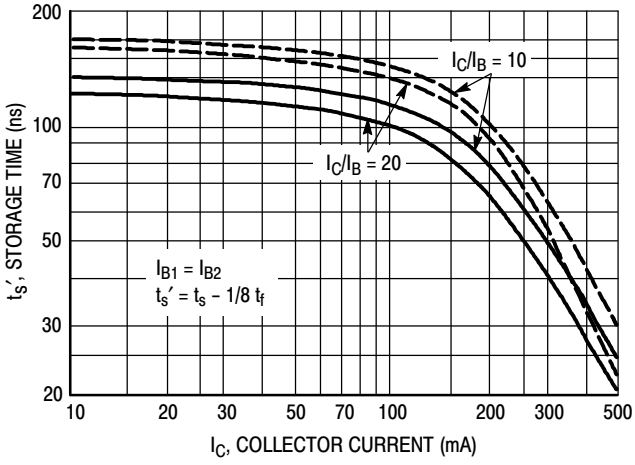


Figure 7. Storage Time

SMALL−SIGNAL CHARACTERISTICS NOISE FIGURE

V_{CE} = −10 Vdc, T_A = 25°C; Bandwidth = 1.0 Hz

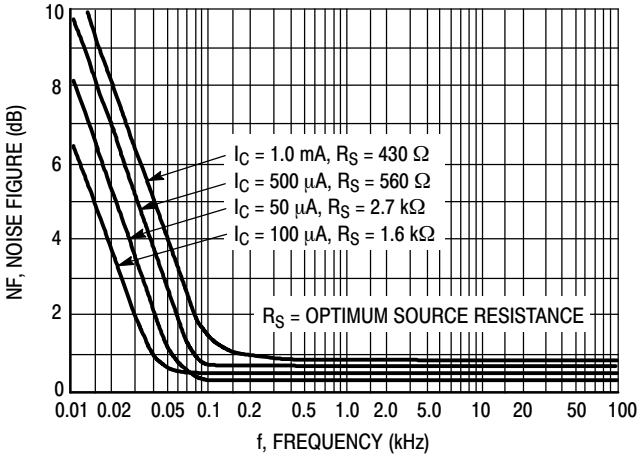


Figure 8. Frequency Effects

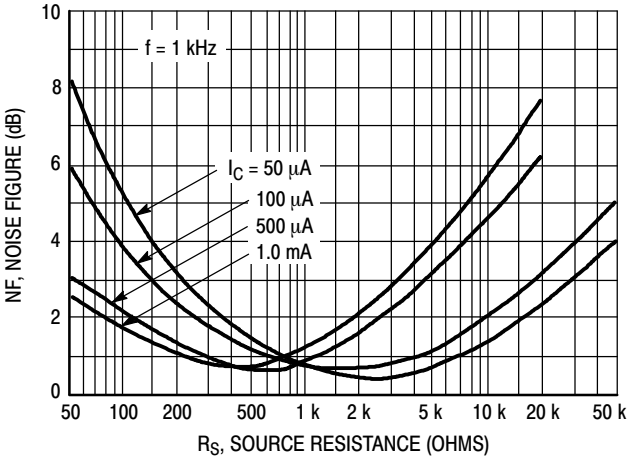


Figure 9. Source Resistance Effects

h PARAMETERS

V_{CE} = 10 Vdc, f = 1.0 kHz, T_A = 25°C

This group of graphs illustrates the relationship between h_{fe} and other "h" parameters for this series of transistors. To obtain these curves, a high−gain and a low−gain unit were selected from the MMBT4403WT1 lines, and the same units were used to develop the correspondingly numbered curves on each graph.

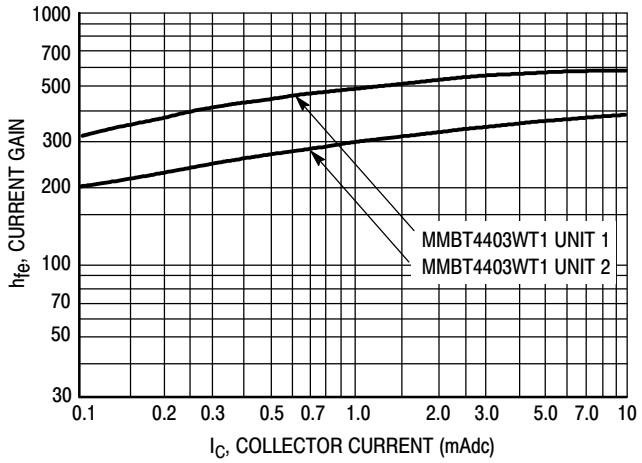


Figure 10. Current Gain

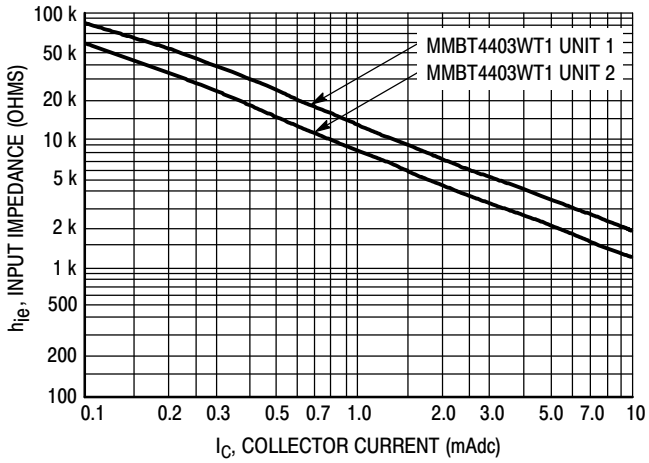


Figure 11. Input Impedance

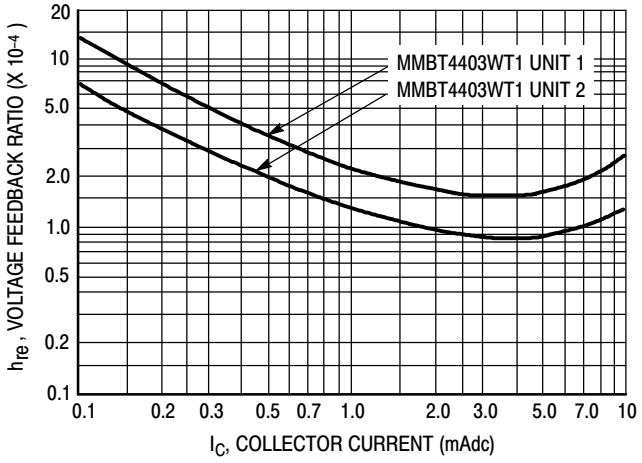


Figure 12. Voltage Feedback Ratio

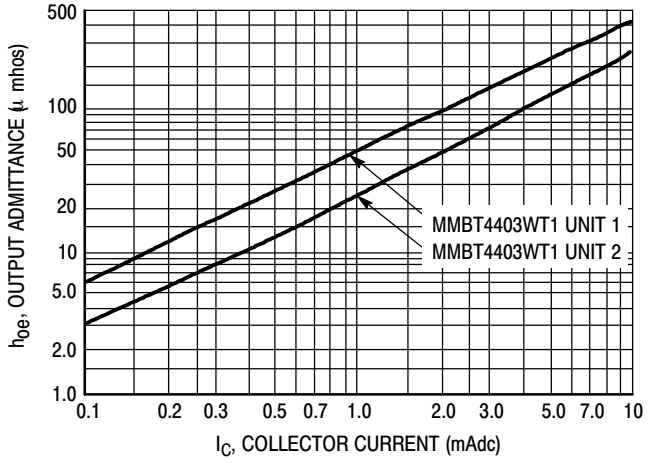


Figure 13. Output Admittance

STATIC CHARACTERISTICS

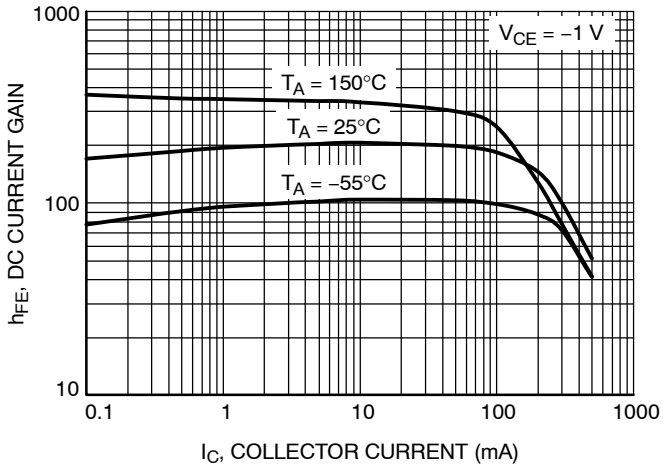


Figure 14. DC Current Gain vs. Collector Current

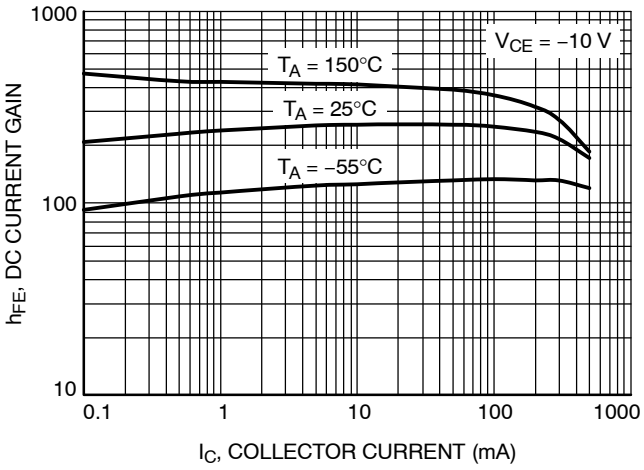


Figure 15. DC Current Gain vs. Collector Current

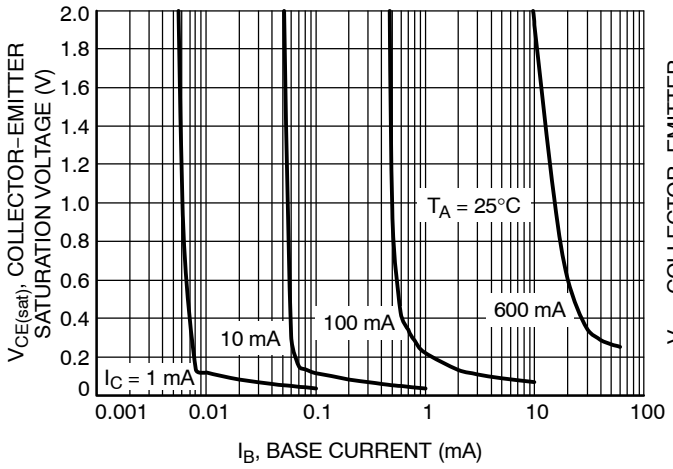


Figure 16. Saturation Region

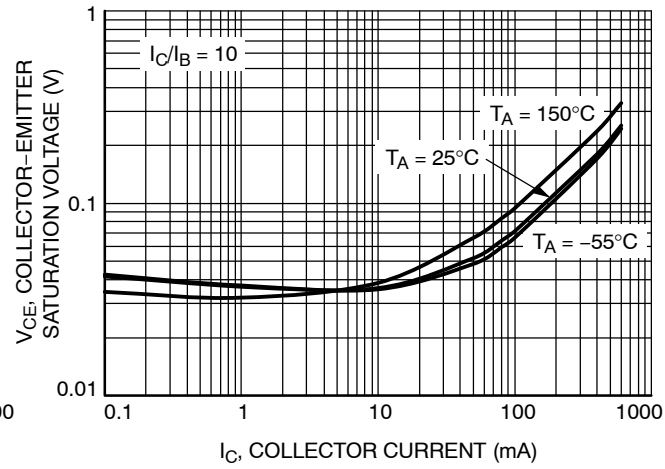


Figure 17. Collector Emitter Saturation Voltage vs. Collector Current

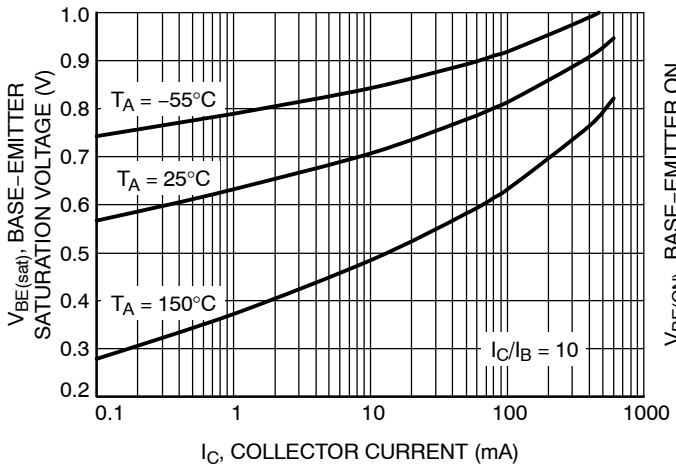


Figure 18. Base Emitter Saturation Voltage vs. Collector Current

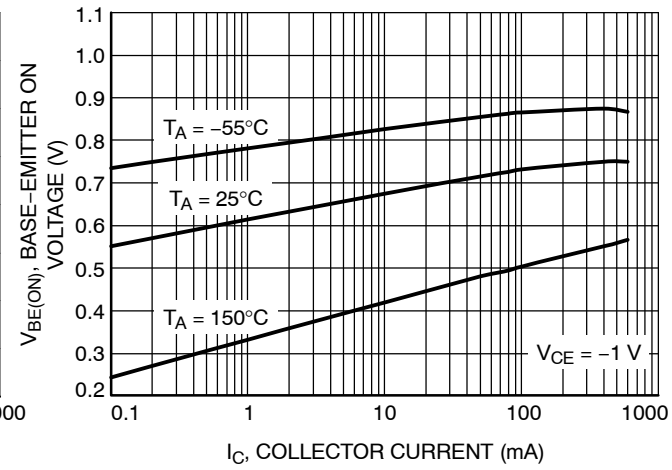


Figure 19. Base−Emitter Turn−On Voltage vs. Collector Current

STATIC CHARACTERISTICS

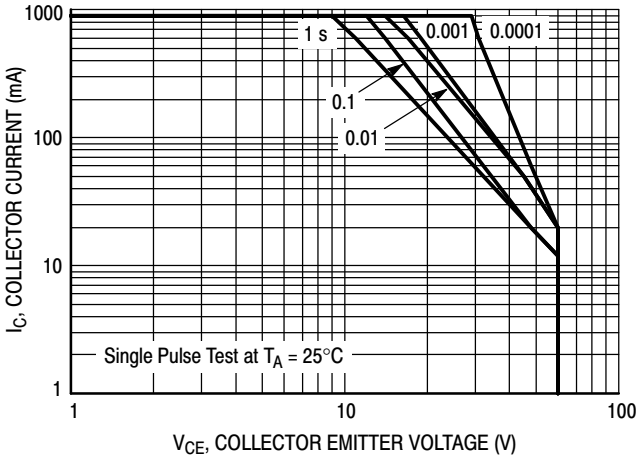


Figure 20. Safe Operating Area

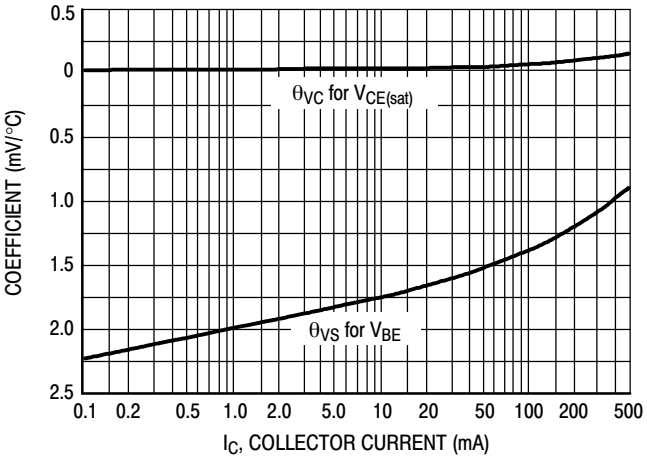


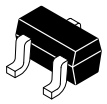
Figure 21. Temperature Coefficients

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

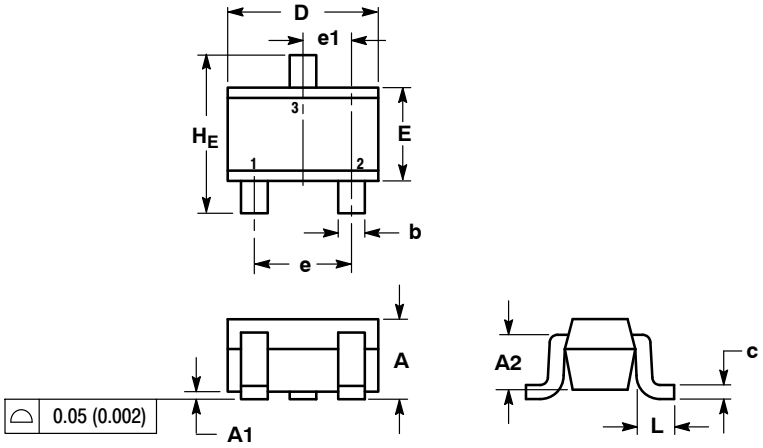
ON Semiconductor®

SC−70 (SOT−323)
CASE 419−04
ISSUE N

DATE 11 NOV 2008



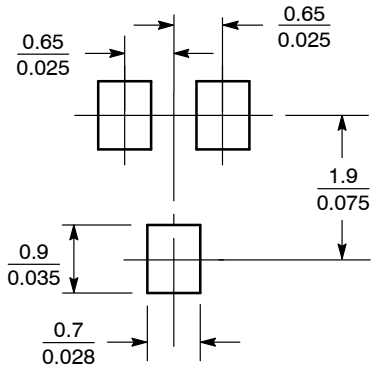
SCALE 4:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.80	0.90	1.00	0.032	0.035	0.040
A1	0.00	0.05	0.10	0.000	0.002	0.004
A2		0.70 REF			0.028 REF	
b	0.30	0.35	0.40	0.012	0.014	0.016
c	0.10	0.18	0.25	0.004	0.007	0.010
D	1.80	2.10	2.20	0.071	0.083	0.087
E	1.15	1.24	1.35	0.045	0.049	0.053
e	1.20	1.30	1.40	0.047	0.051	0.055
e1		0.65 BSC			0.026 BSC	
L	0.20	0.38	0.56	0.008	0.015	0.022
H_E	2.00	2.10	2.40	0.079	0.083	0.095

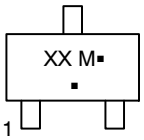
SOLDERING FOOTPRINT*



SCALE 10:1 $\left(\frac{mm}{inches}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM



XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

STYLE 1:
CANCELLED

STYLE 2:
PIN 1. ANODE
2. N.C.
3. CATHODE

STYLE 3:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 5:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 6:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 7:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 8:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. CATHODE−ANODE

STYLE 10:
PIN 1. CATHODE
2. ANODE
3. ANODE−CATHODE

STYLE 11:
PIN 1. CATHODE
2. CATHODE
3. CATHODE

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DESCRIPTION:	**SC−70 (SOT−323)**	**PAGE 1 OF 1**

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