PCN Number:	20190911000.0	PCN Date:	Sept 17, 2019
Title:	TPS63805 Design Change and Datasheet Updates		
Customer Contact:	PCN Manager	Dept:	Quality Services

Change Type:					
☐	Assembly Site	☐	Assembly Process	☐	Assembly Materials
☒	Design	☒	Electrical Specification	☐	Mechanical Specification
☐	Test Site	☐	Packing/Shipping/Labeling	☐	Test Process
☐	Wafer Bump Site	☐	Wafer Bump Material	☐	Wafer Bump Process
☐	Wafer Fab Site	☐	Wafer Fab Materials	☐	Wafer Fab Process
		☐	Part number change		

PCN Details

Description of Change:

This notification is to inform of a design change to the TPS63805 devices. Affected devices are listed in the Product Affected section of this document.

The design change is a minor metal fix to improve overall performance, which includes

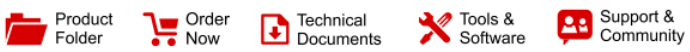
- Changes in internal logic
- Adjustments to internal timers
- Improved ESD robustness
- Loop compensation and gain of error amplifier optimized
- OTP trim settings for buck mode operation enhanced (off time)

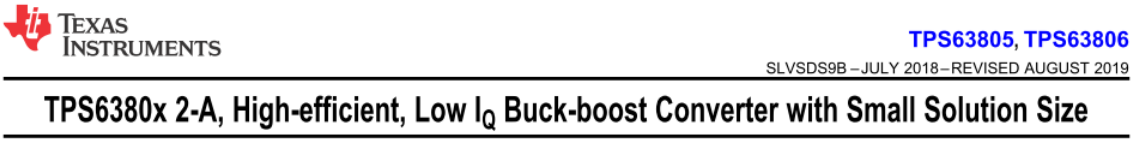
If samples are required, please contact your local Field Sales Representative, or the Business Unit at lbs_request@list.ti.com.

The datasheet number will be changing:

Current	New
Datasheet Number	**Datasheet Number**
SLVSDS9A	SLVSDS9B

The product datasheet(s) is also updated as seen in the change revision history below:





4 Revision History

Changes from Revision A (October 2018) to Revision B	Page
• Changed the *Features* list	1
• Added the TPS63086 to the data sheet	1
• Changed the adjustable output voltage range from 5.0 V to 5.2 V	1
• Deleted *Operates with low and high output capacitance values*from features list	1
• Deleted package size parameters for features list	1
• Changed *Description* to address TPS63805 and TPS63806	1
• Changed Efficiency vs. Output current curve	1
• Added If not used can be left floating for PG-pin	5
• Added V_{IN} = 3.6 V for typical value in condition text	6
• Changed V_{OUT} from 5 V to 5.2 V condition text	6
• Added PG Pin	6
• Changed PFM/PWM pin name to Mode	6
• Changed V_O from 5 V to 5.2 V	6
• Changed typical effective output capacitance from 10 uF to 8.2 uF	6
• Added Vo conditions for C_O range	6
• Changed Soft-start Current limit ramp time test conditions	7
• Changed typical Soft-start Current limit ramp time from 0.6 ms to 224 us	7
• Changed Delay from EN-edge until rising V_{OUT} test conditions	7
• Changed typical Delay from EN-edge until rising V_{OUT} from 100 us to 321 us	7
• Changed typical Overvoltage Protection Threshold from 5.66 V to 5.7 V	7
• Changed maximum Overvoltage Protection Threshold from 5.8 V to 5.9 V	7
• Changd Peak Inductor Current to enter PFM-Mode to 1.06 A typical only	7
• Changed minimum Peak Current Limit Boost Mode from 3.5 A to 4 A	7
• Changed typical Peak Current Limit Boost Mode from 4.8 A to 5 A	7
• Changed maximum Peak Current Limit Boost Mode from 5.8 A to 5.75 A	7
• Changed Peak Current Limit for Reverse Operation to 0.9 A typical only	7
• Changed Inductor Switching Frequency, Buck Mode from 2.7 MHz to 1.6 MHz	8
• Changed typical Line regulation from 0.5% to 0.3 %	8
• Changed typical Load regulation from 0.5% to 0.1%	8
• Changed Quiescent Current vs. Temperature Curve for TPS63805 in Typical Characteristics	9
• Changed Typical Characteristics shutdown current vs. temperature curve for TPS63805	9

These changes may be reviewed at the datasheet link provided:

http://www.ti.com/lit/ds/symlink/tps63805.pdf

Reason for Change:

Improved device performance

Anticipated impact on Form, Fit, Function, Quality or Reliability (positive / negative):

None

Changes to product identification resulting from this PCN:

Die Rev designator will change as shown in the table and sample label below:

Current	New
Die Rev [2P]	**Die Rev [2P]**
A	**B**

Sample product shipping label (not actual product label)

Product Affected: Design Change and datasheet updates

TPS63805YFFR	TPS63805YFFT

Qualification Report

Approve Date 04-Sep-2019

Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

Type	Test Name / Condition	Duration	Qual Device: TPS63805YFF	Qual Device: TPS63806YFF	QBS Product Reference: BQ25898CYFFR	QBS Product Reference: TPS63805YFF
-	Non-Volatile Memory High Temp. Storage Bake, 150C	1000 Hours	-	-	-	3/231/0
ED	Electrical Characterization	Per Datasheet Parameters	-	Pass	Pass	Pass
HAST	Biased HAST, 130C/85%RH	96 Hours	-	-	-	3/231/0
HBM	ESD - HBM	3000V	-	1/3/0	-	1/3/0
CDM	ESD - CDM	1000 V	-	1/3/0	-	-
HTOL	Life Test, 150C	300 Hours	-	-	-	3/231/0
HTSL	High Temp Storage Bake 170C	420 Hours	-	-	3/231/0	-
LU	Latch-up	(per JESD78)	-	1/6/0	-	1/6/0
PD	Physical Dimensions	--	-	-	3/15/0	-
SBS	Bump-shear	--	-	-	5/150/0	-
TC	Temperature Cycle, -55/125C	700 Cycles	-	-	3/231/0	-
TC	Temperature Cycle, -65/150C	500 Cycles	-	-	-	3/231/0
UHAST	Unbiased HAST, 130C/85%RH	96 Hours	-	-	3/231/0	3/230/0

- QBS: Qual By Similarity
- Qual Devices qualified at LEVEL 1-260C: TPS63805YFF, TPS63806YFF
- Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable
- The following are equivalent HTOL options based on an activation energy of 0.7eV: 125C/1k Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours
- The following are equivalent HTSL options based on an activation energy of 0.7eV: 150C/1k Hours, and 170C/420 Hours
- The following are equivalent Temp Cycle options per JESD47: -55C/125C/700 Cycles and -65C/150C/500 Cycles

Quality and Environmental data is available at TI's external Web site: http://www.ti.com/

Green/Pb-free Status:
Qualified Pb-Free (SMT) and Green

For questions regarding this notice, e-mails can be sent to the regional contacts shown below, or you can contact your local Field Sales Representative.

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