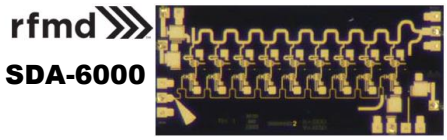
SDA-6000

GaAs Distributed Amplifier



Package: Die, 2.21mm x 1.21mm x 0.102mm

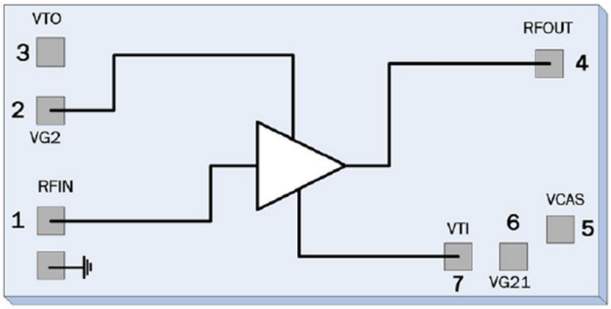
RFMD's SDA-6000 is a directly coupled (DC) GaAs microwave monolithic integrated circuit (MMIC) distributed driver amplifier die designed to support a wide array of high frequency commercial, military, and space applications. They are ideal for wideband amplifier gain blocks, modulators, clock drivers, broadband automated test equipment (ATE), military, and aerospace applications.

Features

- DC to 50GHz Operation
- Output Voltage to $3V_{PP}$
- Gain = 8dB Typical
- Noise Figure = 4.5dB Typical
- 80mA Total Current

Applications

- Drive for Single-Ended (SE) MZM
- NRZ, DPSK, ODB, RZ
- Clock Driver for RZ and CS Pulse Carver
- Broadband ATE
- Instrumentation
- Military
- Aerospace



Functional Block Diagram

Ordering Information

SDA-6000	GaAs Distributed Amplifier, GelPak, 10 pieces or more
SDA-6000SB	Sample Bag, GaAs Distributed Amplifier, GelPak, 2 pieces

RF Micro Devices Inc. 7628 Thorndike Road, Greensboro, NC 27409-9421
For sales or technical support, contact RFMD at +1.336.678.5570 or customerservice@rfmd.com.

DS140210

Absolute Maximum Ratings

Parameter	Rating	Unit
Drain Bias Voltage (V_{DD})	+9.0	V_{DC}
Gate Bias Voltage (V_{TI})	-2 to +1	V_{DC}
Gate Bias Voltage (V_{G2})	(V_{DD}-5.0) to V_{DD}	V_{DC}
RF Input Power (V_{DD} = +8.0V_{DC})	+15	dBm
Operating Junction Temperature (T_J)	+150	°C
Continuous Power Dissipation (T = +85°C)	700	mW
Thermal Resistance (Pad to Die Bottom)	93	°C/W
Storage Temperature	-40 to +150	°C
Operating Temperature	-40 to +85	°C
ESD JESD22-A114 Human Body Model (HBM)	Class 0 (All Pads)	

Caution! ESD sensitive device.

RFMD Green: RoHS compliant per EU Directive 2011/65/EU, halogen free per IEC 61249-2-21, <1000ppm each of antimony trioxide in polymeric materials and red phosphorus as a flame retardant, and <2% antimony solder.

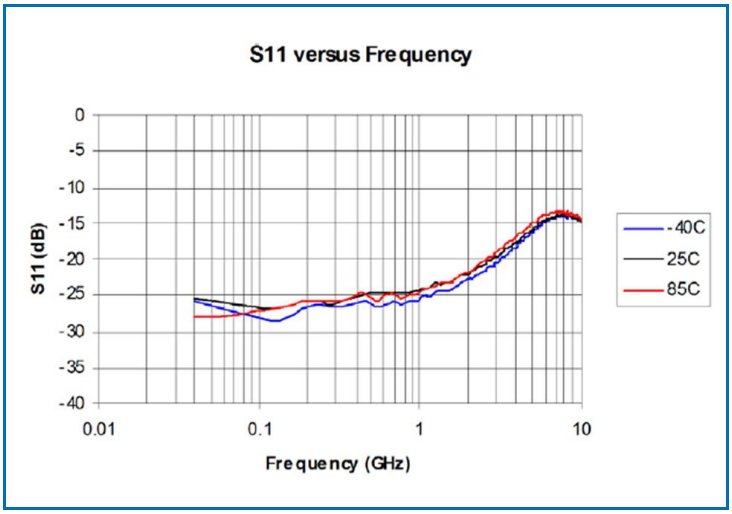
Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

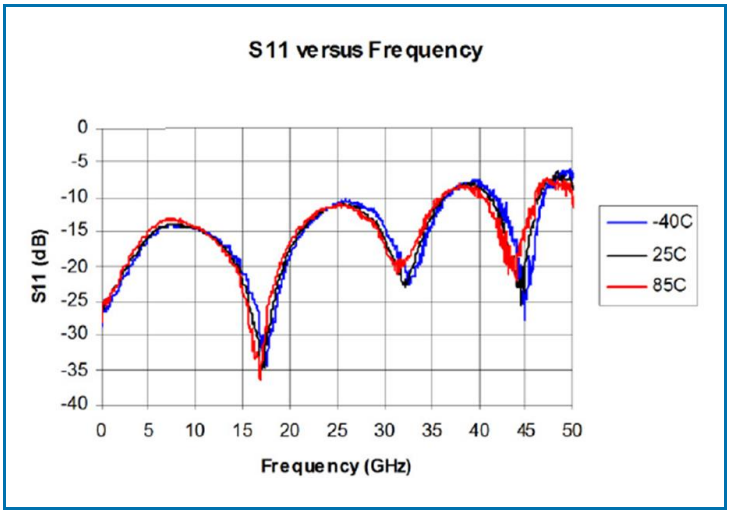
Nominal Operating Parameters

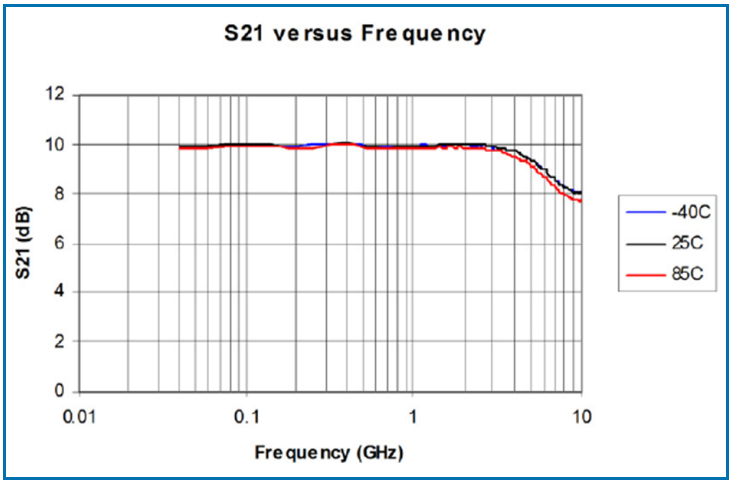
Parameter	Specification			Unit	Condition
	Min	Typ	Max		
General Performance					**T_A = +25°C, V_{DD} = +5V_{DC}, V_{G2} = +2.2V_{DC}, I_{DD} = 80mA***
Operating Frequency	DC		50	GHz	3dB BW
Gain		8		dB	
Output Voltage		3		V_{P-P}	
OIP3 at Mid-Band		24		dBm	
P1dB at Mid-Band		14.5		dBm	20GHz
P3dB at Mid-Band		16.5		dBm	20GHz
Noise Figure at Mid-Band		5.0		dB	20GHz
Input Return Loss		12		dB	DC to 50GHz
Output Return Loss		12		dB	DC to 50GHz
Supply Current		80		mA	
Supply Voltage		5		V_{DC}	

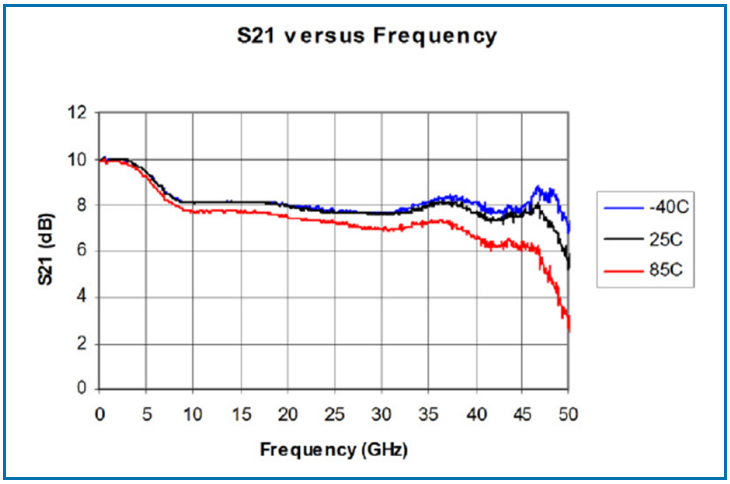
*Adjust V_{TI} between -1.5V_{DC} to +0.2V_{DC} to achieve I_{DD} = 80mA typical.

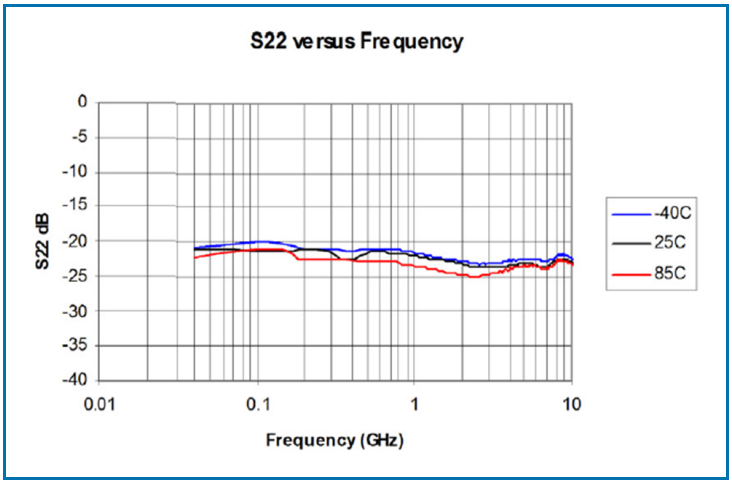
Typical Performance (See section at the end of the data sheet for measurement comments)

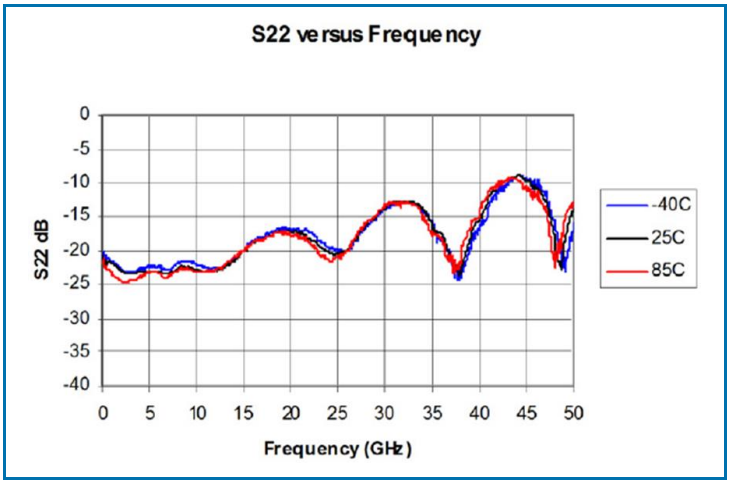




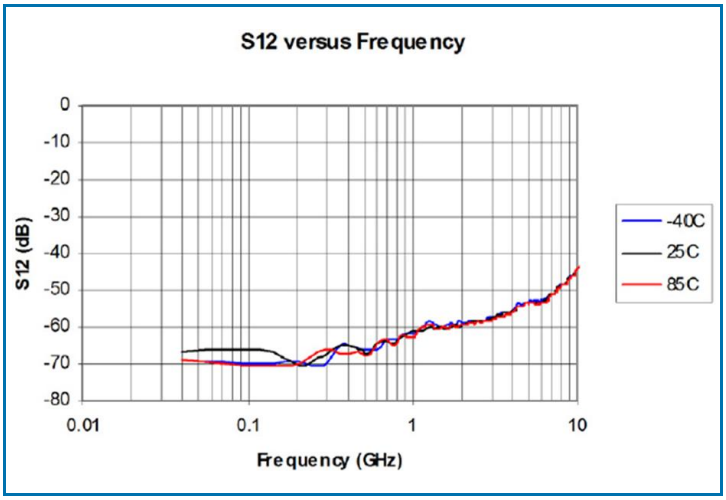


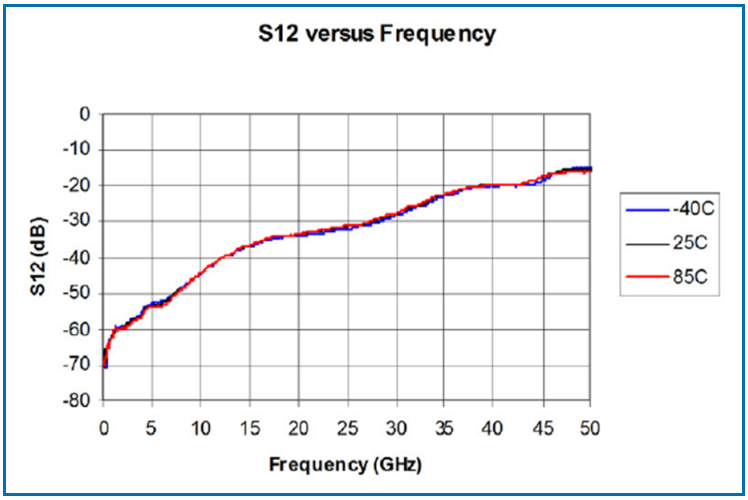


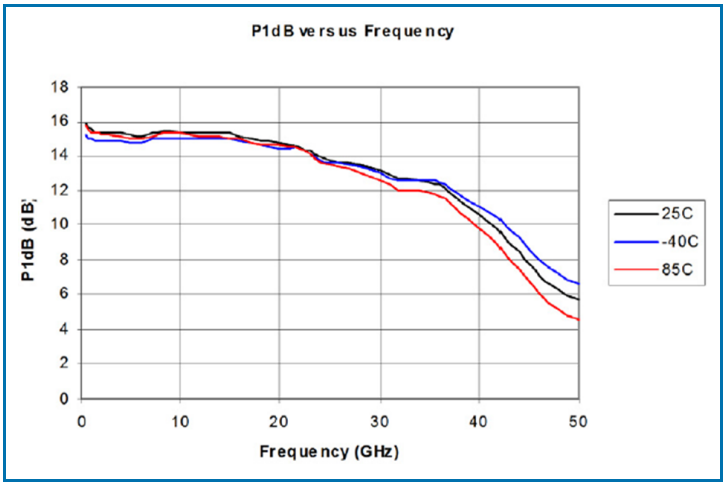


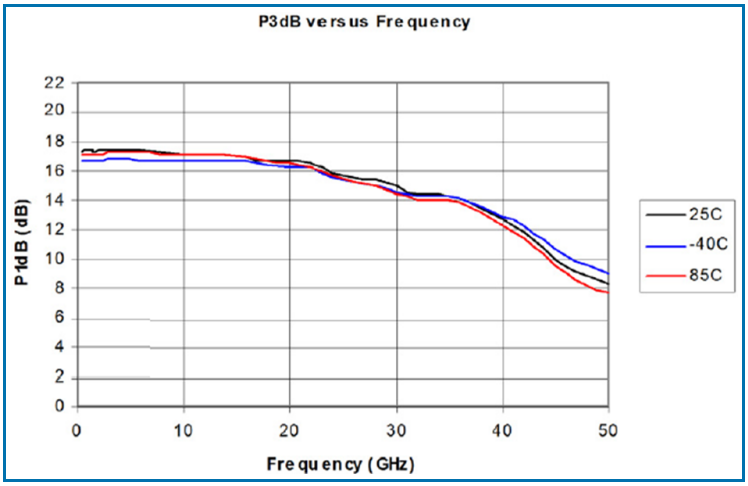


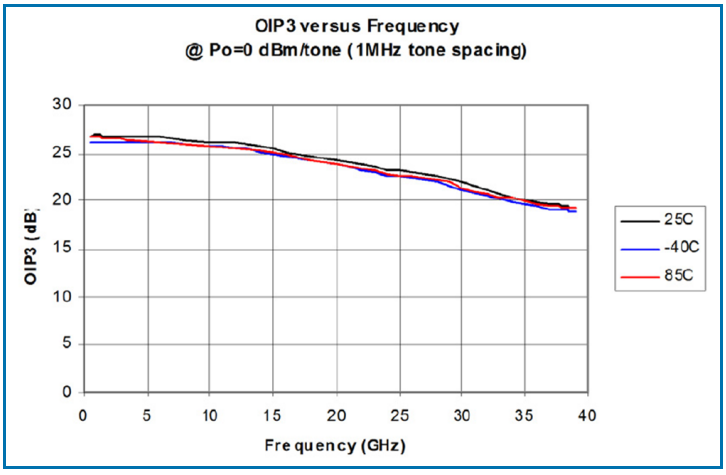
Typical Performance (Continued)

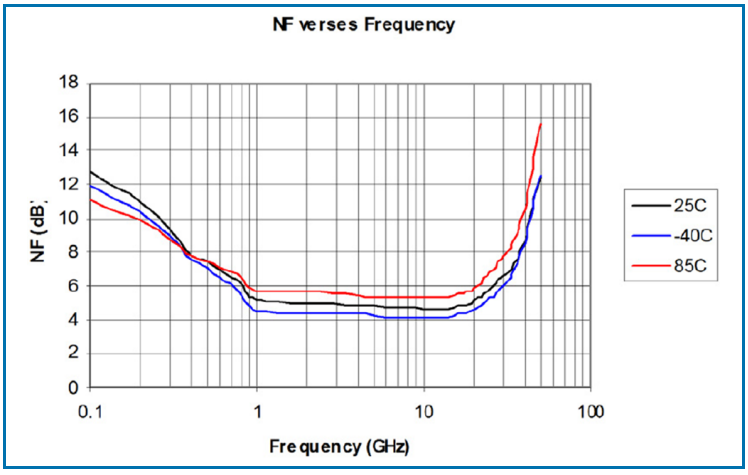




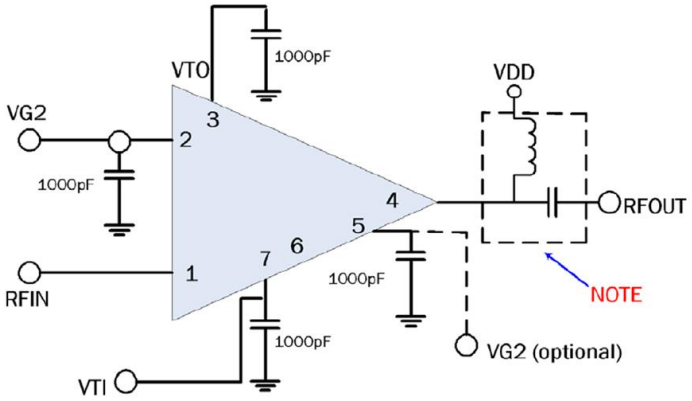






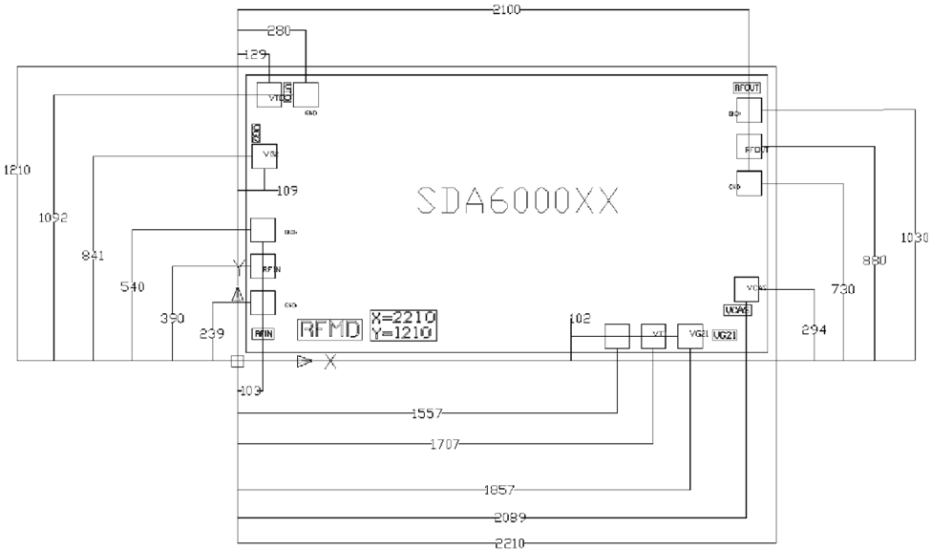


Application Schematic



NOTE: *Drain Bias (Vdd) must be applied through a broadband bias tee or external bias network.*

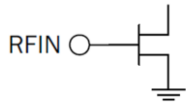
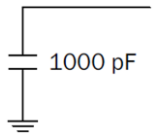
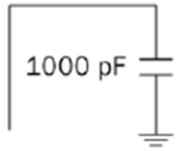
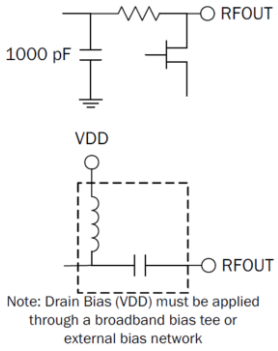
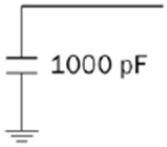
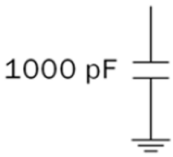
Die Drawing (Dimensions in microns)



Notes:

1. No connection required for unlabeled bond pads
2. Die thickness is 0.102mm (4mil)
3. Typical bond pad is 0.100mm square
4. Backside metallization: gold
5. Backside metal is ground
6. Bond pad metallization: gold

Pin Names and Descriptions

Pin	Name	Description	Interface Schematic
1	RFIN	RF Input. This pad is DC coupled and matched to 50Ω from DC to 50GHz. 50Ω microstrip transmission line on 0.127mm (5mil) thick alumina thin film substrate is recommended for RF input and output. A DC blocking capacitor is required for this connection. The calue of this capacitor will be based on the desired frequency range of application.	
2	VG2	Each amplifier stage in the SDA-6000 is a cascade configuration. The gate of each upper FET in the cascade amplifiers is biased with the 2.2 V_{DC} supply mentioned in this data sheet. The DC connection for the upper device gates runs across the length of the die. Pads 2 and 5 are both on this DC connection but are on opposite ends of the die. The 2.2V_{DC} connection can therefore be placed on either pad. A bypass capacitor is recommended on both ends, pads 2 and 5.	
3	VTO	The output drain termination pad. This pad requires a 1000pF bypass capacitor with the shortest wirebond length to prevent low frequency gain ripple.	
4	RFOUT and VDD	RF Output. 50Ω microstrip transmission line on 0.127mm (5mil) thick alumina thin film substrate is recommended for RF input and output. Connect the DC bias (V_{DD}) network to provide drain current (I_{DD}). Note: Drain Bias (V_{DD}) must be applied through a broadband bias tee or external bias network.	
5	VCAS	Each amplifier stage in the SDA-6000 is a cascade configuration. The gate of each upper FET in the cascade amplifiers is biased with the 2.2V_{DC} supply mentioned in this data sheet. The DC connection for the upper device gates runs across the length of the die. Pads 2 and 5 are both on this DC connection but are on opposite ends of the die. The 2.2V_{DC} connection can therefore be placed on either pad. A bypass capacitor is recommended on both ends, pads 2 and 5.	
6	VG21	Not connected.	
7	VTI	Input gate voltage for the lower devices in the cascade amplifier. This pad also serves as the RF ground for the input termination resistor. The DC voltage applied to this pad will be between -2V_{DC} (device is pinched OFF) to +1V_{DC} (fully ON). The value of this capacitor will effect the low frequency response of the amplifier.	
Die	GND	Ground connection. Connect die bottom directly to ground plane for best performance. NOTE: The die should be connected directly to the ground plane with conductive epoxy.	

Bias Sequence (Turn Device On):

VTI - Apply negative -2.0 volts. (This shuts the device off.)

VG2 - Apply positive 2.2 volts.

VDD - Apply positive 5.0 volts to the RF output bias tee.

Important - Adjust VTI between -2 to +1 volts to achieve IDD = 80mA nominal.

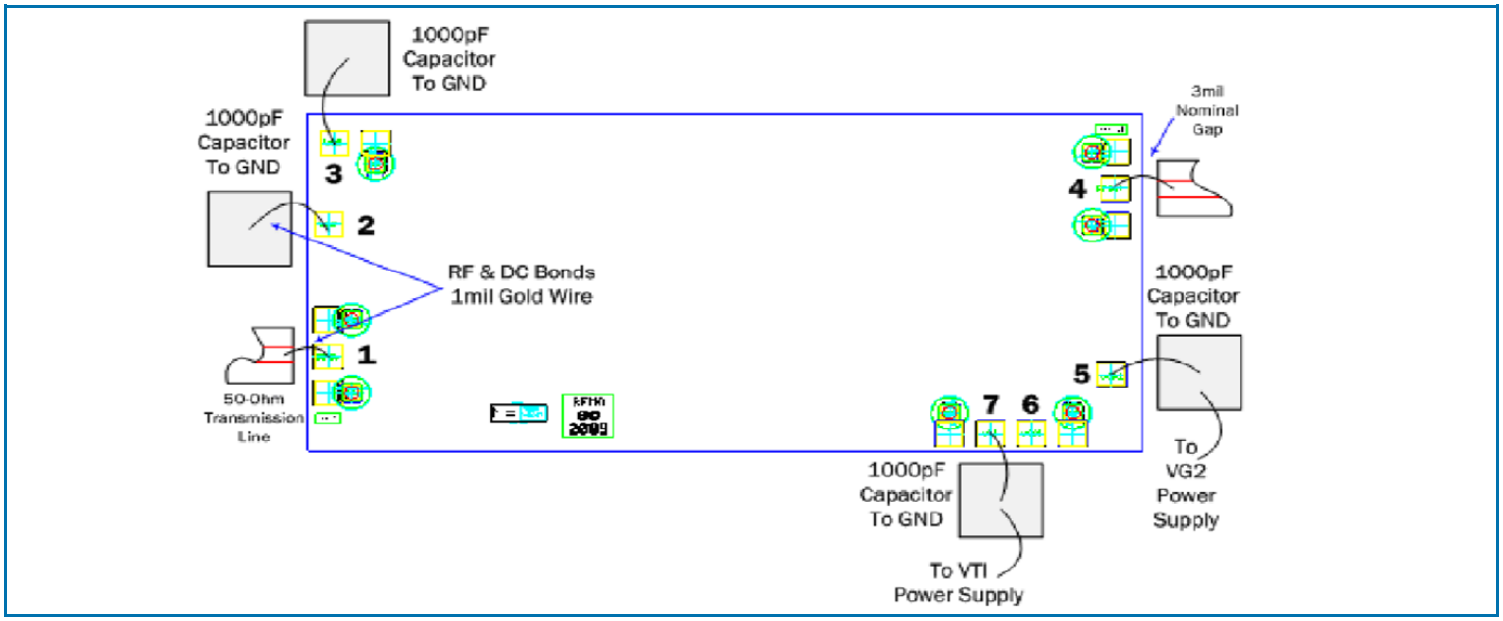
Bias Sequence (Turn Device Off):

VTI - Return to negative -2.0 volts.

VDD - Remove positive 5.0 volts to the RF output bias tee.

VG2 - Remove positive 2.2 volts.

Assembly Diagram



Measurement Technique

All data presented in this document represents the integrated circuit and accompanying bond wires.

All performance data reported in this document were measured in the following manner. Data was taken using a temperature controlled probe station utilizing 150 µm pitch GSG probes. The interface between the probes and integrated circuit was made with a coplanar to microstrip ceramic test interface. The test interface was wire bonded to the die using 1 mil diameter bondwires. The spacing between the test interface and the die was 200 µm, and the bond wire loop height was 100 µm. The calibration of the test fixture included the probes and test interfaces, so that the measurement reference plane was at the point of bond wire attachment to the ceramic interface. The presented data therefore represents the chip plus wirebonds.

SDA-6000 Product Image