L6986H

Datasheet

38 V, 2 A synchronous step-down switching regulator with 30 µA quiescent current

HTSSOP16 (R_{th}=40 °C/W)

Product status link
L6986H

Features

- 2 A DC output current
- 4 V to 38 V operating input voltage
- Low consumption mode or low noise mode
- 30 µA I_Q at light-load (LCM V_{OUT} = 3.3 V)
- 8 µA $I_{Q\text{-}SHTDWN}$
- Adjustable f_{SW} (250 kHz - 2 MHz)
- Fixed output voltage (3.3 V and 5 V) or adjustable from 0.85 V to V_{IN}
- Embedded output voltage supervisor
- Synchronization
- Adjustable soft-start time
- Internal current limiting
- Overvoltage protection
- Output voltage sequencing
- Peak current mode architecture
- $R_{DS(on)\ HS}$ = 180 mΩ, $R_{DS(on)\ LS}$ = 150 mΩ
- Thermal shutdown

Applications

- Designed for 12 V and 24 V buses
- Programmable logic controllers (PLCs)
- Decentralized intelligent nodes
- Sensors and low noise applications (LNM)

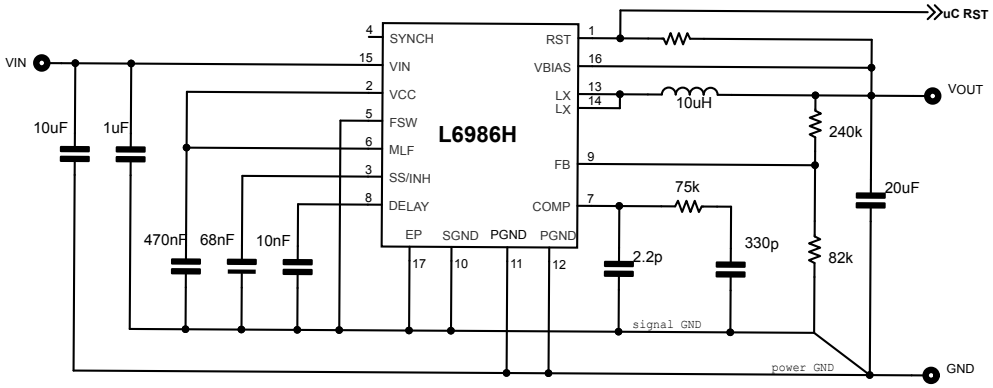
Description

The L6986H is a step-down monolithic switching regulator able to deliver up to 2 A DC. The output voltage adjustability ranges from 0.85 V to VIN. Thanks to the P-channel MOSFET high-side power element, the device features 100% duty cycle operation. The wide input voltage range meets the specification for the 5 V, 12 V and 24 V power supplies.

The “low consumption mode” (LCM) is designed for applications active during idle mode, so it maximizes the efficiency at light-load with controlled output voltage ripple. The “low noise mode” (LNM) makes the switching frequency constant and minimizes the output voltage ripple overload current range, meeting the low noise application specifications. The output voltage supervisor manages the reset phase for any digital load (µC, FPGA). The RST open collector output can also implement output voltage sequencing during the power-up phase. The synchronous rectification, designed for high efficiency at medium - heavy load, and the high switching frequency capability make the size of the application compact. Pulse by pulse current sensing on both power elements implements an effective constant current protection.

1 Application schematic

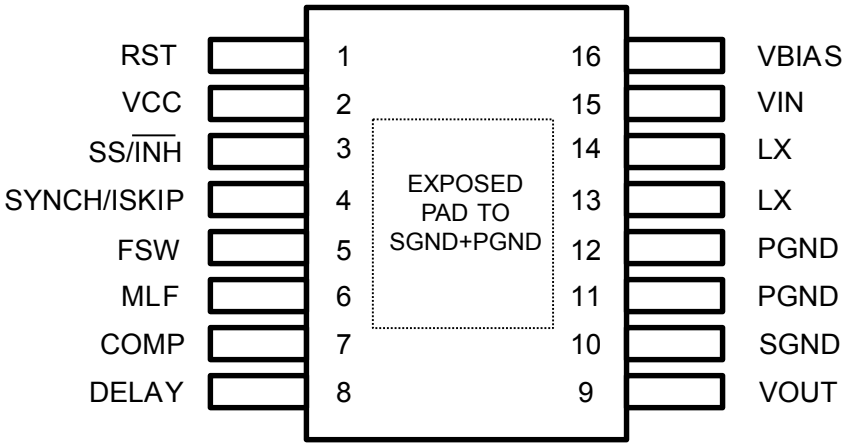
Figure 1. **Application schematic**



2 Pin settings

2.1 Pin connection

Figure 2. **Pin connection (top view)**



2.2 Pin description

Table 1. **Pin description**

Number	Pin	Description
1	RST	The RST open collector output is driven low when the output voltage is out of regulation. The RST is released after an adjustable time DELAY once the output voltage is over the active delay threshold.
2	VCC	Connect a ceramic capacitor (≥ 470 nF) to filter internal voltage reference. This pin supplies the embedded analog circuitry.
3	SS/$\overline{\text{INH}}$	An open collector stage can disable the device clamping this pin to GND ($\overline{\text{INH}}$ mode). An internal current generator (4 µA typ.) charges the external capacitor to implement the soft-start.
4	SYNCH/ ISKP	The pin features master / slave synchronization in LNM (see Low noise mode (LNM)) and skip current level selection in LCM (see Low consumption mode (LCM)). In LNM, leave this pin floating when it is not used.
5	FSW	A pull-up resistor (E24 series only) to VCC or pull down to GND selects the switching frequency. Pin strapping is active only before the soft-start phase to minimize the IC consumption.
6	MLF	A pull-up resistor (E24 series only) to VCC or pull-down to GND selects the low consumption mode/low noise mode and the active RST threshold. Pin strapping is active only before the soft-start phase to minimize the IC consumption.
7	COMP	Output of the error amplifier. The designed compensation network is connected at this pin.
8	DELAY	An external capacitor connected to this pin sets the time DELAY to assert the rising edge of the RST o.c. after the output voltage is over the reset threshold. If this pin is left floating, RST is like a Power Good.
9	VOUT	Output voltage sensing

Number	Pin	Description
10	SGND	Signal GND
11	PGND	Power GND
12	PGND	Power GND
13	LX	Switching node
14	LX	Switching node
15	VIN	DC input voltage
16	VBIAS	Typically connected to the regulated output voltage. An external voltage reference can be used to supply part of the analog circuitry to increase the efficiency at light-load. Connect to GND if not used.
-	Exposed pad	Exposed pad must be connected to SGND, PGND

2.3 Maximum ratings

Stressing the device above the rating listed in Table 2. Absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 2. Absolute maximum ratings

Symbol	Description	Min.	Max.	Unit
V_{IN}	See Table 1	-0.3	40	V
DELAY		-0.3	VCC+ 0.3	V
PGND		SGND - 0.3	SGND + 0.3	V
SGND		-	-	V
V_{CC}		-0.3	(VIN+ 0.3) or (max. 4)	V
SS /$\overline{INH}$		-0.3	VIN+ 0.3	V
MLF		-0.3	VCC+ 0.3	V
COMP		-0.3	VCC+ 0.3	V
VOUT		-0.3	10	V
FSW		-0.3	VCC+ 0.3	V
SYNCH		-0.3	VIN+ 0.3	V
V_{BIAS}		-0.3	(VIN+ 0.3) or (max. 6)	V
RST		-0.3	VIN+ 0.3	V
LX		-0.3	VIN+ 0.3	V
T_J	Operating temperature range	-40	150	°C
T_{STG}	Storage temperature range	-	-65 to 150	°C
T_{LEAD}	Lead temperature (soldering 10 s.)	-	260	°C
I_{HS}, I_{LS}	High-side / low-side switch current	-	2	A

2.4 Thermal data

Table 3. **Thermal data**

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction ambient (device soldered on the STMicroelectronics demonstration board)	40	°C/W
R_{thJC}	Thermal resistance junction to exposed pad for board design (not suggested to estimate T_J from power losses)	5	°C/W

2.5 ESD protection

Table 4. **ESD protection**

Symbol	Test conditions	Value	Unit
ESD	HBM	2	kV
	CDM	500	V

3 Electrical characteristics

T_J =25 °C, V_{IN} = 12 V unless otherwise specified.

Table 5. Electrical characteristics

Symbol	Parameter	Test conditions	Note	Min.	Typ.	Max.	Unit
V_{IN}	Operating input voltage range	-	-	4	-	38	V
V_{IN_H}	V_{CC} UVLO rising threshold	-	-	2.7	-	3.5	
V_{IN_L}	V_{CC} UVLO falling threshold	-	-	2.4	-	3.5	
I_{PK}	Peak current limit	Duty cycle < 20%	-	2.55	-	-	A
		Duty cycle = 100% closed loop operation	-	2.1	-	-	
I_{VY}	Valley current limit	-	-	2.7	-	-	
I_{SKIPH}	Programmable skip current limit	LCM, V_{SYNCH} = GND	(1)		0.6	0.8	
I_{SKIPL}		LCM, V_{SYNCH} = VCC	(2)	-	0.2	-	-
I_{VY_SNK}	Reverse current limit	LNM or V_{OUT} overvoltage	-	0.8	1	2	-
$R_{DS(on)\ HS}$	High-side RDSON	I_{SW}=1 A	-	-	0.18	0.36	Ω
$R_{DS(on)\ LS}$	Low-side RDSON	I_{SW}=1 A	-	-	0.15	0.30	
f_{SW}	Selected switching frequency	FSW pinstrapping before SS	-	See Table 6. f_{SW} selection			
I_{FSW}	FSW biasing current	SS ended	-	-	0	500	nA
LCM/LNM	Low noise mode /low consumption mode selection	MLF pinstrapping before SS	-	See Table 7. LNM/ LCM selection (L6986H3V3), Table 8. LNM/ LCM selection (L6986H5V) and Table 9. LNM/ LCM selection (L6986H)			
I_{MLF}	MLF biasing current	SS ended	-	-	0	500	nA
D	Duty cycle	-	(2)	0	-	100	%
$T_{ON\ MIN}$	Minimum on-time	-	-	-	80	-	ns
VCC regulator							
VCC	LDO output voltage	V_{BIAS} = GND (no switchover)	-	2.9	3.3	3.6	V
		V_{BIAS} = 5 V (switchover)	-	2.9	3.3	3.6	
SWO	V_{BIAS} threshold ($3\ V < V_{BIAS} < 5.5\ V$)	Switch internal supply from V_{IN} to V_{BIAS}	-	2.85	-	3.2	
		Switch internal supply from V_{BIAS} to V_{IN}	-	2.78	-	3.15	
Power consumption							
I_{SHTDWN}	Shutdown current from V_{IN}	VSS/INH =GND	-	4	8	15	µA

Symbol	Parameter	Test conditions	Note	Min.	Typ.	Max.	Unit
$I_{Q\ OPVIN}$	Quiescent current from V_{IN}	**LCM -SWO** $V_{REF}< V_{FB}< V_{OVP}$(SLEEP) V_{BIAS} = 3.3 V	(3)	4	10	15	µA
		LCM -NO SWO VREF< VFB< VOVP(SLEEP) VBIAS = GND	(3)	35	70	120	
		LNM -SWO V_{FB}= GND (NO SLEEP) V_{BIAS} = 3.3 V	-	0.5	1.5	5	mA
		LNM -NO SWO V_{FB}= GND (NO SLEEP) V_{BIAS} = GND	-	2	2.8	6	
$I_{Q\ OPVBIAS}$	Quiescent current from V_{BIAS}	**LCM -SWO** $V_{REF}< V_{FB}< V_{OVP}$(SLEEP) V_{BIAS} = 3.3 V	(3)	25	50	115	µA
		LNM -SWO V_{FB}= GND (NO SLEEP) V_{BIAS} = 3.3 V	-	0.5	1.2	5	mA
Soft-start							
V_{INH}	VSS threshold	SS rising	-	200	460	700	mV
$V_{INH\ HYST}$	VSS hysteresis	-	-	-	100	140	
$I_{SS\ CH}$	C_{SS} charging current	$V_{SS}<V_{INH}$ OR t< $T_{SS\ SETUP}$ OR $V_{EA}+>V_{FB}$	(2)	-	1	-	µA
		t> $T_{SS\ SETUP}$ AND $V_{EA}+<V_{FB}$	(2)	-	4	-	
$V_{SS\ START}$	Start of internal error amplifier ramp	-	-	0.995	1.1	1.150	V
SS_{GAIN}	SS/INH to internal error amplifier gain	-	-	-	3	-	-
Error amplifier							
V_{OUT}	Voltage feedback	3.3 V(L6986H3V3)	-	3.25	3.3	3.35	V
		5 V(L6986H5V)	-	4.925	5.0	5.075	
		L6986H	-	0.841	0.85	0.859	
I_{VOUT}	VOUT biasing current	3.3 V(L6986H3V3)	-	4	6	8.5	µA
		5 V(L6986H5V)	-	7.5	10	13.5	
		L6986H	-	-	50	500	nA
A_V	Error amplifier gain	-	(2)	-	100	-	dB
I_{COMP}	EA output current capability	-	-	±6	±12	±25	µA
Inner current loop							
g_{CS}	Current sense transconductance (V_{COMP} to inductor current gain)	I_{pk} = 1 A	(2)	-	2.5	-	A/V

Symbol	Parameter	Test conditions	Note	Min.	Typ.	Max.	Unit
V_{PP}*g_{CS}	Slope compensation	-	(4)	0.45	0.75	1	A
Overvoltage protection							
V_{OVP}	Overvoltage trip (V_{OVP}/V_{REF})	-	-	1.15	1.2	1.25	-
$V_{OVP\ HYST}$	Overvoltage hysteresis	-	-	0.5	2	5	%
Synchronization (fanout: 6 slave devices typ.)							
f_{SYNCH}	Synchronization frequency	LNM; FSW=VCC	-	275		1400 (2)	kHz
		LNM; FSW=GND		475		2200 (2)	
$V_{SYN\ TH}$	SYNCH input threshold	LNM,SYNCH rising	-	0.70	-	1.2	V
I_{SYN}	SYNCH pull-down current	LNM, V_{SYN}=1.2 V	-		0.7	-	mA
$V_{SYN\ OUT}$	High level output	LNM,5 mA sinking load	-	1.40	-	-	V
	Low level output	LNM,0.7 mA sourcing load	-	-	-	0.6	
Reset							
V_{THR}	Selected RST threshold	MLF pinstrapping before SS	-	See Table 7. LNM/ LCM selection (L6986H3V3), Table 8. LNM/ LCM selection (L6986H5V) and Table 9. LNM/ LCM selection (L6986H)			
$V_{THR\ HYST}$	RST hysteresis	-	(2)	-	2	-	%
V_{RST}	RST open collector output	V_{IN}>V_{INH} AND V_{FB}< V_{TH}4 mA sinking load	-	-	-	0.4	V
		2 <V_{IN}< V_{INH} 4 mA sinking load	-	-	-	0.8	
Delay							
V_{THD}	RST open collector released as soon as V_{DELAY} > V_{THD}	V_{FB}> V_{THR}	-	1.19	1.234	1.258	V
$I_{D\ CH}$	C_{DELAY} charging current	V_{FB}> V_{THR}	-	1	2	3	µA
Thermal shutdown							
T_{SHDWN}	Thermal shutdown temperature	-	(2)	-	165	-	°C
T_{HYS}	Thermal shutdown hysteresis	-	(2)	-	30	-	

1. *Parameter tested in static condition during testing phase. Parameter value may change over dynamic application conditions.*
2. *Not tested in production.*
3. *LCM enables SLEEP mode at light-load.*
4. *Measured at f_{sw}=250 kHz*

T_J = 25 °C, V_{IN}= 12 V unless otherwise specified.

Table 6. f_{SW} selection

Symbol	R_{VCC} (E24 series)	R_{GND} (E24 series)	T_j	f_{SW} min.	f_{SW} typ.	f_{SW} max.	Unit
f_{SW}	0 Ω	NC	(1)	225	**250**	275	kHz
	1.8 Ω	NC	(1)(2)	-	**285**	-	
	3.3 kΩ	NC		-	**330**	-	
	5.6 kΩ	NC		-	**380**	-	
	10 kΩ	NC		-	**435**	-	
	NC	0 Ω	(3)	450	**500**	550	
	18 kΩ	NC	(1) (3)	-	**575**	-	
	33 kΩ	NC		-	**660**	-	
	56 kΩ	NC		-	**755**	-	
	NC	1.8 kΩ		-	**870**	-	
	NC	3.3 kΩ	(3)	900	**1000**	1100	
	NC	5.6 kΩ	(2) (3)	-	**1150**	-	
	NC	10 kΩ		-	**1310**	-	
	NC	18 kΩ		-	**1500**	-	
	NC	33 kΩ	(3)	1575	**1750**	1925	
	NC	56 kΩ	(3)	1800	**2000**	2200	

1. *Synchronization as slave in LNM between 275 kHz and 1400 kHz.*
2. *Not tested in production*
3. *Synchronization as slave in LNM between 475 kHz and 2200 kHz*

T_J = 25 °C, V_{IN} = 12 V unless otherwise specified.

Table 7. LNM/ LCM selection (L6986H3V3)

Symbol	R_{VCC}(E24 1%)	R_{GND}(E24 1%)	Operating mode	V_{RST}/V_{OUT} (tgt. value)	V_{RST} min.	V_{RST} typ.	V_{RST} max.	Unit
V_{RST}	0 Ω	NC	**LCM**	**93%**	3.008	3.069	3.130	V
	8.2 kΩ	NC		**80%**	2.587	**2.640**	2.693	
	18 kΩ	NC		**87%**	2.814	**2.871**	2.928	
	39 kΩ	NC		**96%**	3.105	**3.168**	3.231	
	NC	0 Ω	**LNM**	**93%**	3.008	3.069	3.130	
	NC	8.2 kΩ		**80%**	2.587	**2.640**	2.693	
	NC	18 kΩ		**87%**	2.814	**2.871**	2.928	
	NC	39 kΩ		**96%**	3.105	**3.168**	3.231	

T_J = 25 °C, V_{IN} = 12 V unless otherwise specified.

Table 8. LNM/ LCM selection (L6986H5V)

Symbol	R_{VCC}(E24 1%)	R_{GND}(E24 1%)	Operating mode	V_{RST}/V_{OUT} (tgt. value)	V_{RST} min.	V_{RST}typ.	V_{RST}max.	Unit
V_{RST}	0 Ω	NC	**LCM**	**93%**	4.557	**4.650**	4743	V
	8.2 kΩ	NC		**80%**	3920	**4000**	4080	
	18 kΩ	NC		**87%**	4263	**4350**	4437	
	39 kΩ	NC		**96%**	4704	**4800**	4896	
	NC	0 Ω	**LNM**	**93%**	4557	**4650**	4743	
	NC	8.2 kΩ		**80%**	3920	**4000**	4080	
	NC	18 kΩ		**87%**	4263	**4350**	4437	
	NC	39 kΩ		**96%**	4704	**4800**	4896	

T_J = 25 °C, V_{IN} = 12 V unless otherwise specified.

Table 9. LNM/ LCM selection (L6986H)

Symbol	R_{VCC}(E24 1%)	R_{GND}(E24 1%)	Operating mode	V_{RST}/V_{OUT} (tgt. value)	V_{RST} min.	V_{RST}typ.	V_{RST}max.	Unit
V_{RST}	0 Ω	NC	**LCM**	**93%**	0.779	**0.791**	0.802	V
	8.2 kΩ ±1%	NC		**80%**	0.670	**0.680**	0.690	
	18 kΩ ±1%	NC		**87%**	0.728	**0.740**	0.751	
	39 kΩ ±1%	NC		**96%**	0.804	**0.816**	0.828	
	NC	0 Ω	**LNM**	**93%**	0.779	**0.791**	0.802	
	NC	8.2 kΩ ±1%		**80%**	0.670	**0.680**	0.690	
	NC	18 kΩ ±1%		**87%**	0.728	**0.740**	0.751	
	NC	39 kΩ ±1%		**96%**	0.804	**0.816**	0.828	

4 Functional description

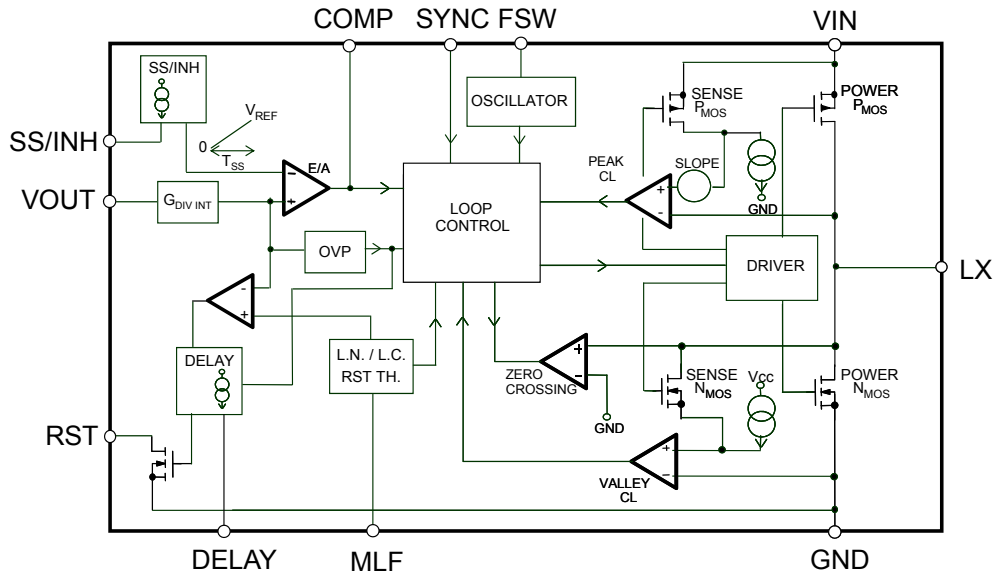
The L6986H device is based on a “peak current mode”, constant frequency control. As a consequence, the intersection between the error amplifier output and the sensed inductor current generates the PWM control signal to drive the power switch.

The device features LNM (low noise mode) that is forced PWM control, or LCM (low consumption mode) to increase the efficiency at light-load.

The main internal blocks shown in the block diagram in Figure 3. Internal block diagram are:

- Embedded power elements. Thanks to the P-channel MOSFET as high-side switch the device features low-dropout operation
- A fully integrated sawtooth oscillator with adjustable frequency
- A transconductance error amplifier
- An internal feedback divider $G_{DIV\ INT}$
- The high-side current sense amplifier to sense the inductor current
- A “Pulse Width Modulator” (PWM) comparator and the driving circuitry of the embedded power elements
- The soft-start blocks to ramp the error amplifier reference voltage and so decreases the inrush current at power-up. The SS/$\overline{\text{INH}}$ pin inhibits the device when driven low
- The switchover capability of the internal regulator to supply a portion of the quiescent current when the V_{BIAS} pin is connected to an external output voltage
- The synchronization circuitry to manage master / slave operation and the synchronization to an external clock
- The current limitation circuit to implement the constant current protection, sensing pulse by pulse high-side / low-side switch current. In case of heavy short-circuit the current protection is fold back to decrease the stress of the external components
- A circuit to implement the thermal protection function
- The OVP circuitry to discharge the output capacitor in case of overvoltage event
- MLF pin strapping sets the LNM/LCM mode and the thresholds of the RST comparator
- FSW pinstrapping sets the switching frequency
- The RST open collector output

Figure 3. Internal block diagram



4.1 Power supply and voltage reference

The internal regulator block consists of a start-up circuit, the voltage pre-regulator that provides current to all the blocks and the bandgap voltage reference. The starter supplies the start-up current when the input voltage goes high and the device is enabled (SS/$\overline{INH}$ pin over the inhibits threshold).

The pre-regulator block supplies the bandgap cell and the rest of the circuitry with a regulated voltage that has a very low supply voltage noise sensitivity.

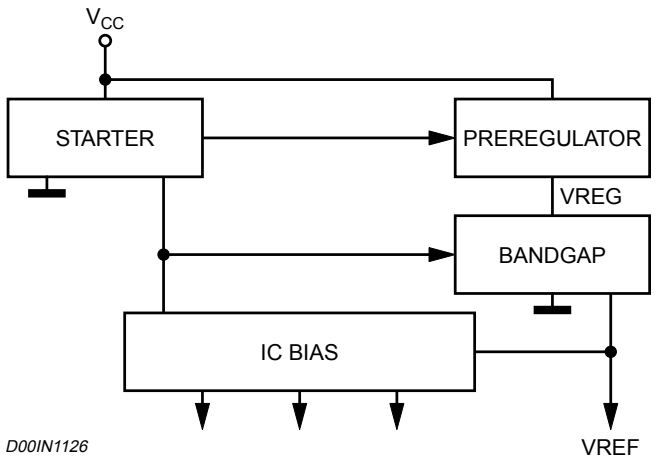
Switchover feature

The switchover scheme of the pre-regulator block features to derive the main contribution of the supply current for the internal circuitry from an external voltage (3 V < V_{BIAS}<5.5 V is typically connected to the regulated output voltage). This helps to decrease the equivalent quiescent current seen at V_{IN}. (Please refer to Switchover feature).

4.2 Voltage monitor

An internal block continuously senses the V_{CC},V_{BIAS} and V_{BG}. If the monitored voltages are good, the regulator starts operating. There is also a hysteresis on the V_{CC} (UVLO).

Figure 4. Internal circuit



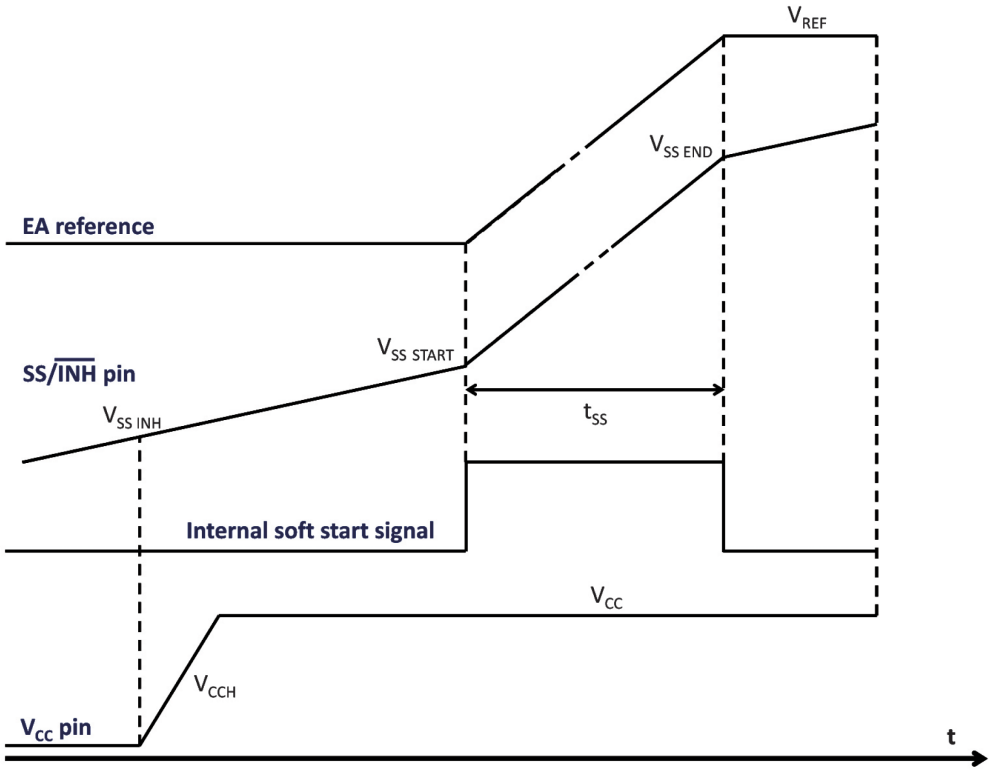
4.3 Soft-start and inhibit

The soft-start and inhibit features are multiplexed on the same pin. An internal current source charges the external soft-start capacitor to implement a voltage ramp on the SS/$\overline{INH}$ pin. The device is inhibited as long as the SS/$\overline{INH}$ pin voltage is lower than the V_{INH} threshold and the soft-start takes place when SS/$\overline{INH}$ pin crosses V_{SS_START}. (See Figure 5. Soft-start phase).

The internal current generator sources 1 mA typ. current when the voltage of the VCC pin crosses the UVLO threshold. The current increases to 4 µA typ. as soon as the SS/$\overline{INH}$ voltage is higher than the V_{INH} threshold. This feature helps to decrease the current consumption in inhibit mode. An external open collector can be used to set the inhibit operation clamping the SS/$\overline{INH}$ voltage below V_{INH} threshold.

The start-up feature minimizes the inrush current and decreases the stress of the power components during the power-up phase. The ramp implemented on the reference of the error amplifier has a gain three times higher (SS_{GAIN}) than the external ramp present at SS/$\overline{INH}$ pin.

Figure 5. **Soft-start phase**

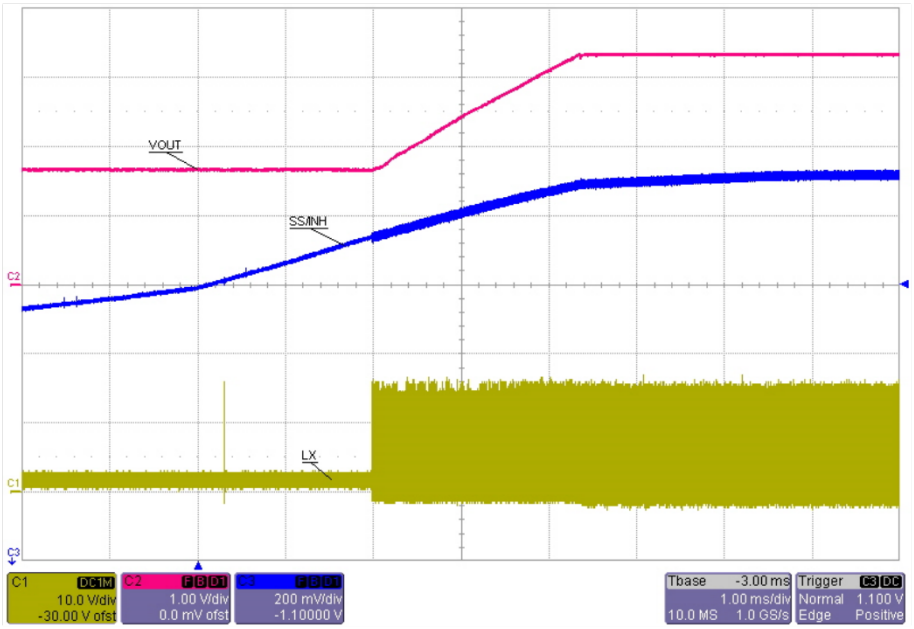


The C_{SS} is dimensioned accordingly with Eq. (1) :

$$C_{SS} = SS_{GAIN} \cdot \frac{I_{SSCH} \cdot T_{SS}}{V_{FB}} = 3 \cdot \frac{4\mu A \cdot T_{SS}}{0.85V} \quad (1)$$

where T_{SS} is the soft-start time, $I_{SS\ CH}$ the charging current and V_{FB} the reference of the error amplifier. The soft-start block supports the precharged output capacitor.

Figure 6. **Soft-start phase with precharged C_{OUT}**



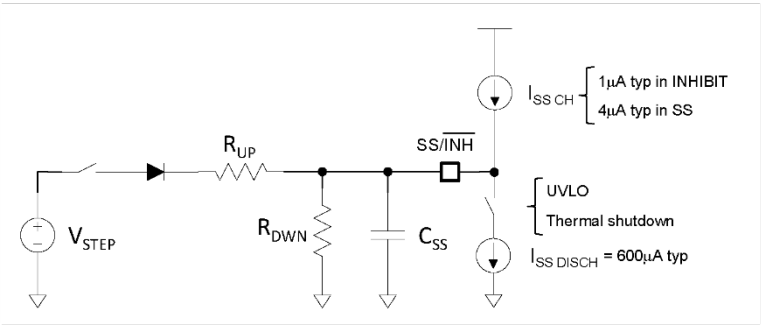
During normal operation a new soft-start cycle takes place in case of:

- Thermal shutdown event
- UVLO event
- The device is driven in $\overline{INH}$ mode

The soft-start capacitor is discharged with a 0.6 mA typ. current capability for 1 ms time max. For complete and proper capacitor discharge in case of fault conditions, a maximum C_{SS} = 67 nF value is suggested.

The application example in Figure 7. Enable the device with external voltage step shows how to enable the L6986H and perform the soft-start phase driven by an external voltage step.

Figure 7. **Enable the device with external voltage step**



The maximum capacitor value has to be limited to guarantee the device can discharge it in case of thermal shutdown and UVLO events (see Figure 9), so restart the switching activity ramping the error amplifier reference voltage

$$C_{SS} < \frac{-1ms}{R_{SS\_EQ} \cdot In(1 - \frac{V_{SS\_FINAL} - 0.9V}{600\mu A - R_{SS\_EQ}})} \quad (2)$$

where:

$$R_{SS\_EQ} = \frac{R_{UP} \cdot R_{DWN}}{R_{UP} + R_{DWN}} \qquad V_{SS\_FINAL} = (V_{STEP} - V_{DIODE}) \cdot \frac{R_{DWN}}{R_{UP} + R_{DWN}} \quad (3)$$

The optional diode prevents the device from disabling if the external source drops to ground.

R_{UP} value is selected in order to make the capacitor charge at first approximation independent from the internal current generator (4 µA typ. current capability, see Table 1), so:

$$\frac{V_{STEP} - V_{DIODE} - V_{SS\_END}}{R_{UP}} \gg I_{SS\_CHARGE} \equiv 4\mu A \quad (4)$$

where

$$V_{SS\_END} = V_{SS\_START} + \frac{V_{FB}}{SS_{GAIN}} \quad (5)$$

represents the SS/$\overline{\text{INH}}$ voltage correspondent to the end of the ramp on the error amplifier (see Figure 5. Soft-start phase); refer to Table 1 for $V_{SS\ START}$, V_{FB} and SS_{GAIN} parameters.

As a consequence the voltage across the soft-start capacitor can be written as:

$$V_{SS}(t) = V_{SS\_FINAL} \cdot \frac{1}{1 - e^{-\frac{t}{C_{SS} \cdot R_{SS\_EQ}}}} \quad (6)$$

R_{SS_DOWN} is selected to guarantee the device stays in inhibit mode when the internal generator sources 1 µA typ. out of the SS/INH pin and V_{STEP} is not present:

$$R_{DWN} \cdot I_{SSINHIBIT} \equiv R_{DWN} \cdot 1\mu A \ll V_{INH} \equiv 200mV \quad (7)$$

so

$$R_{DWN} < 100k\Omega \quad (8)$$

R_{UP} and R_{DWN} are selected to guarantee:

$$V_{SS\_FINAL} \cong 2V > V_{SS\_END} \quad (9)$$

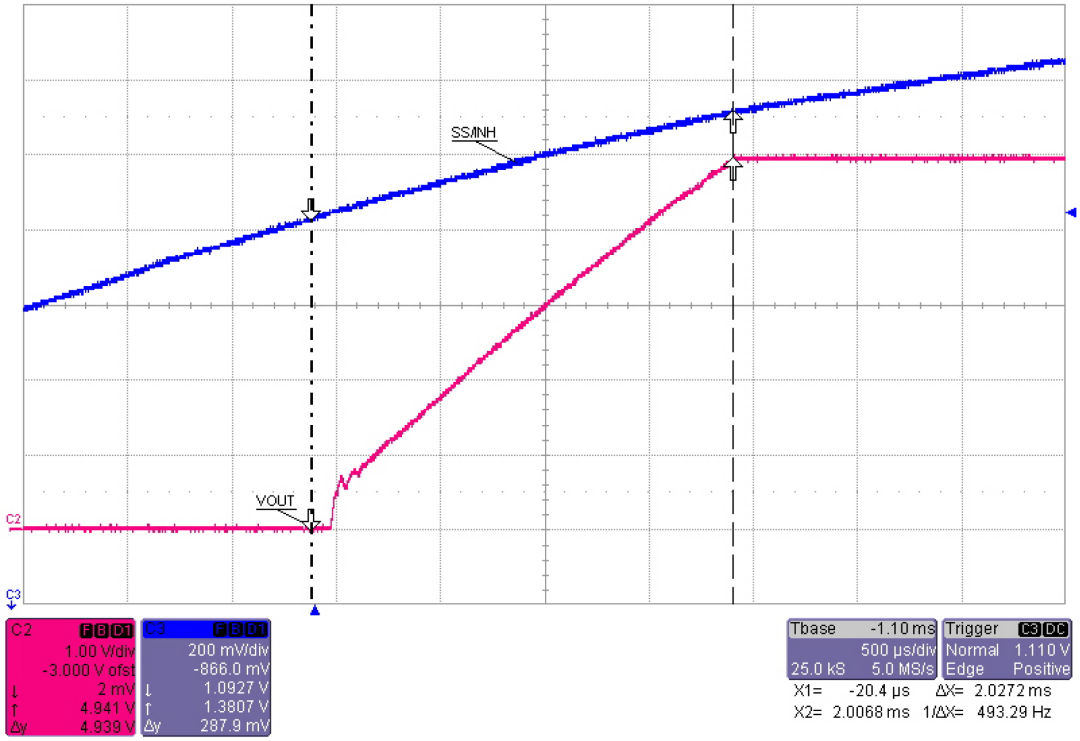
The time to ramp the internal voltage reference can be calculated as follows

$$T_{SS} = C_{SS} \cdot R_{SS\_EQ} \cdot In(\frac{V_{SS\_FINAL} - V_{SS\_START}}{V_{SS\_FINAL} - V_{SS\_END}}) \quad (10)$$

that is the equivalent soft-start time to ramp the output voltage.

Figure 8. External soft-start network V_{STEP} driven shows the soft-start phase with the following component selection: R_{UP} = 180 kΩ, R_{DWN} = 33 kΩ, C_{SS} = 200 nF, the 1N4148 is a small signal diode and V_{STEP} = 13 V.

Figure 8. **External soft-start network V_{STEP} driven**

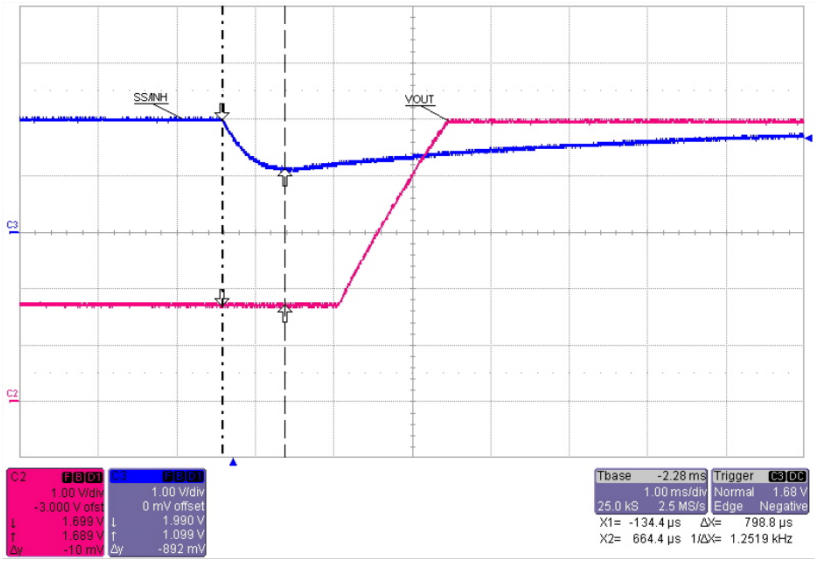


The circuit in Figure 7. Enable the device with external voltage step introduces a time delay between V_{STEP} and the switching activity that can be calculated as:

$$T_{SS} = C_{SS} \cdot R_{SS\_EQ} \cdot In\left(\frac{V_{SS\_FINAL}}{V_{SS\_FINAL} - V_{SS\ \ START}}\right) \quad (11)$$

Figure 9. External soft-start after UVLO or thermal shutdown shows how the device discharges the soft-start capacitor after an UVLO or thermal shutdown event in order to restart the switching activity ramping the error amplifier reference voltage.

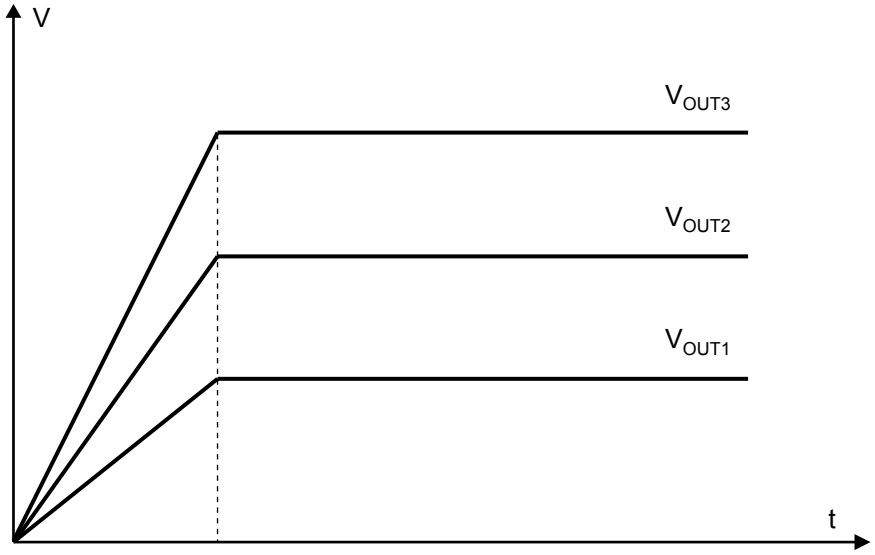
Figure 9. **External soft-start after UVLO or thermal shutdown**



4.3.1 Ratiometric startup

The ratiometric start-up is implemented sharing the same soft-start capacitor for a set of the L6986H devices

Figure 10. Ratiometric startup



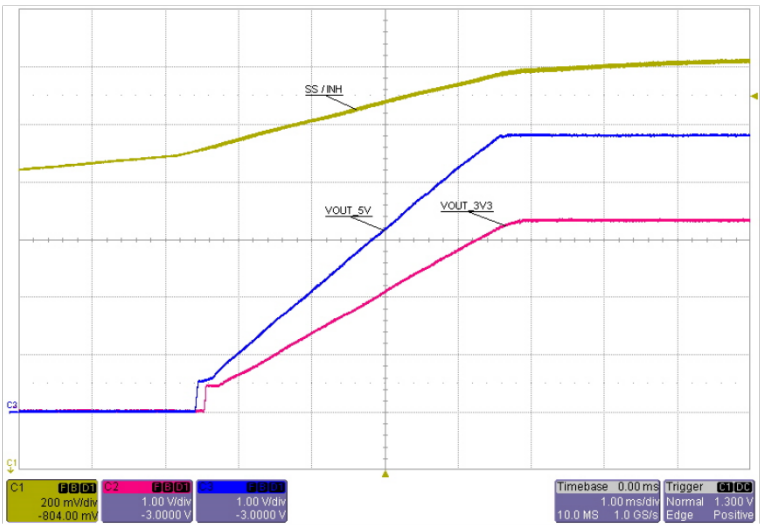
As a consequence all the internal current generators charge in parallel the external capacitor. The capacitor value is dimensioned accordingly, as per equation below:

$$C_{SS} = n_{L6986H} \cdot SS_{GAIN} \cdot \frac{I_{SSCH} \cdot T_{SS}}{V_{FB}} = n_{L6986H} \cdot 3 \cdot \frac{4\mu A \cdot T_{SS}}{0.85V} \quad (12)$$

where n_{L6986H} represents the number of devices connected in parallel.

For better tracking of the different output voltages the synchronization of the set of regulators is suggested.

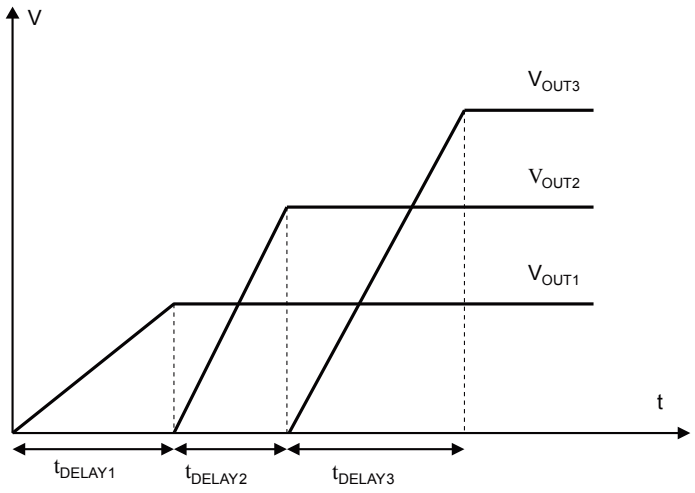
Figure 11. Ratiometric start-up operation



4.3.2 Output voltage sequencing

The L6986H device implements sequencing connecting the RST pin of the master device to the SS/$\overline{INH}$ of the slave. The slave is inhibited as long as the master output voltage is outside regulation so implementing the sequencing, see Figure 12. Output voltage sequencing.

Figure 12. Output voltage sequencing



High flexibility is achieved thanks to the programmable RST thresholds (Table 7. LNM/ LCM selection (L6986H3V3) and Table 8. LNM/ LCM selection (L6986H5V)) and programmable delay time. To minimize the component count the DELAY pin capacitor can be also omitted so the pin works as a normal Power Good.

4.4 Error amplifier

The voltage error amplifier is the core of the loop regulation. It is a transconductance operational amplifier whose non inverting input is connected to the internal voltage reference (0.85 V), while the inverting input (FB) is connected to the external divider or directly to the output voltage.

Table 10. Uncompensated error amplifier characteristics

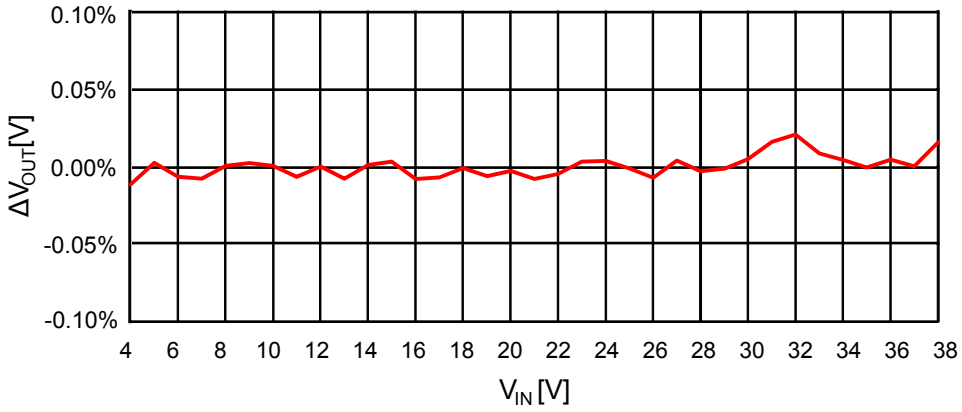
Description	Value
Transconductance	155 µS
Low frequency gain	100 dB

The error amplifier output is compared with the inductor current sense information to perform PWM control. The error amplifier also determines the burst operation at light-load when the LCM is active.

4.5 Output voltage line regulation

The regulator features an enhanced line regulation thanks to the peak current mode architecture. Figure 13. V_{OUT} = 3.3 V line regulation shows negligible output voltage variation (normalized to the value measured at V_{IN} = 12 V) over the entire input voltage range for the L6986H with V_{OUT} = 3.3V.

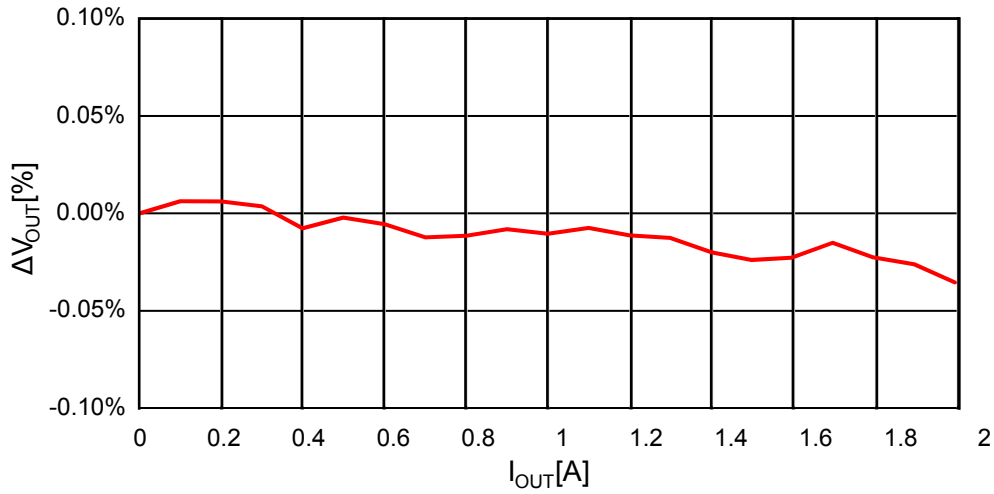
Figure 13. V_{OUT} = 3.3 V line regulation



4.6 Output voltage load regulation

Figure 14. VOUT = 3.3 V load regulation shows negligible output voltage variation (normalized to the value measured at I_{OUT} = 0 A) over the entire output current range for the L6986H with V_{OUT} = 3.3 V, measured on the L6986H evaluation board (see Section 6.7 Application board).

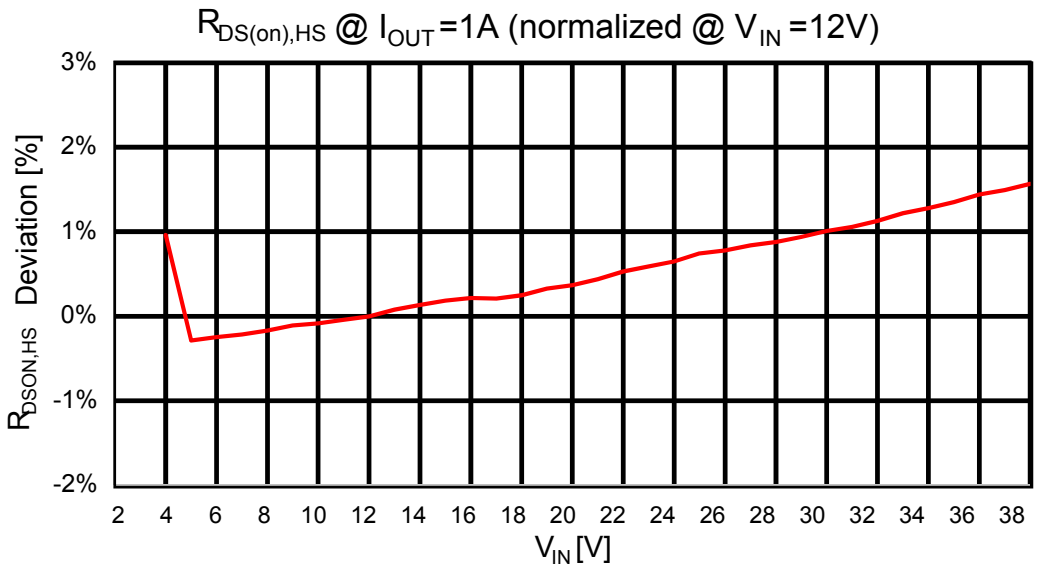
Figure 14. VOUT = 3.3 V load regulation



4.7 High-side switch resistance vs. input voltage

Figure 15. Normalized $R_{DS(on),HS}$ variation shows the high-side switch $R_{DS(on)}$ variation over the entire input voltage operating range normalized at the value measured at V_{IN} = 12 V (see Section 3 Electrical characteristics).

Figure 15. **Normalized $R_{DS(on),HS}$ variation**



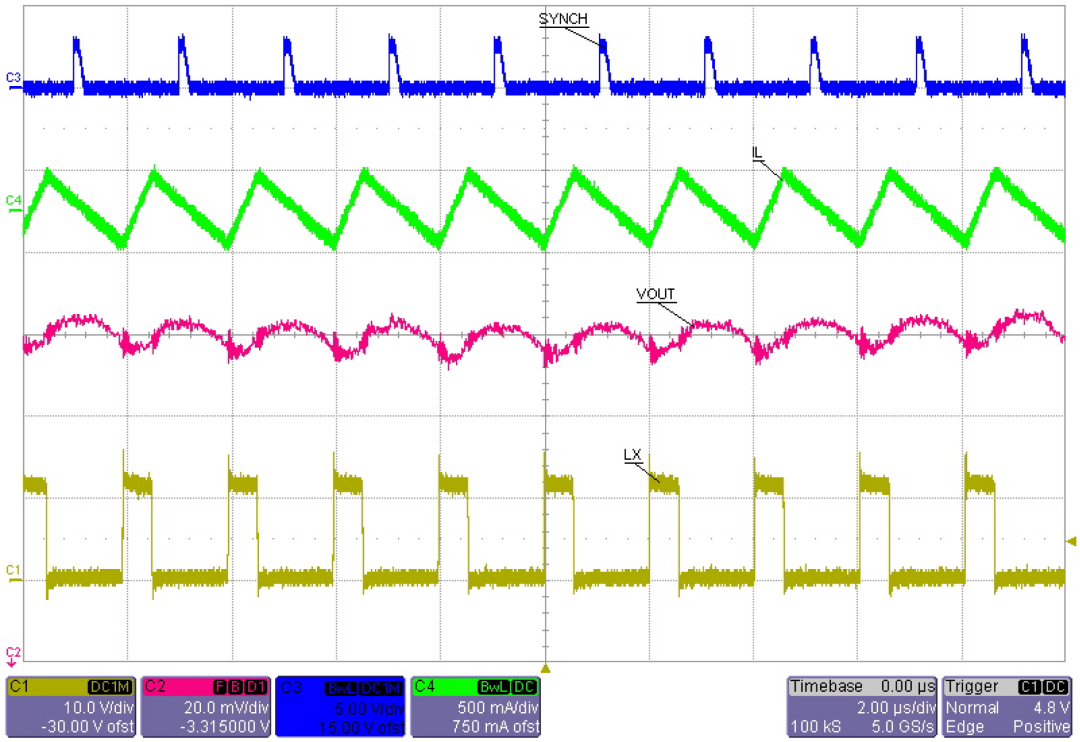
4.8 Light-load operation

The MLF pinstrapping during the power-up phase determines the light-load operation (refer to Table 7. LNM/ LCM selection (L6986H3V3) and Table 8. LNM/ LCM selection (L6986H5V)).

4.8.1 Low noise mode (LNM)

The low noise mode implements a forced PWM operation over the different loading conditions. The LNM features a constant switching frequency to minimize the noise in the final application and a constant voltage ripple at fixed V_{IN}. The regulator in steady loading condition never skips pulses and it operates in continuous conduction mode (CCM) over the different loading conditions, thus making this operation mode ideal for noise sensitive applications.

Figure 16. **Low noise mode operation**



4.8.2 Low consumption mode (LCM)

The low consumption mode maximizes the efficiency at light-load. The regulator prevents the switching activity whenever the switch peak current request is lower than the I_{SKIP} threshold. As a consequence the L6986H device works in bursts and it minimizes the quiescent current request in the meantime between the switching operation. In LCM operation, the pin SYNCH/ISKIP level dynamically defines the I_{SKIP} current threshold (see Table 5. Electrical characteristics) as shown in Table 11. I_{SKIP} programmable current threshold.

Table 11. **I_{SKIP} programmable current threshold**

SYNCH / ISKIP (pin 4)	I_{SKIP} current threshold
Low	$ISKIP_H$ = 0.6 A typical
High	$ISKIP_L$ = 0.2 A typical

The I_{SKIP} programmability helps to optimize the performance in terms of the output voltage ripple or efficiency at the light-load, that are parameters which disagree each other by definition. A lower skip current level minimizes the voltage ripple but increases the switching activity (time between bursts gets closer) since less energy per burst is transferred to the output voltage at the given load. On the other side, a higher skip level reduces the switching activity and improves the efficiency at the light-load but worsen the voltage ripple.

No difference in terms of the voltage ripple and conversion efficiency for the medium and high load current level, that is when the device operates in the discontinuous or continuous mode (DCM vs. CCM).

The L6986H allows changing the skip current threshold level while the device is switching in order to adapt the pulse skipping operation to the loading condition. The time needed to detect and implement this transition is negligible with respect to the switching period.

When the L6986H is configured in the low consumption mode, the SYNCH/ISKIP pin operates as a logic gate input pin with an internal pull-down (4.5 µA typ.) guaranteeing the I_{SKIPH} operation when leaving the pin floating. Table 12. SYNCH/ISKIP pin voltage thresholds and driving current reports the $V_{SYNCH/ISKIP}$ thresholds and the minimum current needed to drive the pin.

Table 12. SYNCH/ISKIP pin voltage thresholds and driving current

Parameter	Value
$V_{SKIP\_TH\_L\_MAX}$	0.65 V
$V_{SKIP\_TH\_H\_MIN}$	1.6 V
$I_{SYNCH/ISKIP\_DRIVING\_MIN}$	± 10 µA

Figure 17. L6986H skip current level transition at I_{LOAD} = 150 mA with L = 10 µH shows a skip current threshold transition at I_{LOAD} = 150 mA measured on the L6986H - V_{OUT} = 3.3 V with fsw = 500 kHz and L = 10 µH:

- When V(SYNCH/ISKIP) < $V_{SKIP\_TH\_L\_MAX}$, the L6986H operates in the pulse skipping mode minimizing current consumption
- When V(SYNCH/ISKIP) > $V_{SKIP\_TH\_H\_MIN}$, the L6986H operates in the continuous conduction mode minimizing the output voltage ripple

Figure 17. L6986H skip current level transition at I_{LOAD} = 150 mA with L = 10 µH

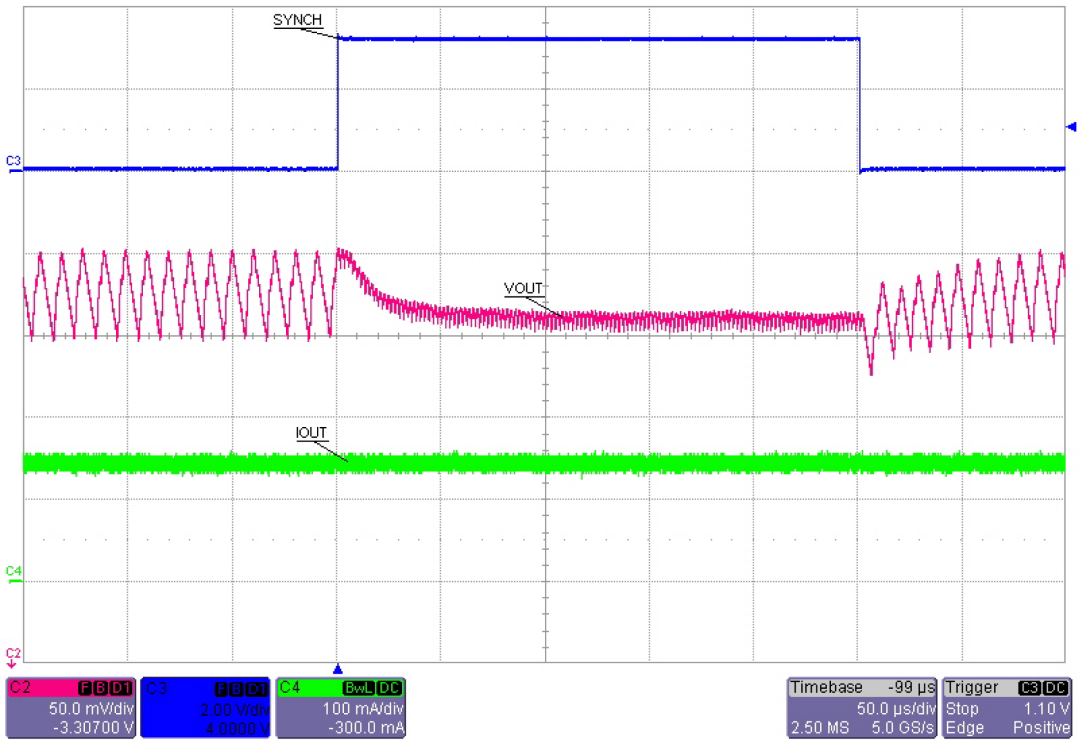


Figure 18. Light-load efficiency comparison at different I_{SKIP} - linear scale and Figure 19. Light-load efficiency comparison at different I_{SKIP} - log scale report the efficiency measurements to highlight the $ISKIP_H$ and $ISKIP_L$ efficiency gap at the light-load also in comparison with the LNM operation. The same efficiency at the medium / high load is confirmed at different ISKIP levels.

Figure 18. Light-load efficiency comparison at different I_{SKIP} - linear scale

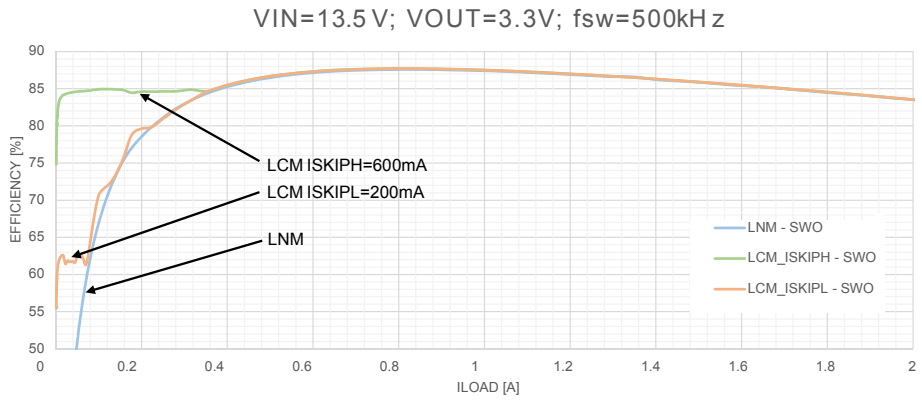


Figure 19. Light-load efficiency comparison at different I_{SKIP} - log scale

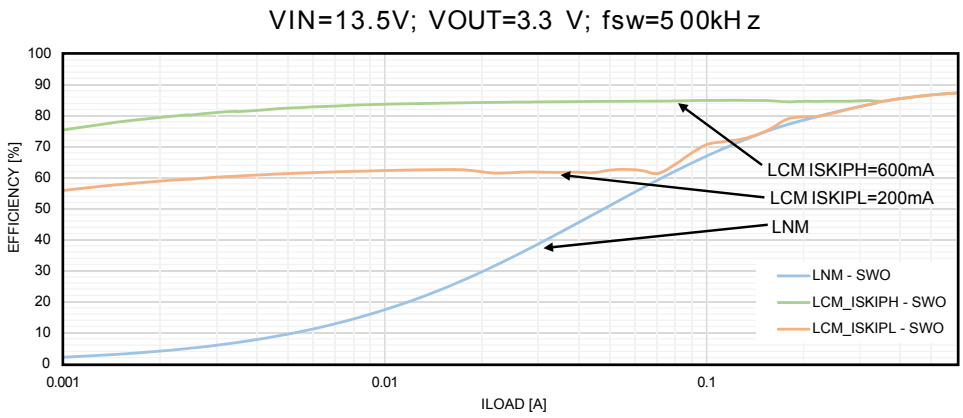


Figure 20. LCM operation with $ISKIP_H$ = 600 mA typ. at zero load and Figure 21. LCM operation with $ISKIP_L$ = 200 mA typ. at zero load show the LCM operation at the different ISKIP level.

Figure 20. LCM operation with $ISKIP_H$ = 600 mA typ. at zero load shows the $ISKIP_H$ = 600 mA typ. and so 50 mV output voltage ripple.

Figure 21. LCM operation with $ISKIP_L$ = 200 mA typ. at zero load shows the $ISKIP_L$ = 200 mA typ. and so less than 20 mV output voltage ripple.

Figure 20. LCM operation with $ISKIP_H$ = 600 mA typ. at zero load

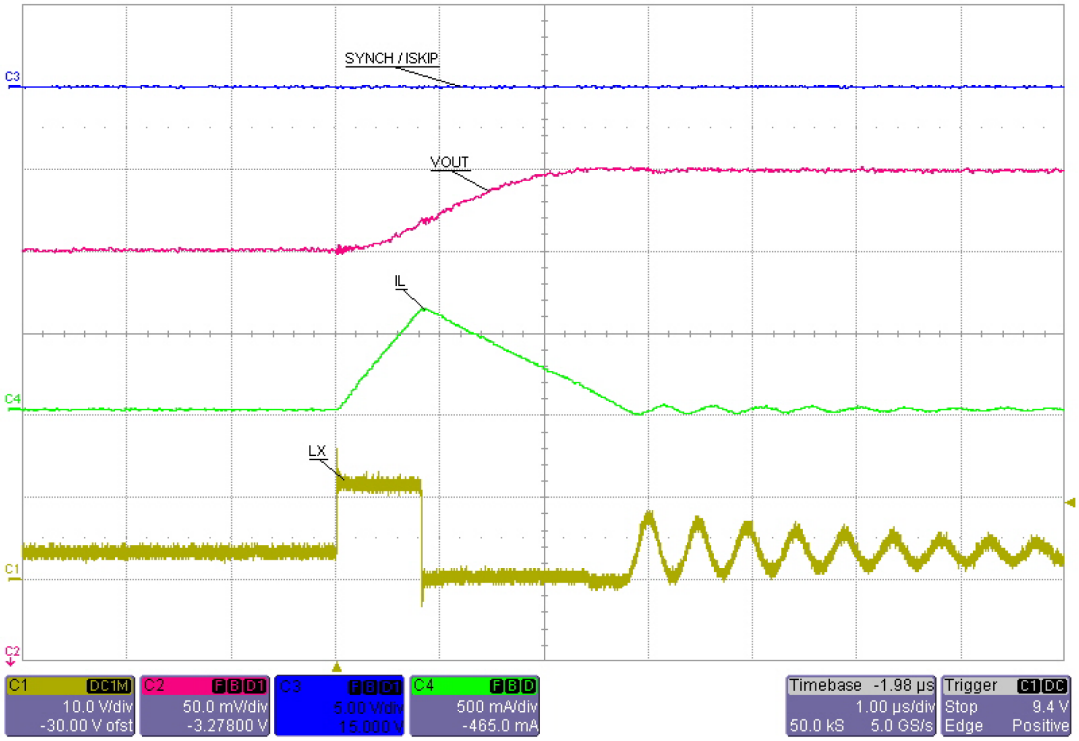
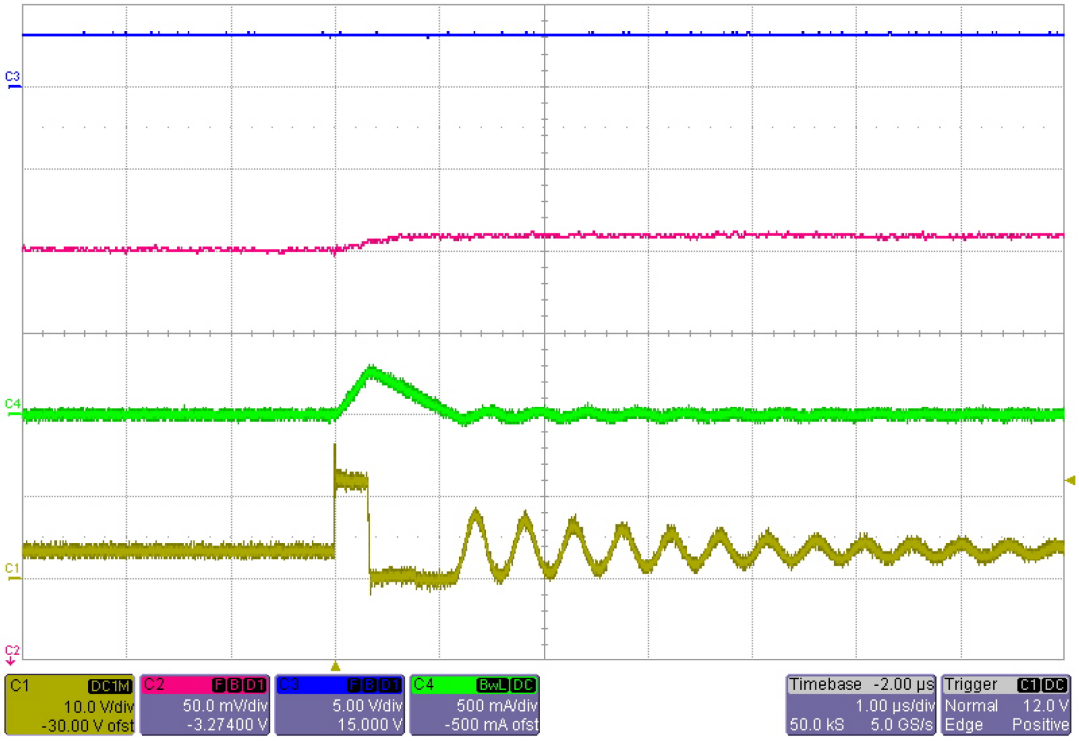


Figure 21. LCM operation with $ISKIP_L$ = 200 mA typ. at zero load



The LCM operation satisfies the high efficiency requirements of the battery powered applications. In order to minimize the regulator quiescent current request from the input voltage, the V_{BIAS} pin can be connected to an external voltage source in the range 3 V < V_{BIAS} < 5.5 V (see Section 4.1 Power supply and voltage reference).

Given the energy stored in the inductor during a burst, the voltage ripple depends on the capacitor value:

$$V_{OUT\ \ RIPPLE} = \frac{\Delta Q_{IL}}{C_{OUT}} = \frac{\int_0^{T_{BURST}} (i_L(t) \cdot dt)}{C_{OUT}} \quad (13)$$

Figure 22. LCM operation over loading condition (part 1)

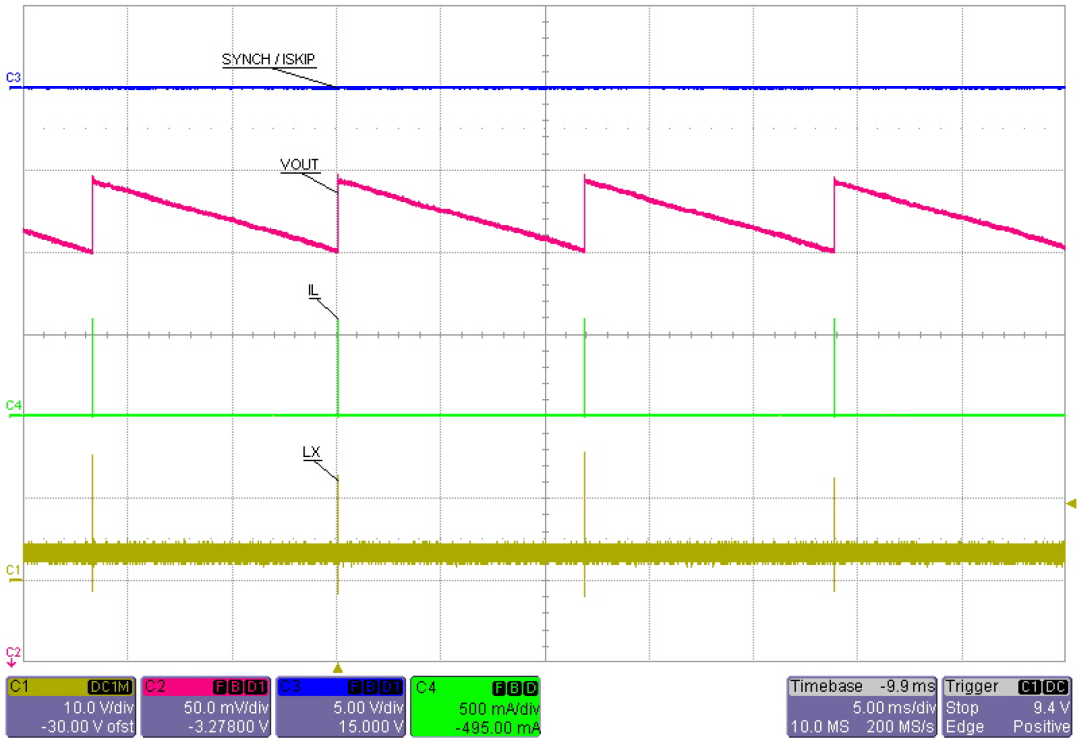


Figure 23. **LCM operation over loading condition (part 2-pulse skipping)**

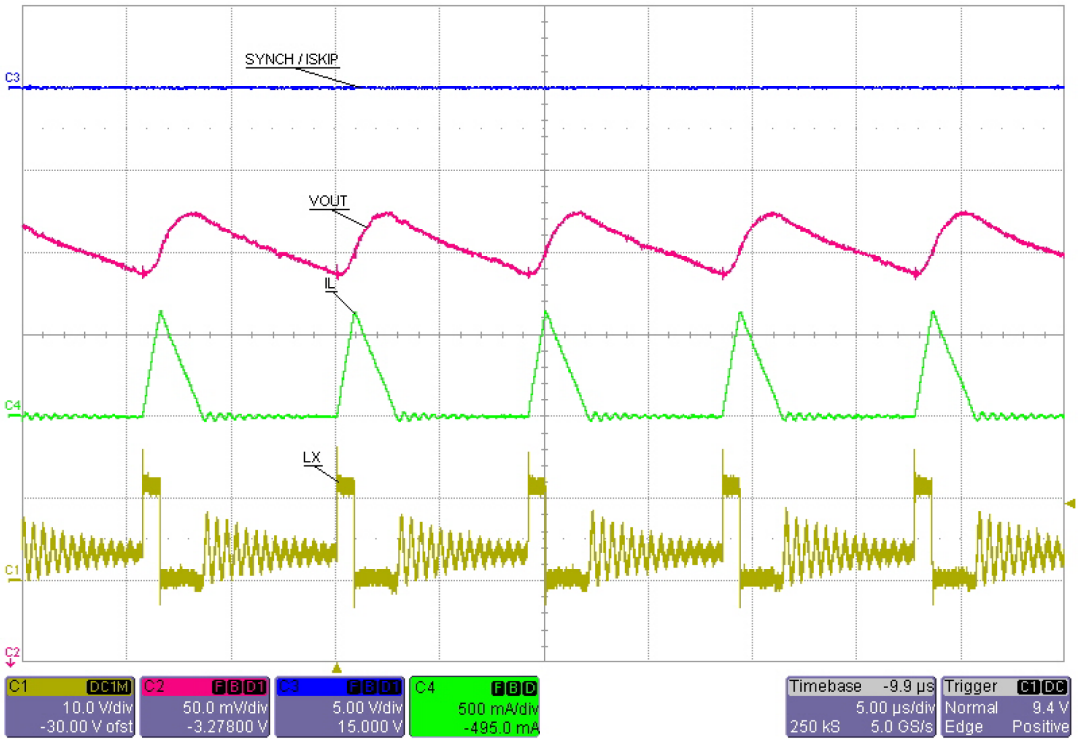


Figure 24. **LCM operation over loading condition (part 3-pulse skipping)**

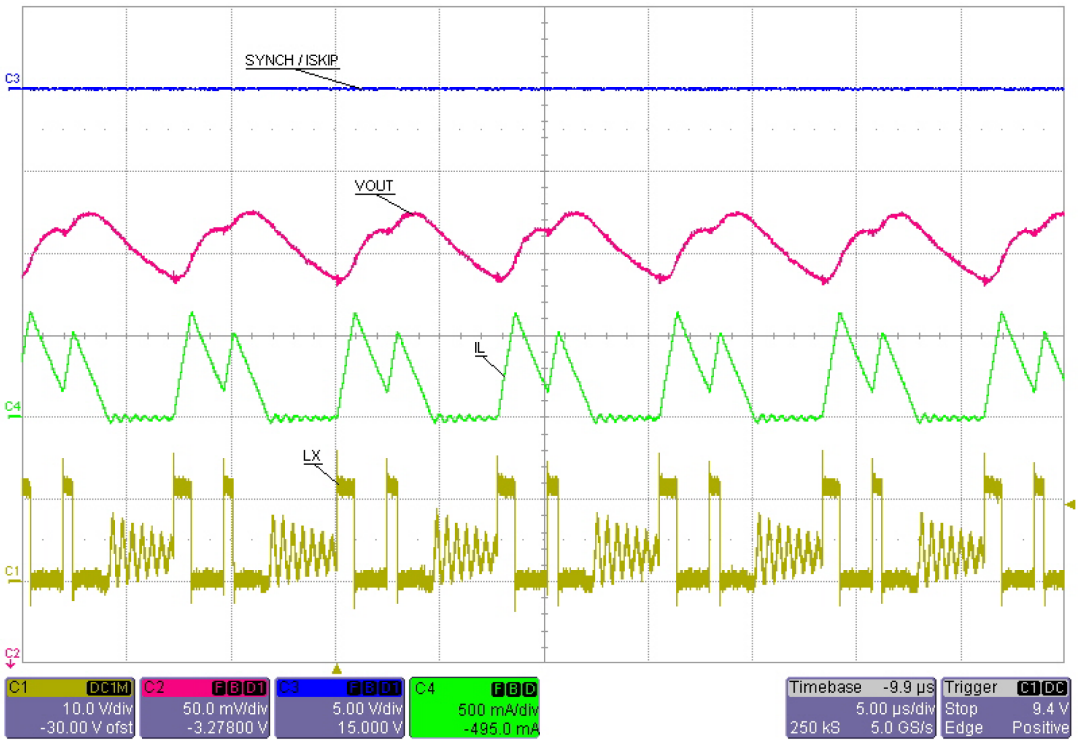
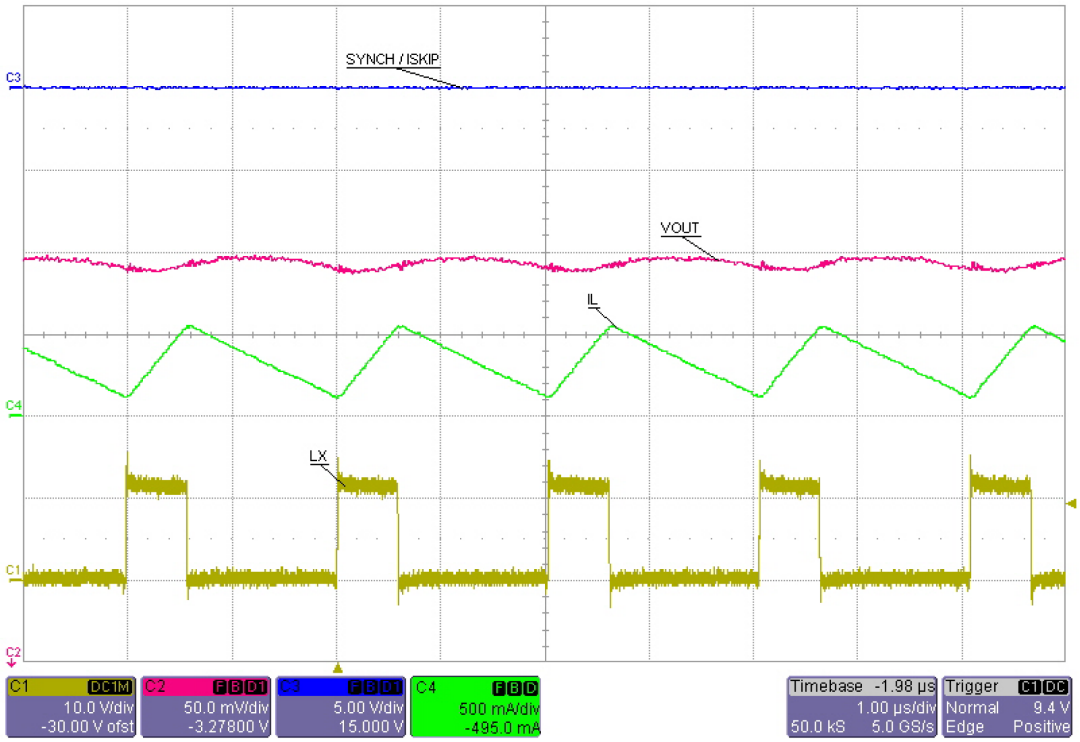


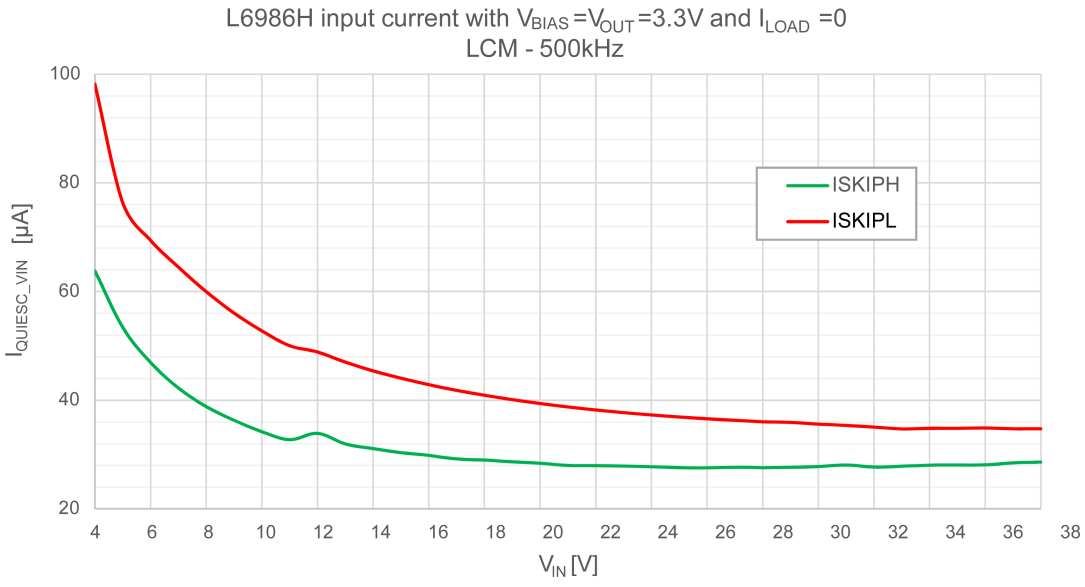
Figure 25. **LCM operation over loading condition (part 4-CCM)**



4.8.3 Quiescent current in LCM with switchover

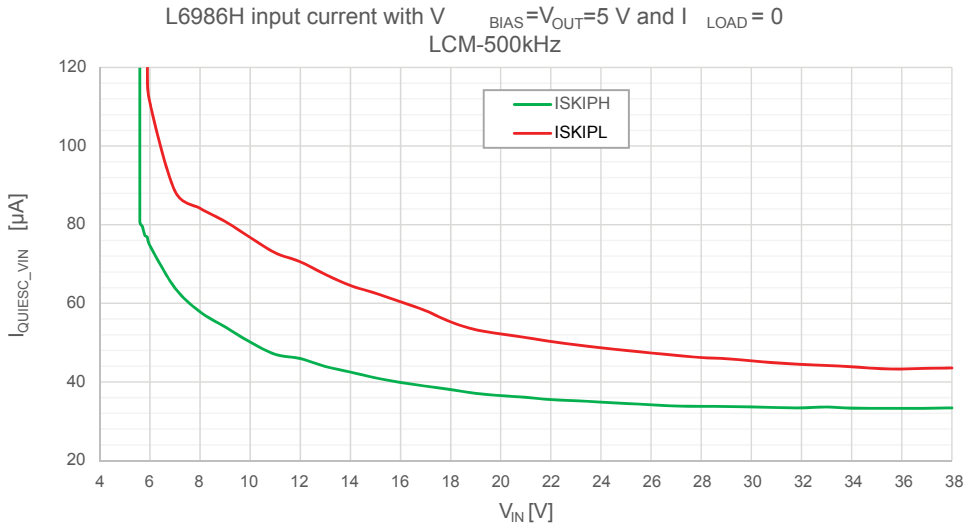
The current absorbed from the input voltage in the low consumption mode while regulating the output voltage at the zero output load depends on the input voltage value and the selected skip current level, as shown in Figure 26. Quiescent current at V_{OUT} = 3.3 V and zero output load and Figure 27. Quiescent current at V_{OUT} = 5 V and zero output load

Figure 26. **Quiescent current at V_{OUT} = 3.3 V and zero output load**



When V_{IN} is adequately higher than V_{OUT} (see Figure 26. Quiescent current at V_{OUT} = 3.3 V and zero output load) the device works in the bursts mode operation, minimizing the power consumption over the entire input voltage (see Section 4.8.2 Low consumption mode (LCM)).

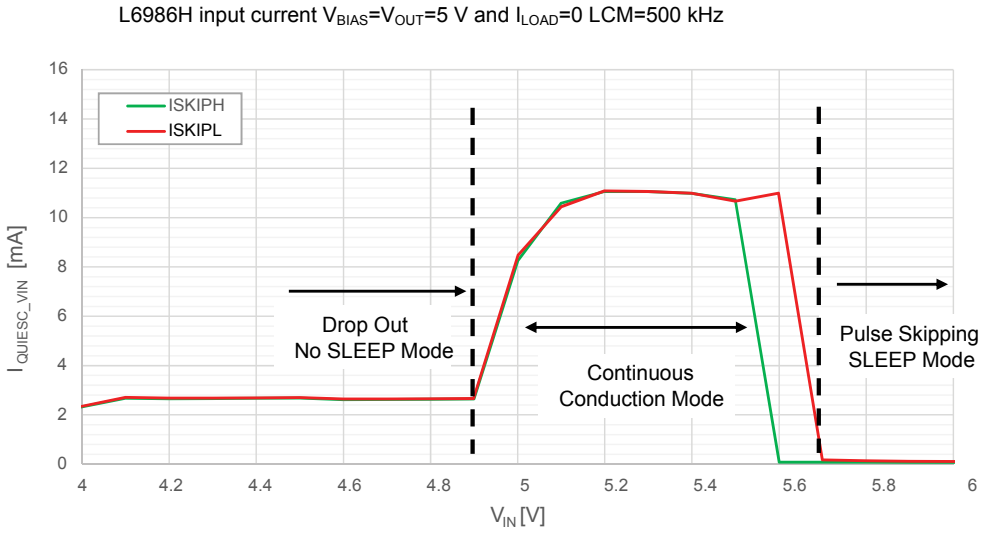
Figure 27. Quiescent current at V_{OUT} = 5 V and zero output load



When V_{IN} approaches V_{OUT} (see Figure 27. Quiescent current at V_{OUT} = 5 V and zero output load and zoomed Figure 28. Quiescent current at V_{IN} while regulating V_{OUT} = 5 V at zero output load) the device increases the switching activity towards the continuous conduction mode operation for the internal slope contribution effect on the programmed skip current threshold. As a consequence the quiescent current increases.

When VIN is lower than VOUT (see Figure 28. Quiescent current at V_{IN} while regulating V_{OUT} = 5 V at zero output load), the device enters in the low-dropout operation with the high-side always switched on. In this operating condition, all the internal circuit blocks are active and the quiescent current corresponds to what measured in the low noise mode operation (see $I_{Q\ OP\ VIN}$ and $I_{Q\ OP\ VBIAS}$ in Table 5. Electrical characteristics given V_{FB} = GND).

Figure 28. Quiescent current at V_{IN} while regulating V_{OUT} = 5 V at zero output load



4.9 Switchover feature

The switchover maximizes the efficiency at the light-load that is crucial for LCM applications.

The switchover operation features to derive the main contribution of the supply current for the internal circuitry from an external voltage (3 V < V_{BIAS} < 5.5 V is typically connected to the regulated output voltage). This helps to decrease the equivalent quiescent current seen at V_{IN}.

In case the regulator output voltage is not compatible with the V_{BIAS} input voltage range, it is possible to use an auxiliary voltage source for the switchover operation. The external auxiliary voltage source must always respect the condition 3 V < V_{AUX} < 5.5 V, and must be derived from the L6986H power supply (VIN - pin 15) for proper power sequencing of the internal circuits.

4.9.1 LCM

The LCM operation satisfies the high efficiency requirements of the battery powered applications.

In case the V_{BIAS} pin is connected to the regulated output voltage (V_{OUT}), the total current drawn from the input voltage can be calculated as:

$$I_{QVIN} = I_{QOPVIN} + \frac{1}{\eta_{L6986H}} \cdot \frac{V_{BIAS}}{V_{IN}} \cdot I_{QOPVBIAS} \quad (14)$$

where $I_{Q\ OP\ VIN}$, $I_{Q\ OP\ VBIAS}$ are defined in Table 5. Electrical characteristics and η_{L6986H} is the efficiency of the conversion in the working point.

4.9.2 LNM

is also valid when the device works in LNM and it can increase the efficiency at the medium load since the regulator always operates in the continuous conduction mode.

4.10 Overcurrent protection

The current protection circuitry features a constant current protection, so the device limits the maximum peak current (see Table 5. Electrical characteristics) in overcurrent condition.

The L6986H device implements a pulse by pulse current sensing on both power elements (high-side and low-side switches) for effective current protection over the duty cycle range. The high-side current sensing is called “peak” the low-side sensing “valley”.

The internal noise generated during the switching activity makes the current sensing circuitry ineffective for a minimum conduction time of the power element. This time is called “masking time” because the information from the analog circuitry is masked by the logic to prevent an erroneous detection of the overcurrent event. As a consequence, the peak current protection is disabled for a masking time after the high-side switch is turned on, the valley for a masking time after the low-side switch is turned on. In other words, the peak current protection can be ineffective at extremely low duty cycles, the valley current protection at extremely high duty cycles.

The L6986H device assures an effective overcurrent protection sensing the current flowing in both power elements. In case one of the two current sensing circuitry is ineffective because of the masking time, the device is protected sensing the current on the opposite switch. Thus, the combination of the “peak” and “valley” current limits assures the effectiveness of the overcurrent protection even in extreme duty cycle conditions.

The valley current threshold is designed higher than the peak to guarantee a proper operation. In case the current diverges because of the high-side masking time, the low-side power element is turned on until the switch current level drops below the valley current sense threshold. The low-side operation is able to prevent the high-side turn on, so the device can skip pulses decreasing the switching frequency.

Figure 29. **Valley current sense operation in overcurrent condition**

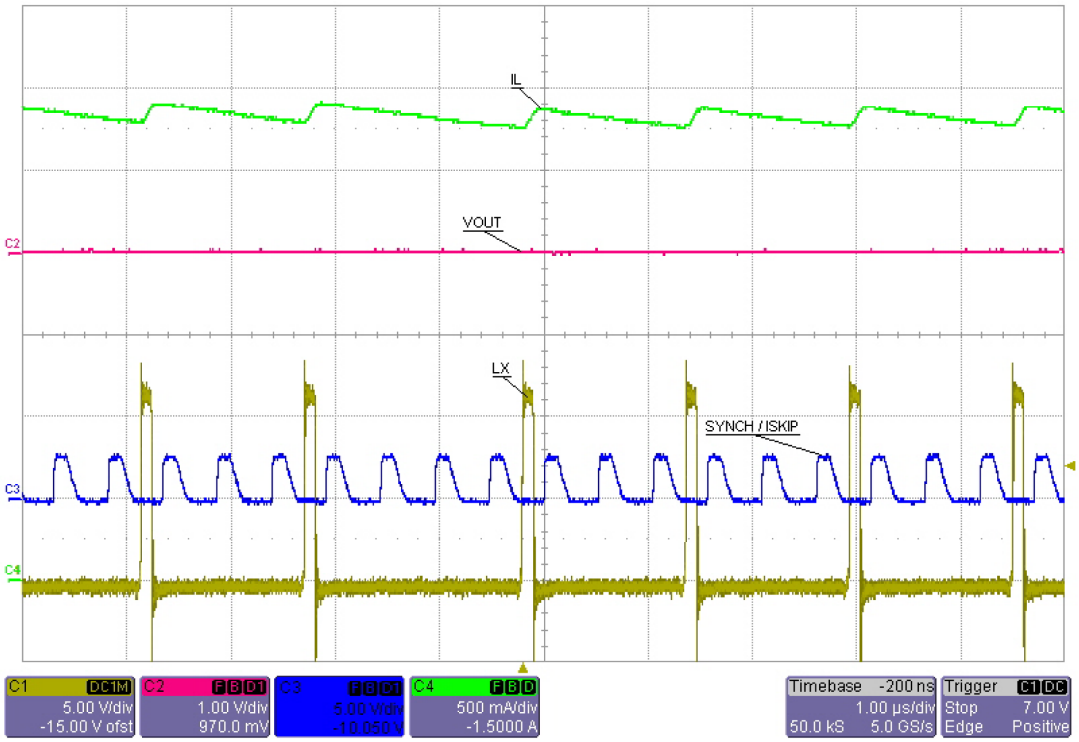


Figure 29. Valley current sense operation in overcurrent condition shows the switching frequency reduction during the valley current sense operation in case of extremely low duty cycle (V_{IN} = 12 V, f_{SW} = 2 MHz short-circuit condition).

In a worst case scenario (like Figure 29. Valley current sense operation in overcurrent condition) of the overcurrent protection the switch current is limited to:

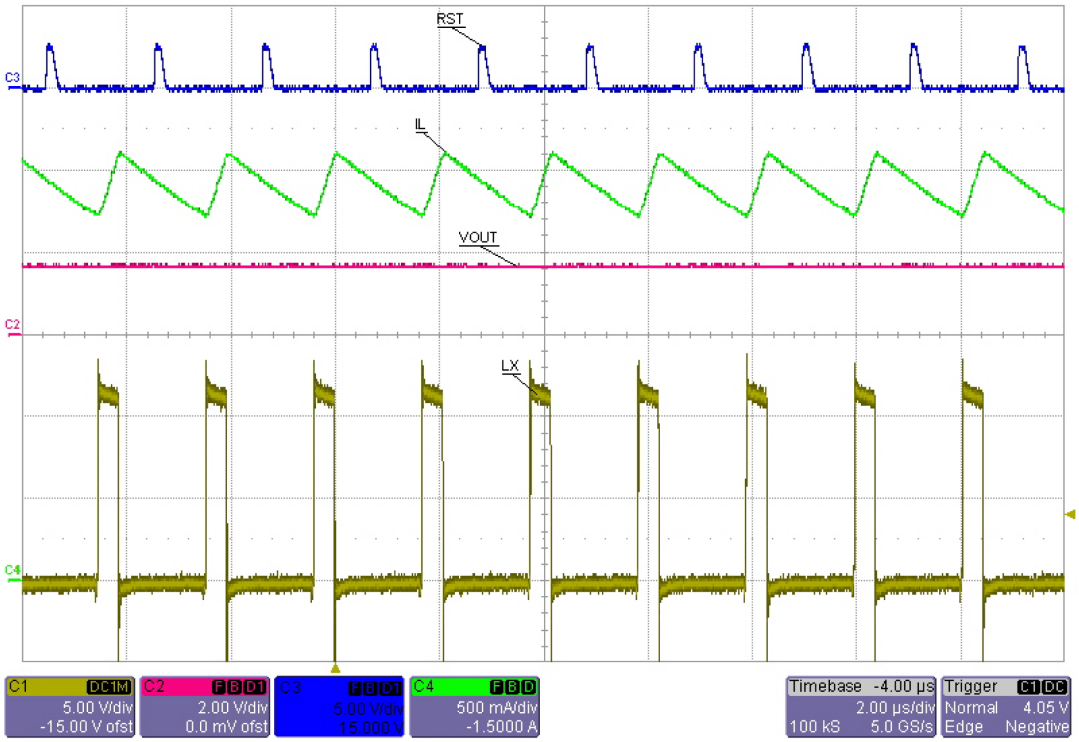
$$I_{MAX} = I_{VALLEYTH} + \frac{V_{IN} - V_{OUT}}{L} \cdot T_{MASKHS} \quad (15)$$

where I_{VALLEY_TH} is the current threshold of the valley sensing circuitry (see Table 5. Electrical characteristics) and T_{MASK_HS} is the masking time of the high-side switch 100 ns typ.).

In most of the overcurrent conditions the conduction time of the high-side switch is higher than the masking time and so the peak current protection limits the switch current.

$$I_{MAX} = I_{PEAK\_TH} \quad (16)$$

Figure 30. **Peak current sense operation in overcurrent condition**



The DC current flowing in the load in overcurrent condition is:

$$I_{DCOC}(V_{OUT}) = I_{MAX} - \frac{I_{RIPPLE}(V_{OUT})}{2} = I_{MAX} - (\frac{V_{IN} - V_{OUT}}{2 \cdot L} \cdot T_{ON}) \quad (17)$$

4.11 OCP and switchover feature

Output capacitor discharging the current flowing to ground during heavy short-circuit events is only limited by parasitic elements like the output capacitor ESR and short-circuit impedance.

Due to parasitic inductance of the short-circuit impedance, negative output voltage oscillations can be generated with huge discharging current levels (see Figure 1).

Figure 31. **Output voltage oscillations during heavy short-circuit**

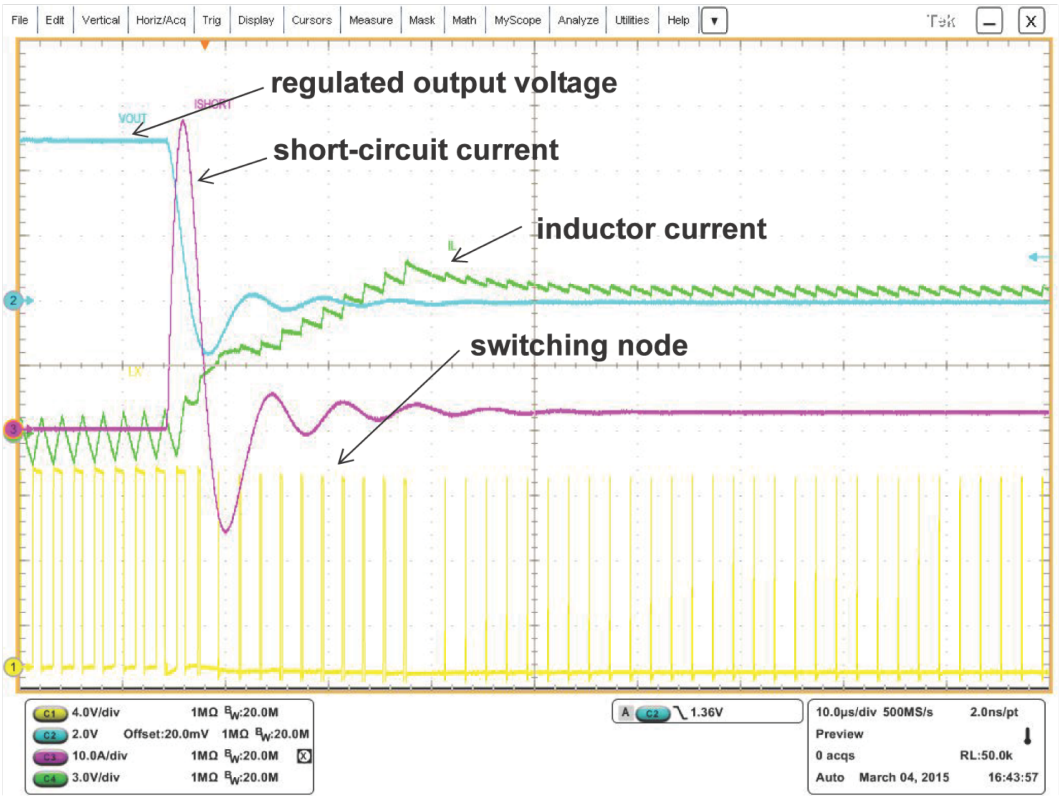
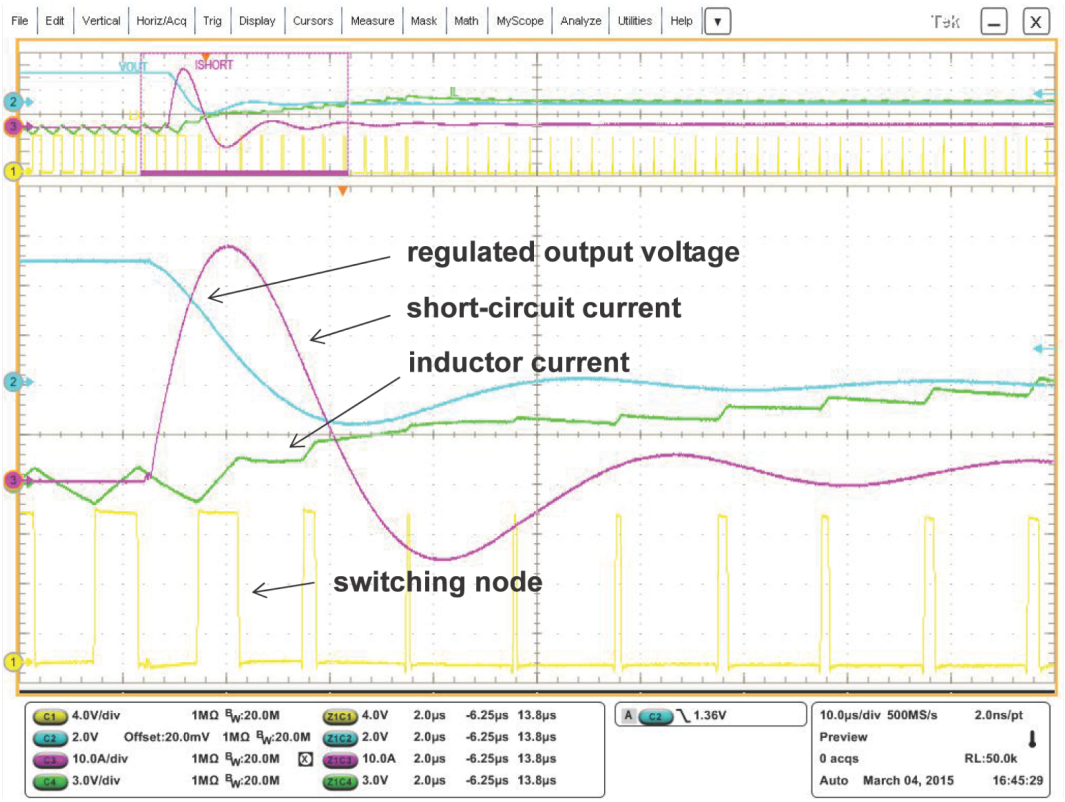


Figure 32. **Zoomed waveforms**

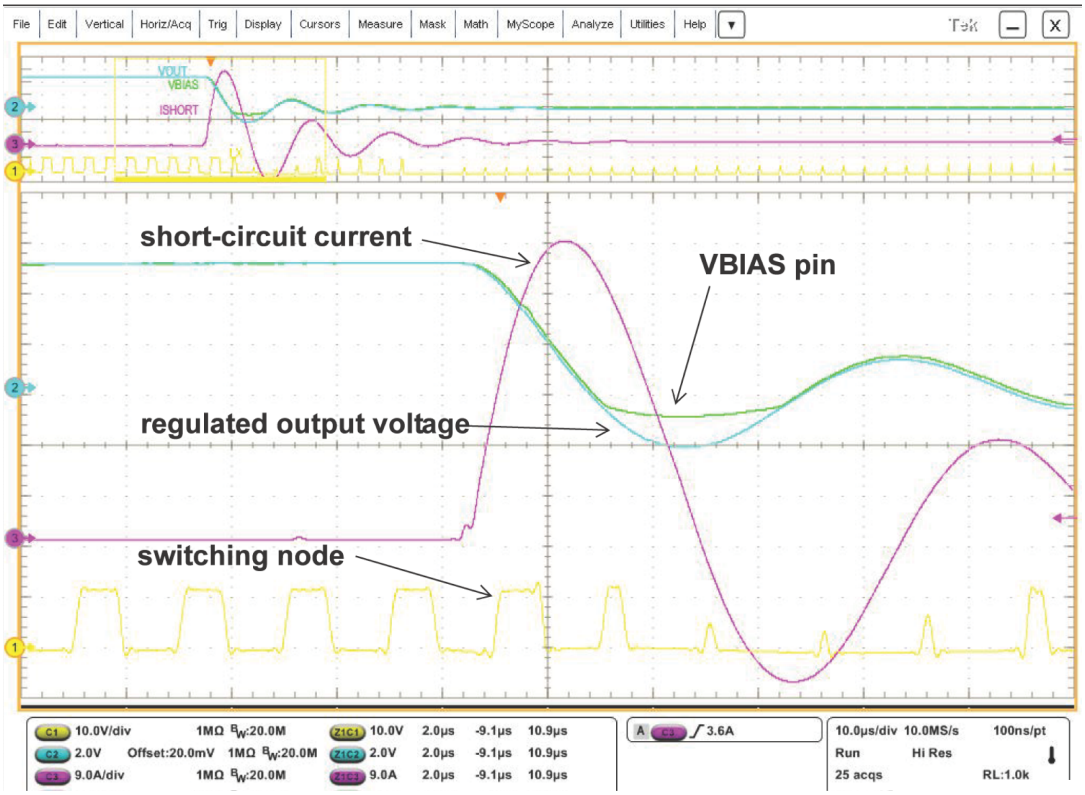


The V_{BIAS} pin absolute maximum ratings (see Table 1) must be satisfied over the different dynamic conditions.

If the V_{BIAS} is connected to GND there are no issues (see Figure 31. Output voltage oscillations during heavy short-circuit and Figure 32. Zoomed waveforms).

A small resistor value (few ohms) in series with the V_{BIAS} can help to limit the pin negative voltage (see Figure 33. V_{BIAS} in heavy short-circuit event) during heavy short-circuit events if it is connected to the regulated output voltage.

Figure 33. V_{BIAS} in heavy short-circuit event



4.12 Overvoltage protection

The overvoltage protection monitors the VOUT pin and enables the low-side MOSFET to discharge the output capacitor if the output voltage is 20% over the nominal value.

This is a second level protection and should never be triggered in normal operating conditions if the system is properly dimensioned. In other words, the selection of the external power components and the dynamic performance determined by the compensation network should guarantee an output voltage regulation within the overvoltage threshold even during the worst case scenario in term of load transitions.

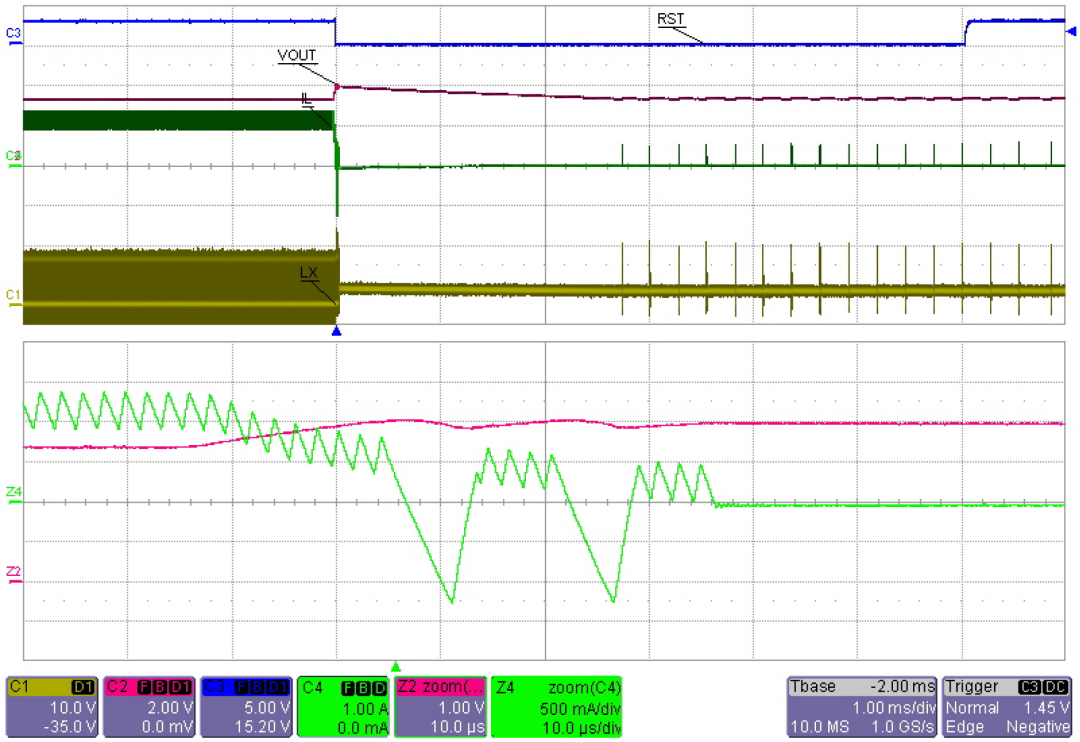
The protection is reliable and also able to operate even during normal load transitions for a system whose dynamic performance is not in line with the load dynamic request. As a consequence the output voltage regulation would be affected.

Figure 34. Overvoltage operation shows the overvoltage operation during a negative steep load transient for a system configured in low consumption mode and designed with a not optimized compensation network. This can be considered as an example for a system with dynamic performance not in line with the load request.

The L6986H device implements a 1 A typ. negative current limitation to limit the maximum reversed switch current during the overvoltage operation.

Moreover, the overvoltage protection also activates the internal pull-down on RST pin. Once OVP is deactivated, the L6986H releases the RST pin after the delay programmed by DELAY capacitor (6 ms in Figure 34. Overvoltage operation).

Figure 34. **Overvoltage operation**

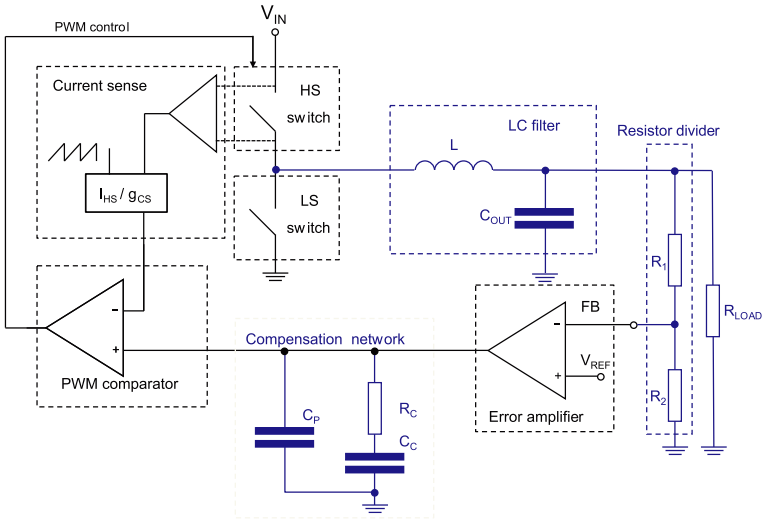


4.13 Thermal shutdown

The shutdown block disables the switching activity if the junction temperature is higher than a fixed internal threshold (165 °C typical). The thermal sensing element is close to the power elements, ensuring fast and accurate temperature detection. A hysteresis of approximately 30 °C prevents the device from turning ON and OFF continuously. When the thermal protection runs away a new soft-start cycle will take place.

5 Closing the loop

Figure 35. **Block diagram of the loop**



5.1 $G_{CO}(s)$ control to output transfer function

The accurate control to output transfer function for a buck peak current mode converter can be written as:

$$G_{CO}(s) = R_{LOAD} \cdot g_{CS} \cdot \frac{1}{1 + \frac{R_{LOAD} \cdot T_{SW}}{L} \cdot [m_C \cdot (1 - D) - 0.5]} \cdot \frac{1 + \frac{S}{\omega_Z}}{1 + \frac{S}{\omega_p}} \cdot F_H(s) \quad (18)$$

where R_{LOAD} represents the load resistance, g_{CS} the equivalent sensing transconductance of the current sense circuitry, w_p the single pole introduced by the power stage and w_z the zero given by the ESR of the output capacitor.

$F_H(s)$ accounts the sampling effect performed by the PWM comparator on the output of the error amplifier that introduces a double pole at one half of the switching frequency.

$$\omega_Z = \frac{1}{ESR \cdot C_{OUT}} \quad (19)$$

$$\omega_p = \frac{1}{R_{LOAD} \cdot C_{OUT}} + \frac{m_c \cdot (1 - D) - 0.5}{L \cdot C_{OUT} \cdot f_{SW}} \quad (20)$$

where:

$$\begin{cases} m_C = 1 + \frac{S_e}{S_n} \\ S_e = V_{PP} \cdot g_{CS} \cdot f_{SW} \\ S_n = \frac{V_{IN} - V_{OUT}}{L} \end{cases} \quad (21)$$

S_n represents the on time slope of the sensed inductor current, Se the on time slope of the external ramp (V_{PP} peak-to-peak amplitude) that implements the slope compensation to avoid sub-harmonic oscillations at duty cycle over 50%.

S_e can be calculated from the parameter $V_{PP} \times g_{CS}$ given in Table 1 .

The sampling effect contribution $F_H(s)$ is:

$$F_H(s) = \frac{1}{1 + \frac{s}{\omega_n \cdot Q_p + \frac{s^2}{\omega_n^2}}} \quad (22)$$

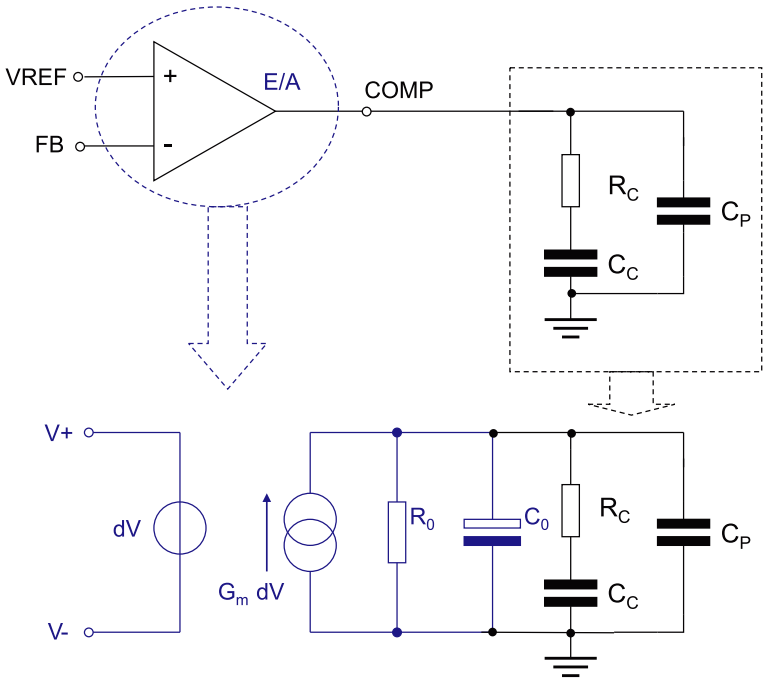
where:

$$\begin{cases} \omega_n = \pi \cdot f_{SW} \\ Q_p = \frac{1}{\pi \cdot [m_c \cdot (1 - D) - 0.5]} \end{cases} \quad (23)$$

5.2 Error amplifier compensation network

The typical compensation network required to stabilize the system is shown in Figure 36. Transconductance embedded error amplifier:

Figure 36. Transconductance embedded error amplifier



R_C and C_C introduce a pole and a zero in the open loop gain. C_P does not significantly affect system stability but it is useful to reduce the noise at the output of the error amplifier.
The transfer function of the error amplifier and its compensation network is:

$$A_0(s) = \frac{A_{V0} \cdot (1 + s \cdot R_C \cdot C_c)}{s^2 \cdot R_0 \cdot (C_0 + C_p) \cdot R_C \cdot C_c + s \cdot (R_0 \cdot C_c + R_0 \cdot (C_0 + C_p) + R_c \cdot C_c) + 1} \quad (24)$$

Where $A_{vo} = G_m \cdot R_o$
The poles of this transfer function are (if $C_c >> C_0 + C_P$):

$$f_{PLF} = \frac{1}{2 \cdot \pi \cdot R_0 \cdot C_c} \quad (25)$$

$$f_{PHF} = \frac{1}{2 \cdot \pi \cdot R_0 \cdot (C_0 + C_p)} \quad (26)$$

whereas the zero is defined as:

$$f_Z = \frac{1}{2 \cdot \pi \cdot R_c \cdot C_c} \tag{27}$$

5.3 Voltage divider

The contribution of the internal voltage divider for fixed output voltage devices is:

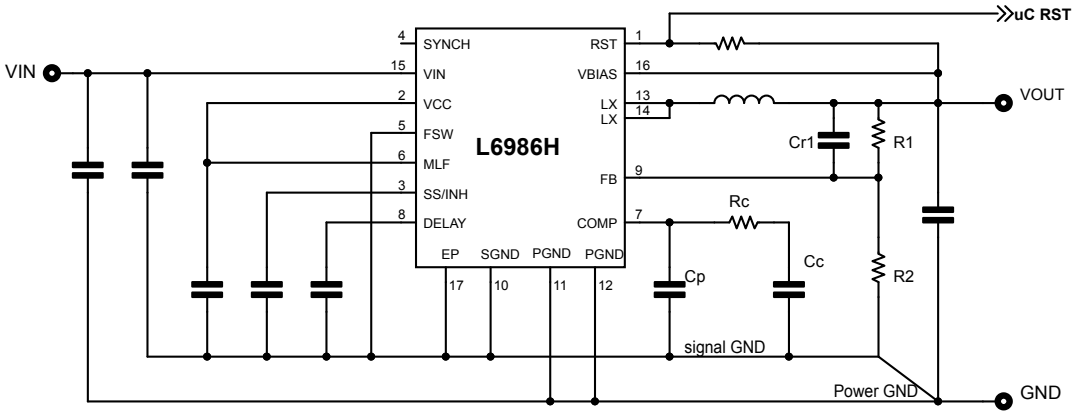
$$G_{DIV}(s) = \frac{R_2}{R_1 + R_2} = \frac{V_{FB}}{V_{OUT}} = \frac{0.85}{3.3} = 0.2575 \qquad L6986H3V$$
$$G_{DIV}(s) = \frac{R_2}{R_1 + R_2} = \frac{V_{FB}}{V_{OUT}} = \frac{0.85}{5} = 0.17 \qquad L698H5V \tag{28}$$

while for the adjustable output part number L6986H is:

$$G_{DIV}(s) = \frac{R_2}{R_1 + R_2} \qquad L6986H \tag{29}$$

A small signal capacitor in parallel to the upper resistor (see Figure 37. Leading network example) of the voltage divider implements a leading network ($f_{zero} < f_{pole}$), sometimes necessary to improve the system phase margin:

Figure 37. Leading network example



The Laplace transformer of the leading network is:

$$G_{DIV}(s) = \frac{R_2}{R_1 + R_2} \cdot \frac{(1 + s + R_1 \cdot C_{R1})}{(1 + s \cdot \frac{R_1 \cdot R_2}{R_1 + R_2} \cdot C_{R1})} \tag{30}$$

where

$$f_Z = \frac{1}{2 \cdot \pi \cdot R_1 \cdot C_{R1}}$$
$$f_p = \frac{1}{2 \cdot \pi \cdot \frac{R_1 \cdot R_2}{R_1 + R_2} \cdot C_{R1}} \tag{31}$$
$$f_Z < f_p$$

5.4 Total loop gain

In summary, the open loop gain can be expressed as:

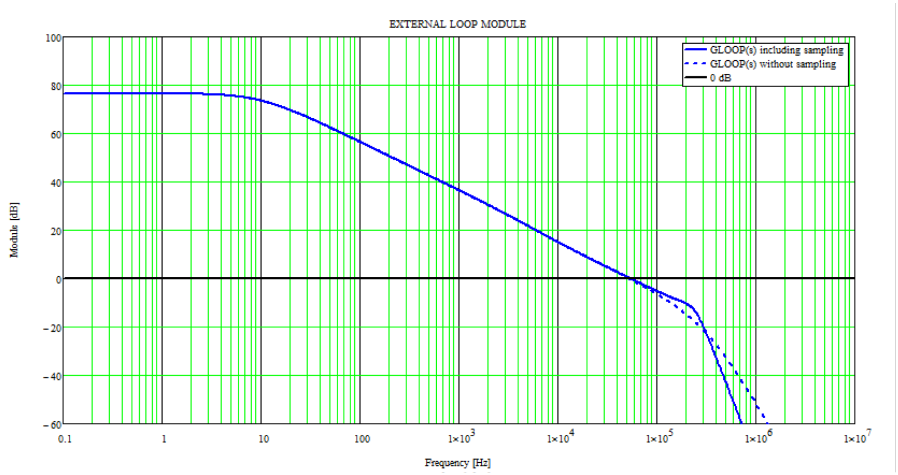
$$G_{(s)} = G_{DIV}(s) \cdot G_{CO}(s) \cdot A_0(s) \quad (32)$$

example 1:

V_{IN} = 12 V, V_{OUT} = 3.3 V, R_{OUT} = 1.67 Ω

Selecting the L6986H with V_{OUT}=3.3 V, f_{SW} = 500 kHz, L = 10 µH, C_{OUT} = 20 µF and ESR = 3 mΩ, R_C = 75 kΩ, C_C = 330 pF, C_P = 2.2 pF (please refer to Table 19. L6986H 3V3 demonstration board BOM), the gain and phase bode diagrams are plotted respectively in Figure 38. Module plot and Figure 39. Phase plot.

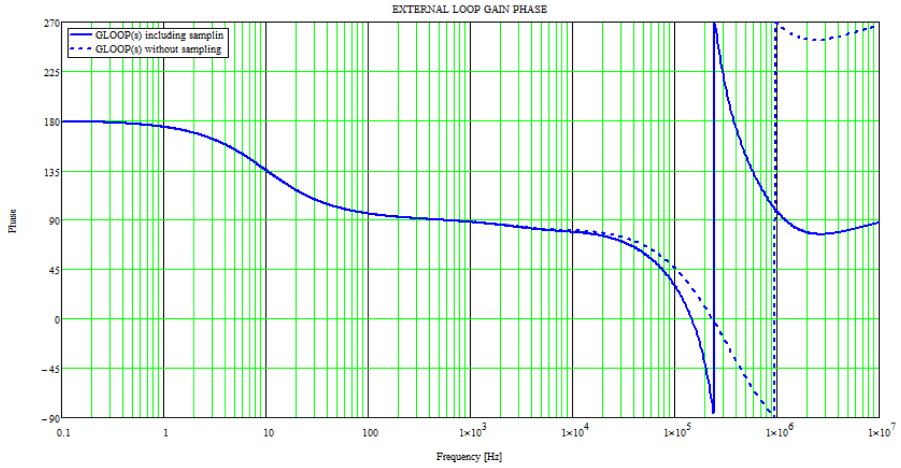
Figure 38. Module plot



BW = 55 kHZ

phase margin = 60 °

Figure 39. Phase plot



The blue solid trace represents the transfer function including the sampling effect term (see), the dotted blue trace neglects the contribution.

5.5 Compensation network design

The maximum bandwidth of the system can be designed up to f_{SW}/6 up to 150 kHz maximum to guarantee a valid small signal model.

$$R_C = \frac{2 \cdot \pi \cdot BW \cdot C_{OUT} \cdot V_{OUT}}{0.85V \cdot g_{CS} \cdot g_{m\ \ TYP}} \quad (33)$$

where:

$$f_{POLE} = \frac{\omega_p}{2 \cdot \pi} \quad (34)$$

ω_p is defined by , gCS represents the current sense transconductance (see Table 1) and $g_{m\ TYP}$ the error amplifier transconductance.

$$C_C = \frac{5}{2 \cdot \pi \cdot R_C \cdot BW} \quad (35)$$

Example 2:

Considering V_{IN} = 12 V, V_{OUT} = 3.3 V, L = 6.8 µH, C_{OUT} = 10 µF, f_{SW} = 500 kHz, I_{OUT} = 1 A.

The maximum system bandwidth is 80 kHz. Assuming to design the compensation network to achieve a system bandwidth of 70 kHz:

$$f_{POLE} = 2.7\ \ kHz \quad (36)$$

$$R_{LOAD} = \frac{V_{OUT}}{I_{OUT}} = 3.3\Omega \quad (37)$$

so accordingly with Eq. (33) and Eq. (35):

$$R_C = 48.5k\Omega \approx 47k\Omega \quad (38)$$

$$C_C = 237pF \approx 270pF \quad (39)$$

The gain and phase bode diagrams are plotted respectively in Figure 40. Magnitude plot for example 2 and Figure 41. Phase plot for example 2.

Figure 40. Magnitude plot for example 2

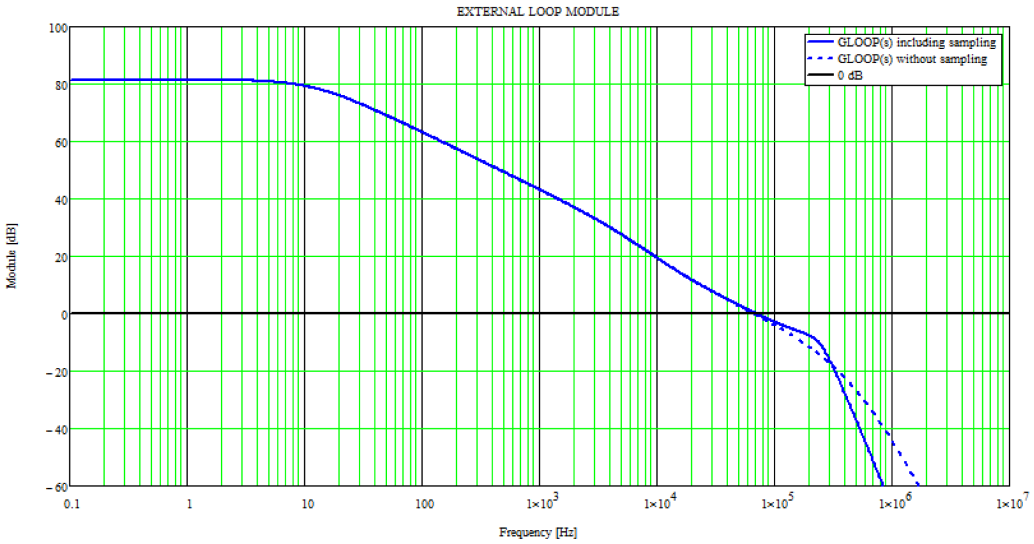
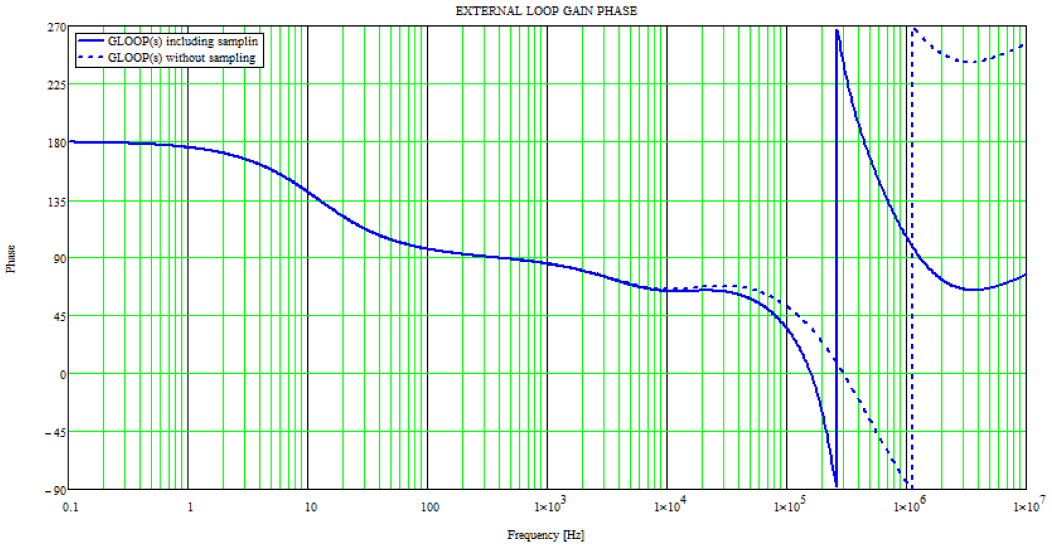


Figure 41. **Phase plot for example 2**



6 Application notes

6.1 Output voltage adjustment

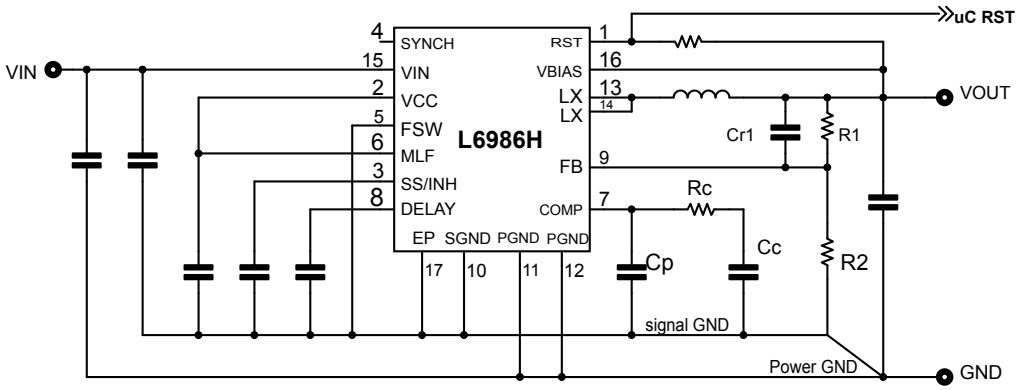
The error amplifier reference voltage is 0.85 V typical.

The output voltage is adjusted accordingly as per equation below: (see Figure 42. L6986H application circuit).

$$V_{OUT} = 0.85 \cdot (1 + \frac{R_1}{R_2}) \quad (40)$$

C_{r1} capacitor is sometimes useful to increase the small signal phase margin (please refer to Compensation network design).

Figure 42. L6986H application circuit



6.2 Switching frequency

A resistor connected to the FSW pin features the selection of the switching frequency. The pinstrapping is performed at power-up, before the soft-start takes place. The FSW pin is pinstrapped and then driven floating in order to minimize the quiescent current from VIN. Please refer to Table 2 to identify the pull-up / pull-down resistor value. f_{SW} = 250 kHz / f_{SW} = 500 kHz preferred codifications do not require any external resistor.

6.3 MLF pin

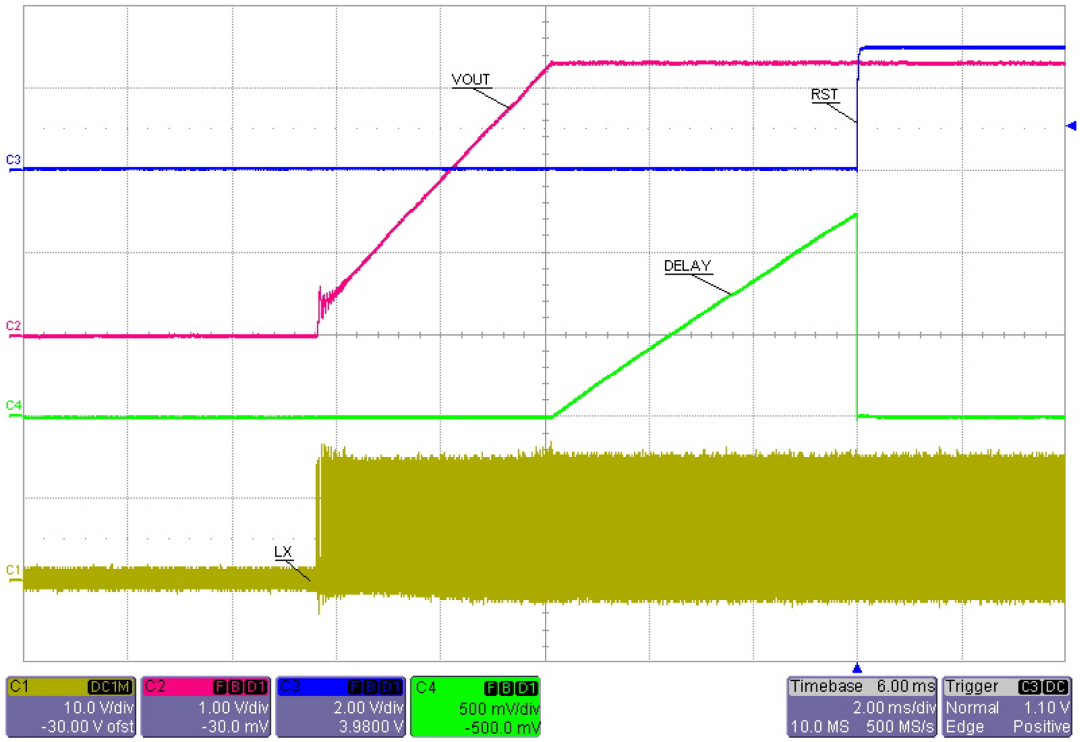
A resistor connected to the MLF pin features the selection of the between low noise mode / low consumption mode and the different RST thresholds. The pinstrapping is performed at power-up, before the soft-start takes place. The FSW pin is pinstrapped and then driven floating in order to minimize the quiescent current from VIN.

Please refer to Table 7. LNM/ LCM selection (L6986H3V3), Table 8. LNM/ LCM selection (L6986H5V), and Table 9. LNM/ LCM selection (L6986H) to identify the pull-up / pull-down resistor value. (LNM, RST threshold 93%) / (LCM, RST threshold 93%) preferred codifications don't require any external resistor.

6.4 Voltage supervisor

The embedded voltage supervisor (composed of the RST and the DELAY pins) monitors the regulated output voltage and keeps the RST open collector output in low impedance as long as the V_{OUT} is out of regulation. In order to ensure a proper reset of digital devices with a valid power supply, the device can delay the RST assertion with a programmable time.

Figure 43. Voltage supervisor operation



The comparator monitoring the FB voltage has four different programmable thresholds (80%, 87%, 93%, 96% nominal output voltage) for high flexibility (see MLF pin, Table 7. LNM/ LCM selection (L6986H3V3), Table 8. LNM/ LCM selection (L6986H5V), and Table 9. LNM/ LCM selection (L6986H)).

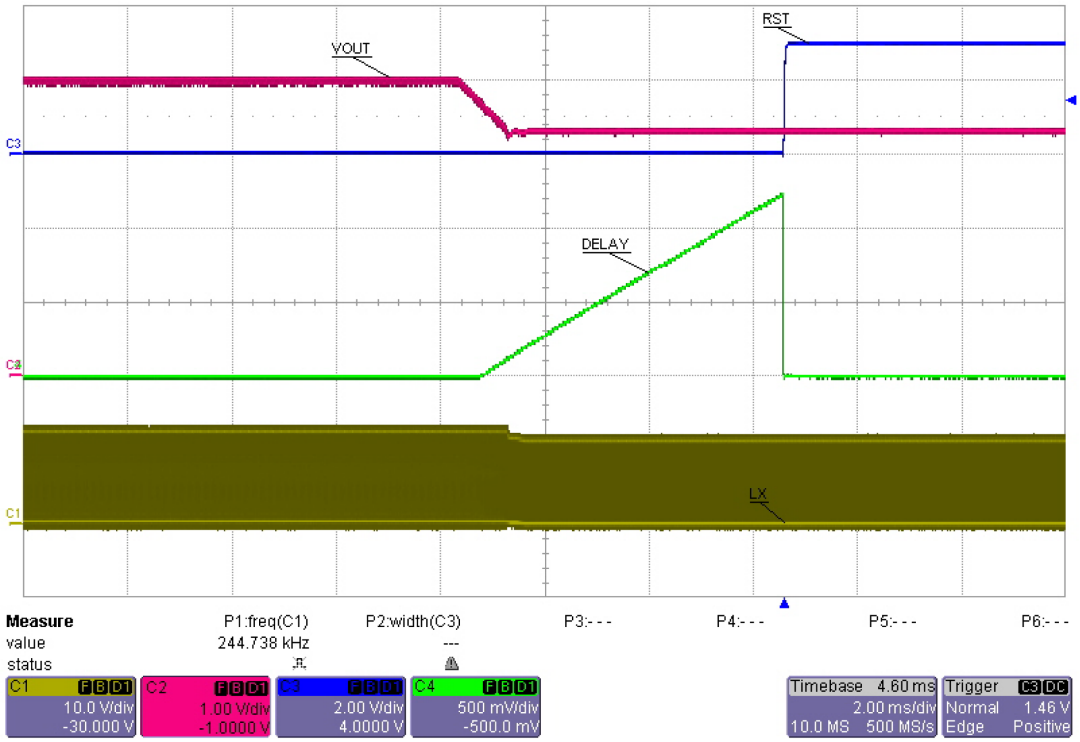
When the RST comparator detects the output voltage is in regulation, a 2 mA internal current source starts to charge an external capacitor to implement a voltage ramp on the DELAY pin. The RST open collector is then released as soon as V_{DELAY} = 1.234 V (see Figure 43. Voltage supervisor operation). The C_{DELAY} is dimensioned as follows:

$$C_{DELAY} = \frac{I_{SSCH} \cdot T_{DELAY}}{V_{DELAY}} = \frac{2\mu A \cdot T_{DELAY}}{1.234V} \quad (41)$$

The maximum suggested capacitor value is 270 nF.

The L6986H also activates internal pull-down on RST pin in case overvoltage protection is triggered. As soon as the output voltage goes below OVP threshold (20% typ.), the 2 µA internal current source starts to charge an external capacitor to implement a voltage ramp on the DELAY pin. The RST open collector is then released as soon as V_{DELAY} = 1.234 V(see figure below).

Figure 44. **Voltage supervisor operation during OVP**



6.5 Synchronization (LNM)

The synchronization feature helps the hardware designer to prevent beating frequency noise that is an issue when multiple switching regulators populate the same application board.

6.5.1 Embedded master - slave synchronization

The L6986H synchronization circuitry features the same switching frequency for a set of regulators simply connecting their SYNCH pin together, so preventing beating noise. The master device provides the synchronization signal to the others since the SYNCH pin is I/O able to deliver or recognize a frequency signal.

For proper synchronization of multiple regulators, all of them have to be configured with the same switching frequency (see Table 2), so the same resistor connected at the FSW pin.

In order to minimize the RMS current flowing through the input filter, the L6986H device provides a phase shift of 180° between the master and the SLAVES. If more than two devices are synchronized, all slaves will have a common 180° phase shift with respect to the master.

Considering two synchronized L6986H which regulate the same output voltage (i.e.: operating with the same duty cycle), the input filter RMS current is optimized and is calculated as:

$$I_{RMS} = \begin{cases} \frac{I_{OUT}}{2} \cdot \sqrt{2D \cdot (1-2D)} & if D < 0.5 \\ \frac{I_{OUT}}{2} \cdot \sqrt{(2D-1) \cdot (2-2D)} & if D > 0.5 \end{cases} \quad (42)$$

The graphical representation of the input RMS current of the input filter in the case of two devices with 0° phase shift (synchronized to an external signal) or 180° phase shift (synchronized connecting their SYNCH pins) regulating the same output voltage is provided in the figure below. To dimension the proper input capacitor please refer to Input capacitor selection).

Figure 45. **Input RMS current**

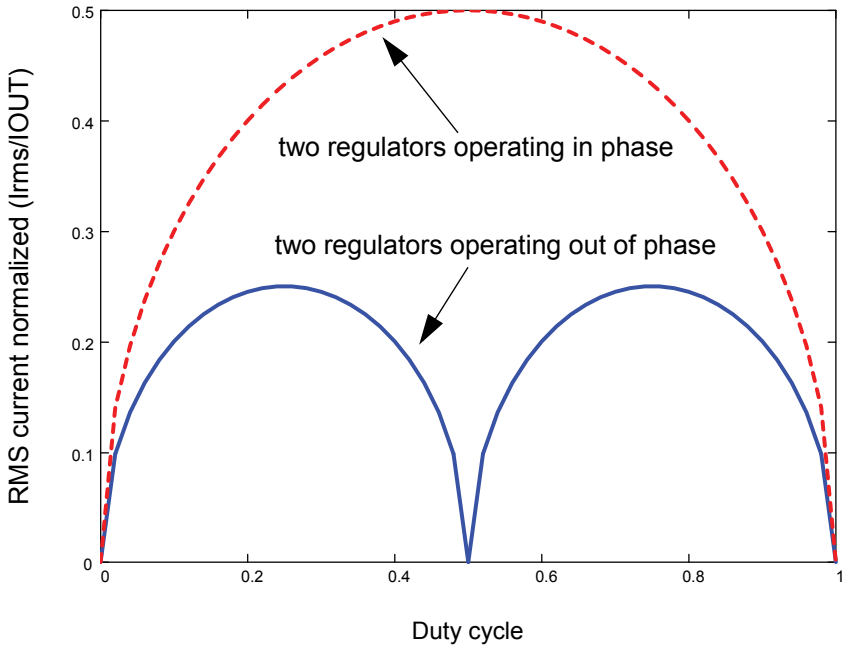


Figure 46. Two regulators not synchronized shows two not synchronized regulators with unconnected SYNCH pin.

Figure 46. **Two regulators not synchronized**

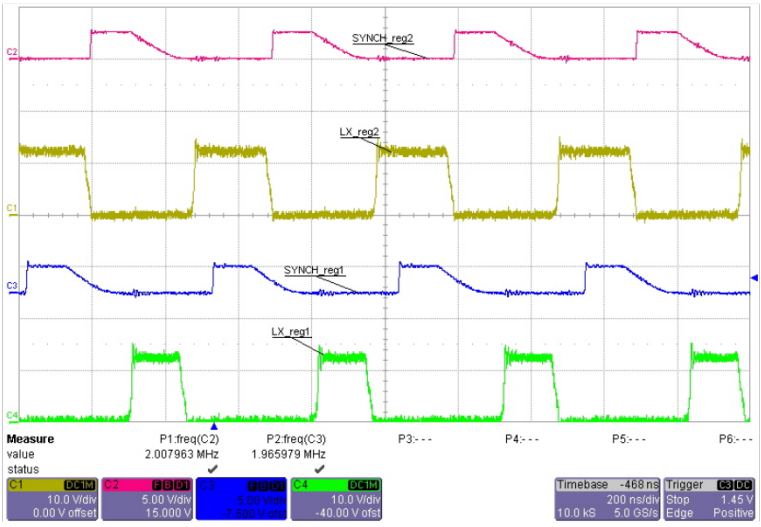
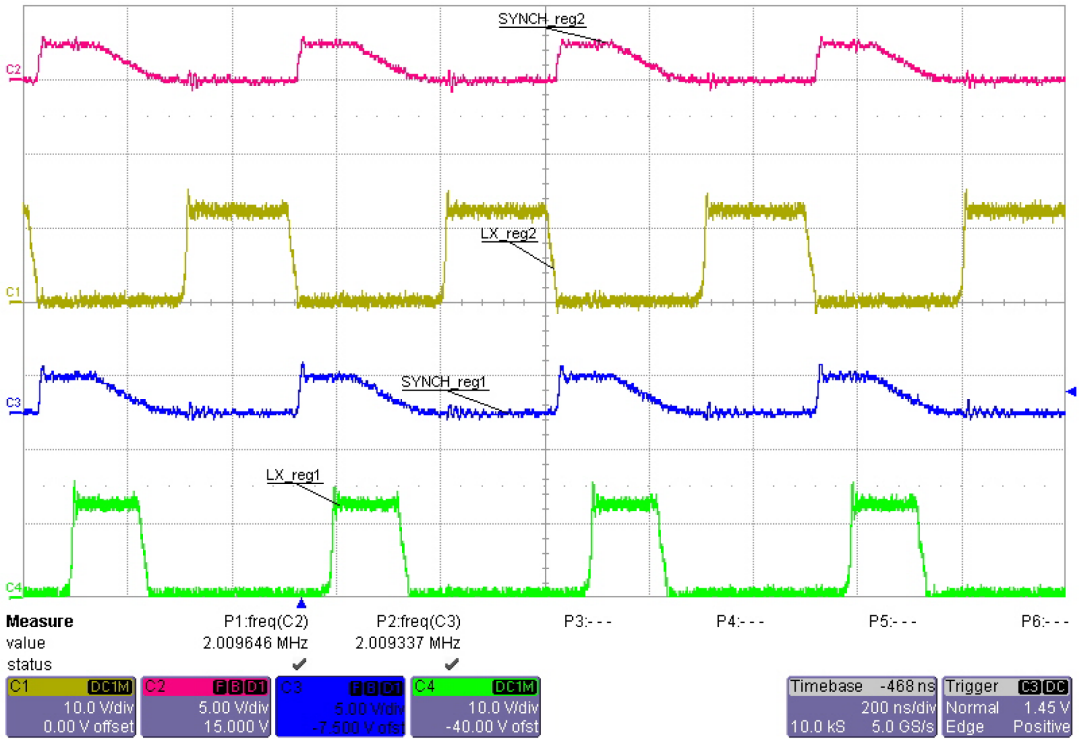


Figure 47. Two regulators synchronized shows the same regulators working synchronized having the SYNCH pins connected. The MASTER regulator (LX_reg2 trace) delivers the synchronization signal to the SLAVE device (LX_reg1). The SLAVE regulator works in phase with the synchronization signal, which is out of phase with the MASTER switching operation.

Figure 47. **Two regulators synchronized**



6.5.2 External synchronization signal

Multiple L6986H can be synchronized to an external frequency signal fed to the SYNCH pin. In this case the regulator set is phased to the reference and all the devices will work with 0° phase shift.

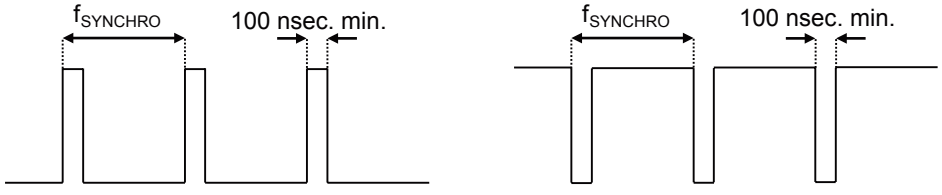
The minimum synchronization pulse width is 100 ns and the frequency range of the synchronization signal is:

- [275 kHz - 1.4 MHz] if $f_{SW\_PROGRAMMED}$ < 500 kHz
- [475 kHz - 2.2 MHz] if $f_{SW\_PROGRAMMED}$ ≥ 500 kHz

(see Figure 48. Synchronization pulse definition).

Figure 48. **Synchronization pulse definition**

275 kHz < $f_{SYNCHRO}$ < 1.4 MHz if $f_{SW\_PROGRAMMED}$ < 500 kHz typ
475 kHz < $f_{SYNCHRO}$ < 2.2 MHz if $f_{SW\_PROGRAMMED}$ ≥ 500 kHz typ

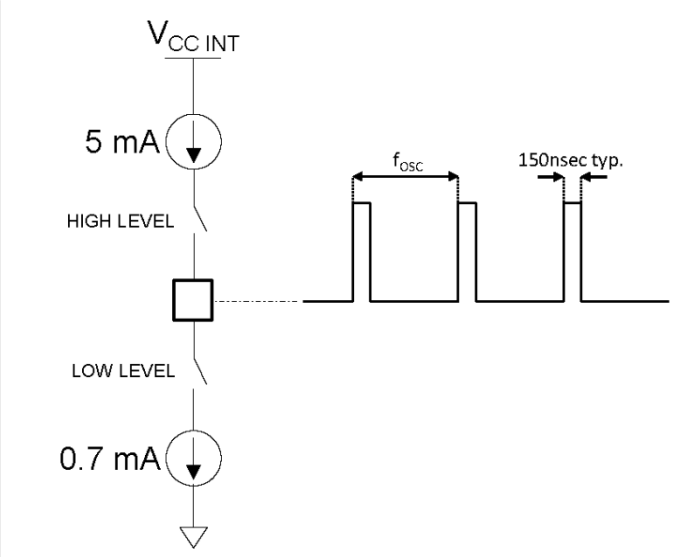


Since the internal slope compensation contribution that is required to prevent subharmonic oscillations in peak current mode architecture depends on the oscillator frequency, it is important to select the same oscillator frequency for all regulators (all of them operate as SLAVE) as close as possible to the frequency of the reference signal (please refer to Table 2). As a consequence all the regulators have the same resistor value connected to the FSW pin, so the slope compensation is optimized accordingly with the frequency of the synchronization signal. The slope compensation contribution is latched at power-up and so fixed during the device operation.

The L6986H normally operates in the MASTER mode, driving the SYNCH line at the selected oscillator frequency as shown in Figure 49. L6986H synchronization driving capability.

In the SLAVE mode the L6986H sets the internal oscillator at 250 kHz typ. (see Table 2) and drives the line accordingly.

Figure 49. L6986H synchronization driving capability



In order to safely guarantee that each regulator recognizes itself in SLAVE mode when synchronized, the external master must drive the SYNCH pin with a clock signal frequency higher than the maximum oscillator spread of the selected line in Table 2 for at least 10 internal clock cycles.

Once recognized as SLAVE the synchronization range is:

- 275 - 1.4 MHz if f_{SW} < 500 kHz
- 475 kHz - 2.2 MHz if f_{SW} >=500 kHz

example 1: selecting R_{FSW} = 0 Ω to VCC

Table 13. Example of oscillator frequency selection

Symbol	R_{VCC} (E24 series)	R_{GND} (E24 series)	f_{SW} min.	f_{SW} typ.	f_{SW} max.
f_{SW}	NC	0 Ω	225	250	275

the device enters in slave mode after 10 pulses at frequency higher than 275 kHz and so it is able to synchronize to a clock signal in the range 275 kHz - 1.4 MHz (see Figure 48. Synchronization pulse definition).

Example 2: selecting R_{FSW} = 0 Ω to GND

Table 14. Example of oscillator frequency selection (2)

Symbol	R_{VCC} (E24 series)	R_{GND} (E24 series)	f_{SW} min.	f_{SW} typ.	f_{SW} max.
f_{SW}	NC	0 Ω	450	500	550

The device enters in slave mode after 10 pulses at frequency higher than 550 kHz and so it is able to synchronize to a clock signal in the range 475 kHz - 2.2 MHz (see Figure 48. Synchronization pulse definition).

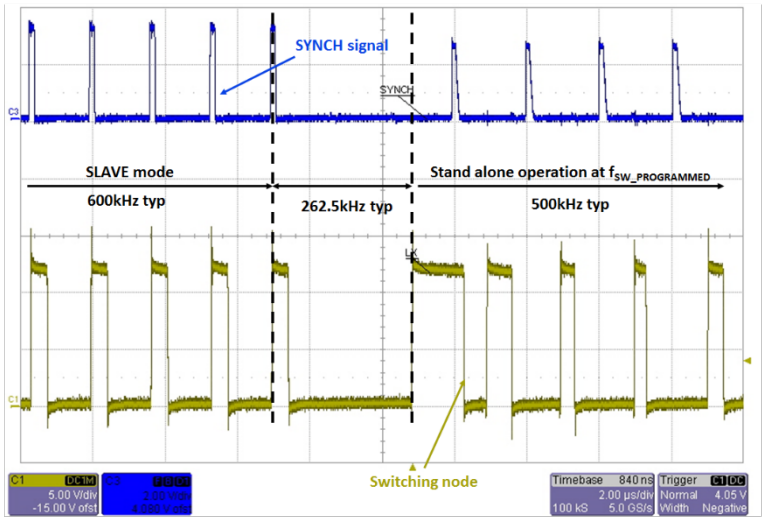
As anticipated above, in SLAVE mode the internal oscillator operates at 250 kHz typ. but the slope compensation is dimensioned accordingly with FSW resistors so it is important to limit the switching operation around a working point close to the selected oscillator frequency (FSW resistor).

As a consequence, to guarantee the full output current capability and to prevent the subharmonic oscillations, the MASTER may limit the driving frequency range within ± 5% of the selected frequency.

A wider frequency range may generate subharmonic oscillation for duty > 50% or limit the peak current capability (see IPK parameter in Table 1) since the internal slope compensation signal may be saturated.

The device keeps operating in slave mode as far as the master is able to drive the SYNCH pin faster than 275 kHz, otherwise the L6986H goes back into MASTER mode at the programmed R_{FSW} oscillator frequency after successfully driving one pulse 250 kHz typ. (see Figure 50. Slave-to-master mode transition) in the SYNCH line.

Figure 50. Slave-to-master mode transition

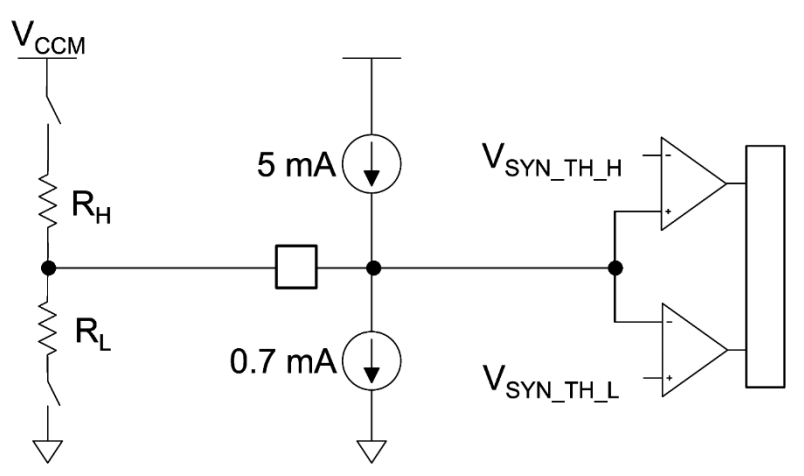


The external master can force a latched SLAVE mode driving the SYNCH pin low at power-up, before the soft-start begins the switching activity. So the oscillator frequency is 250 kHz typ. fixed until a new UVLO event is triggered regardless FSW resistor value, that otherwise counts to design the slope compensation. The same considerations above are also valid.

The master driving capability must be able to provide the proper signal levels at the SYNCH pin (see Table 1):

- Low level < $V_{SYN\ THL}$ = 0.7 V sinking 5 mA
- High level > $V_{SYN\ THH}$ = 1.2 V sourcing 0.7 mA

Figure 51. **Master driving capability to synchronize the L6986H**



6.6 Design of the power components

6.6.1 Input capacitor selection

The input capacitor voltage rating must be higher than the maximum input operating voltage of the application. During the switching activity a pulsed current flows into the input capacitor and so its RMS current capability must be selected accordingly with the application conditions. Internal losses of the input filter depends on the ESR value so usually low ESR capacitors (like multilayer ceramic capacitors) have higher RMS current capability. On the other hand, given the RMS current value, lower ESR input filter has lower losses and so contributes to higher conversion efficiency.

The maximum RMS input current flowing through the capacitor can be calculated as:

$$I_{RMS} = I_{OUT} \cdot \sqrt{(1 - \frac{D}{\eta}) \cdot \frac{D}{\eta}} \quad (43)$$

Where I_{OUT} is the maximum DC output current, D is the duty cycles, η is the efficiency. This function has a maximum at D = 0.5 and, considering h = 1, it is equal to $I_{OUT}/2$.

In a specific application the range of possible duty cycles has to be considered in order to find out the maximum RMS input current. The maximum and minimum duty cycles can be calculated as:

$$D_{MAX} = \frac{V_{OUT} + \Delta V_{LOWSIDE}}{V_{INMIN} + \Delta V_{LOWSIDE} - V_{INMIN} + \Delta V_{HIGHSIDE}} \quad (44)$$

$$D_{MIN} = \frac{V_{OUT} + \Delta V_{LOWSIDE}}{V_{INMAX} + \Delta V_{LOWSIDE} - V_{INMIN} + \Delta V_{HIGHSIDE}} \quad (45)$$

Where DV_{HIGH_SIDE} and DV_{LOW_SIDE} are the voltage drops across the embedded switches. The peak-to-peak voltage across the input filter can be calculated as follows:

$$C_{IN} = \frac{I_{OUT}}{V_{PP} \cdot f_{SW}} \cdot (1 - \frac{D}{\eta}) \cdot \frac{D}{\eta} + ESR \cdot (I_{OUT} + \Delta I_L) \quad (46)$$

In case of negligible ESR (MLCC capacitor) the equation of C_{IN} as a function of the target V_{PP} can be written as follows:

$$C_{IN} = \frac{I_{OUT}}{V_{PP} \cdot f_{SW}} \cdot (1 - \frac{D}{\eta}) \cdot \frac{D}{\eta} \quad (47)$$

Considering η=1 this function has its maximum in D = 0.5:

$$C_{INMIN} = \frac{I_{OUT}}{4 \cdot V_{PPMAX} \cdot f_{SW}} \quad (48)$$

Typically C_{IN} is dimensioned to keep the maximum peak-peak voltage across the input filter in the order of 5% V_{IN_MAX}.

Table 15. **Input capacitors**

Manufacturer	Series	Size	Cap value (µF)	Rated voltage (V)
TDK	C3225X7S1H106M	1210	10	50
	C3216X5R1H106M	1206	-	-
Taiyo Yuden	UMK325BJ106MM-T	1210	-	-

6.6.2 Inductor selection

The inductor current ripple flowing into the output capacitor determines the output voltage ripple (please refer to Output capacitor selection). Usually the inductor value is selected in order to keep the current ripple lower than 20% - 40% of the output current over the input voltage range. The inductance value can be calculated by equation below:

$$\Delta I_L = \frac{V_{IN} - V_{OUT}}{L} \cdot T_{ON} = \frac{V_{OUT}}{L} \cdot T_{OFF} \quad (49)$$

Where T_{ON} and T_{OFF} are the on and off time of the internal power switch. The maximum current ripple, at fixed V_{OUT}, is obtained at maximum T_{OFF} that is at minimum duty cycle (see Input capacitor selection to calculate minimum duty). So fixing ΔI_L = 20% to 40% of the maximum output current, the minimum inductance value can be calculated:

$$L_{MIN} = \frac{V_{OUT}}{\Delta I_{LMAX}} \cdot \frac{1 - D_{MIN}}{f_{SW}} \quad (50)$$

where f_{SW} is the switching frequency 1/(T_{ON} + T_{OFF}).

For example for V_{OUT} = 3.3 V, V_{IN} = 12 V, I_{OUT} = 2 A and F_{SW} = 500 kHz the minimum inductance value to have ΔI_L = 30% of I_{OUT} is about 8.2 µH.

The peak current through the inductor is given by:

$$I_{L,\ PK} = I_{OUT} + \frac{\Delta I_L}{2} \quad (51)$$

So if the inductor value decreases, the peak current (that has to be lower than the current limit of the device) increases. The higher is the inductor value, the higher is the average output current that can be delivered, without reaching the current limit.

In the table below, some inductor part numbers are listed.

Table 16. **Inductors**

Manufacturer	Series	Inductor value (µH)	Saturation current (A)
Coilcraft	XAL50xx	2.2 to 22	6.5 to 2.7
	XAL60xx		12.5 to 4

6.6.3 Output capacitor selection

The triangular shape current ripple (with zero average value) flowing into the output capacitor gives the output voltage ripple, that depends on the capacitor value and the equivalent resistive component (ESR). As a consequence the output capacitor has to be selected in order to have a voltage ripple compliant with the application requirements.

The voltage ripple equation can be calculated as:

$$\Delta V_{OUT} = ESR \cdot \Delta I_{LMAX} + \frac{\Delta I_{LMAX}}{8 \cdot C_{OUT} \cdot f_{SW}} \quad (52)$$

Usually the resistive component of the ripple can be neglected if the selected output capacitor is a multi layer ceramic capacitor (MLCC).

The output capacitor is important also for loop stability: it determines the main pole and the zero due to its ESR. (See Closing the loop to consider its effect in the system stability).

For example with V_{OUT} = 3.3 V, V_{IN} = 12 V, f_{SW} = 500 kHz, ΔI_L = 0.6 A, (resulting by the inductor value) and C_{OUT} = 20 µF MLCC :

$$\frac{\Delta V_{OUT}}{V_{OUT}} \cong \frac{1}{V_{OUT}} \cdot \frac{\Delta I_{LMAX}}{C_{OUT} \cdot f_{SW}} = \left(\frac{1}{3.3} \cdot \frac{0.6}{8 \cdot 20\mu F \cdot 500kHz}\right) = \frac{7.5mV}{3.3} = 0.23\,\% \quad (53)$$

The output capacitor value has a key role to sustain the output voltage during a steep load transient. When the load transient slew rate exceeds the system bandwidth, the output capacitor provides the current to the load. In case the final application specifies high slew rate load transient, the system bandwidth must be maximized and the output capacitor has to sustain the output voltage for time response shorter than the loop response time.

In Table 17. Output capacitors some capacitor series are listed.

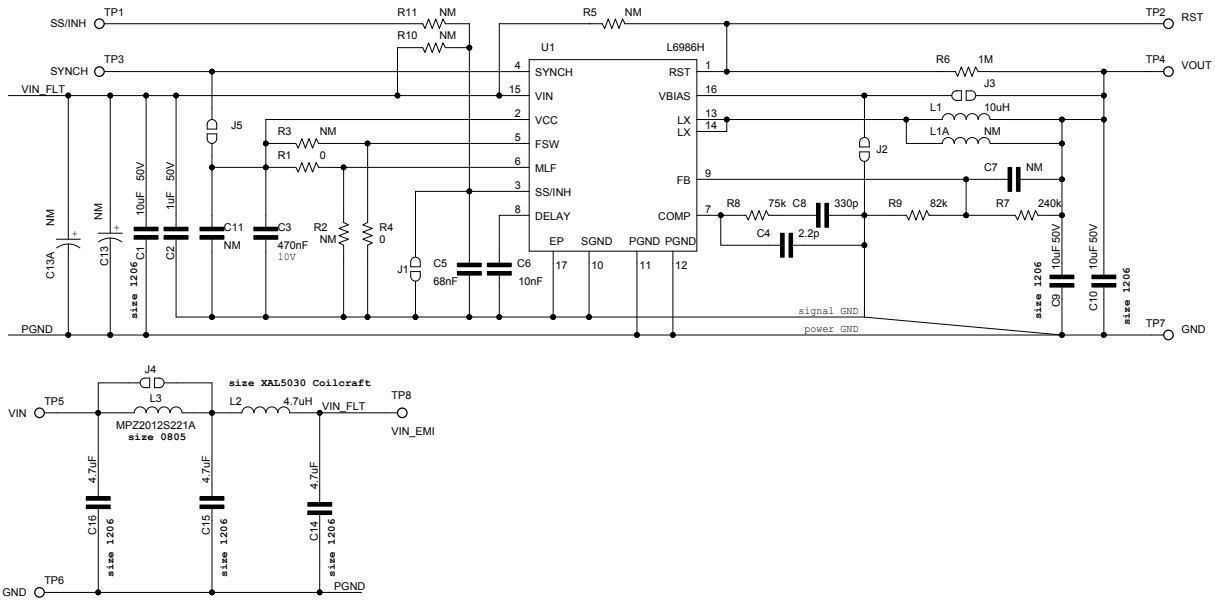
Table 17. Output capacitors

Manufacturer	Series	Cap value (µF)	Rated voltage (V)	ESR (mΩ)
MURATA	GRM32	22 to 100	6.3 to 25	<5
	GRM31	10 to 47	6.3 to 25	<5
PANASONIC	ECJ	10 to 22	6.3	<5
	EEFCD	10 to 68	6.3	15 to 55
SANYO	TPA/B/C	100 to 470	4 to 16	40 to 80
TDK	C3225	22 to 100	6.3	<5

6.7 Application board

The reference evaluation board schematic is shown in the figure below.

Figure 52. Evaluation board schematic



The additional input filter (C16, L3, C15, L2, C14) limits the conducted emission on the power supply (refer to HTSSOP16 package information).

Table 18. **Bill of material (communal parts)**

Reference	Part number	Description	Manufacturer
C1, C9, C10	CGA5L3X5R1H106K	10 µF - 1206 - 50 V - X5R - 10%	TDK
C2	CGA4J3X7R1H105K	1 µF - 0805 - 50 V - X7R - 10%	TDK
C3	-	470 nF - 10 V - 0603	
C4,C7,C8	-	See Table 19. L6986H 3V3 demonstration board BOM, Table 20. L6986H 5V demonstration board BOM, and Table 21. L6986H adj. demonstration board BOM	
C5	-	68 nF - 10 V - 0603	
C6	-	10 nF - 10 V - 0603	
C14, C15, C16	CGA5L3X7R1H475K	4.7 µF - 1206 - 50 V - X7R - 10%	TDK
C11, C13, C13A		Not mounted	
R1, R4		0 Ω - 0603	
R6		1 MΩ - 1%- 0603	
R7, R8, R9		See Table 19. L6986H 3V3 demonstration board BOM, Table 20. L6986H 5V demonstration board BOM, and Table 21. L6986H adj. demonstration board BOM	
R11		10 Ω - 1% - 0603	
R2, R3, R5, R10		Not mounted	
L1	XAL5050-103MEC	10 µH	Coilcraft
L2	XAL4030-472MEC	4.7 µH	Coilcraft
L3	MPZ2012S221A	EMC bead	TDK
J1	Open		
J2	Closed	Switchover disabled	
J3		See Table 19. L6986H 3V3 demonstration board BOM, Table 20. L6986H 5V demonstration board BOM, and Table 21. L6986H adj. demonstration board BOM	
J4	Open		
J5	Open	To adjust the ISKIP current level in LCM operation. Leave open in LNM	
U1	L6986H x-	See Table 19. L6986H 3V3 demonstration board BOM, Table 20. L6986H 5V demonstration board BOM, and Table 21. L6986H adj. demonstration board BOM	ST

Table 19. L6986H 3V3 demonstration board BOM

Reference	Part number	Description	Manufacturer
R7		0 R - 0603	
R9, C7		Not mounted	
R8	-	75 kΩ - 1% - 0603	
C8	-	330 pF - 10 V - 0603	
C4	-	2.2 pF - 10 V - 0603	
J3	Open		
U1	L6986H 3V3	3.3 V internal divider	STM

Table 20. L6986H 5V demonstration board BOM

Reference	Part number	Description	Manufacturer
R7		0 R - 0603	
R9, C7		Not mounted	
R7	-	0 Ω -0603	
R8	-	100 kΩ - 1% - 0603	
C8	-	330 pF - 10 V - 0603	
C4		2.2 pF - 10 V - 0603	
J3	Open		
U1	L6986H 5V	5 V internal divider	STM

Table 21. L6986H adj. demonstration board BOM

Reference	Part number	Description	Manufacturer
R7		240 kΩ - 1% - 0603	
C7		Not mounted	
R9	-	82 kΩ - 1% - 0603	
R8	-	75 kΩ - 1% - 0603	
C8	-	330 pF - 10 V - 0603	
C4		2.2 pF - 10 V - 0603	
J3	Open		
U1	L6986H	External divider (V_{OUT}=3.3 V)	STM

Figure 53. Magnitude bode plot and Figure 54. Phase margin bode plot show the magnitude and phase margin Bode plots related to the BOM of Table 21. L6986H adj. demonstration board BOM.

The small signal dynamic performance in this configuration is:

$$\begin{matrix} BW = 55kHz \\ phase \quad \text{margin} = 60 \circ \end{matrix} \quad (54)$$

Figure 53. **Magnitude bode plot**

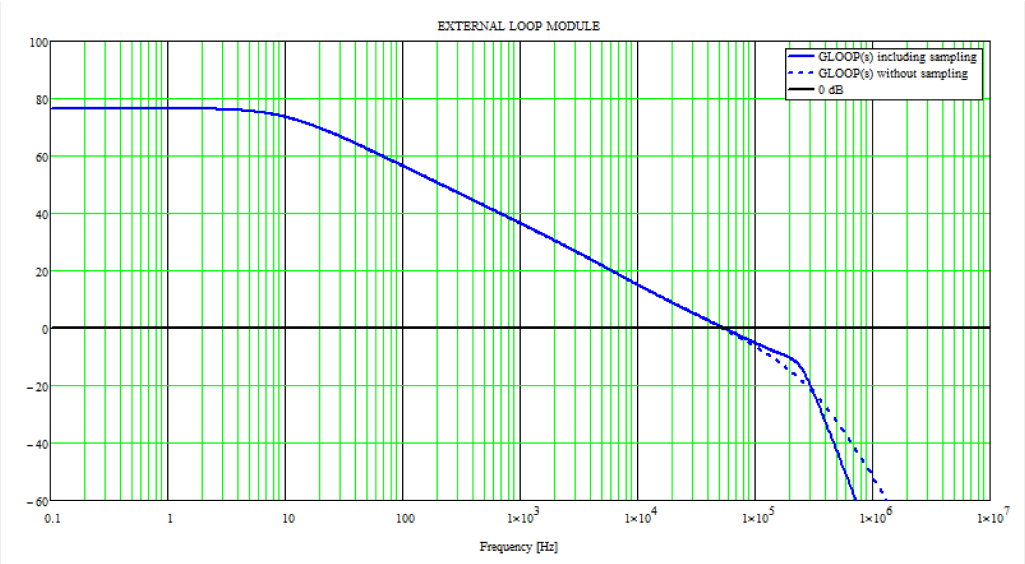


Figure 54. **Phase margin bode plot**

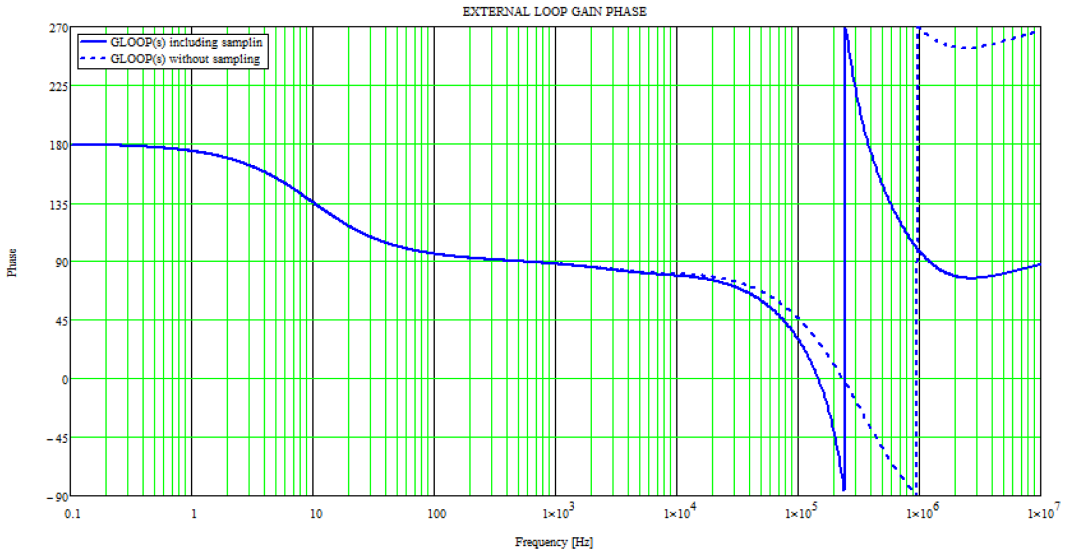


Figure 55. **Top layer**

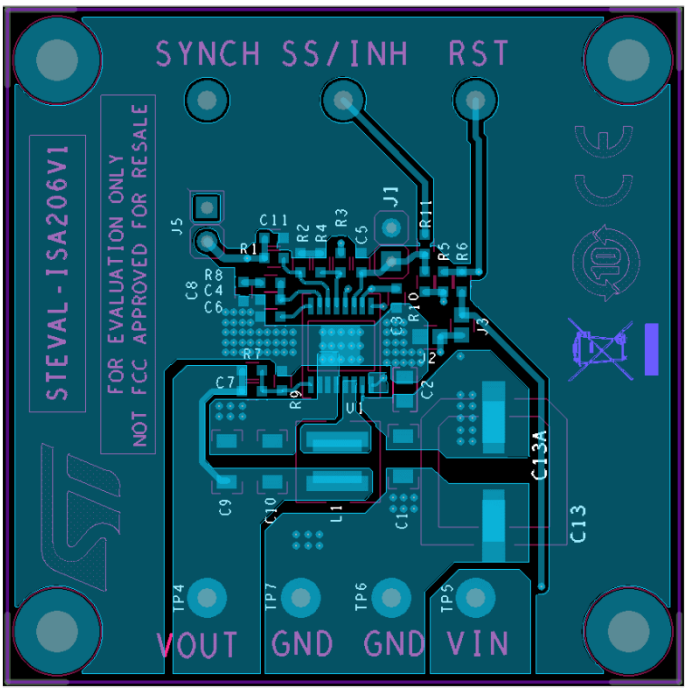
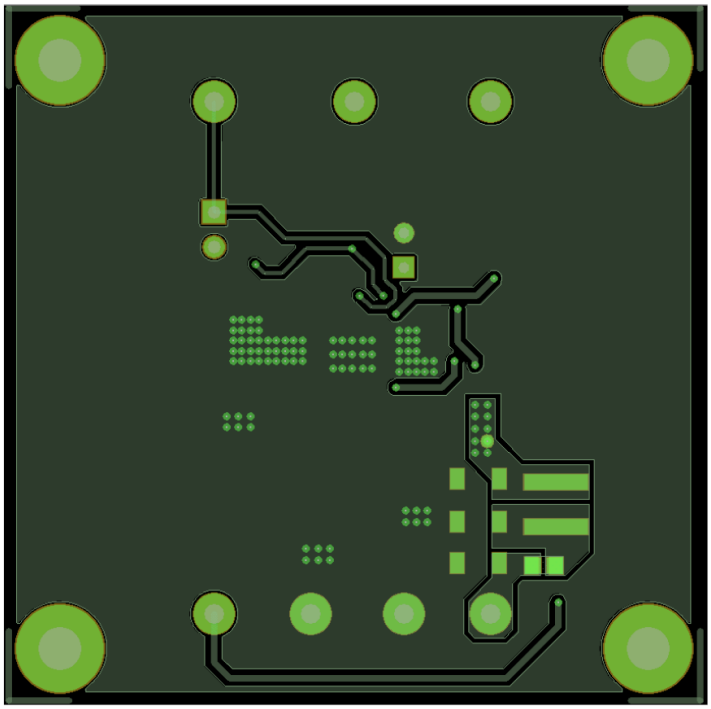


Figure 56. **Bottom layer**



6.8 Efficency curves

Figure 57. Efficiency: V_{IN} = 13.5 V - V_{OUT} = 3.3 V - f_{sw} = 500 kHz

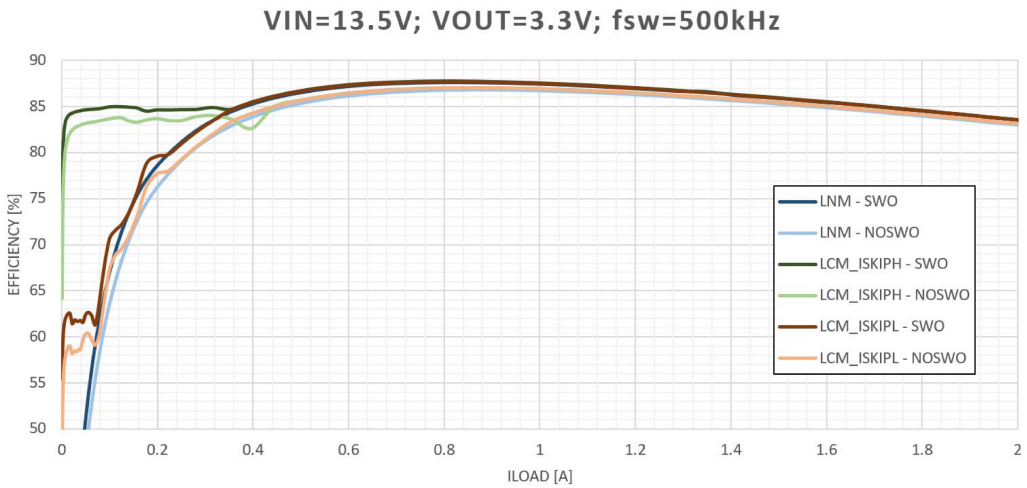


Figure 58. Efficiency: V_{IN} = 13.5 V - V_{OUT} = 3.3 V - f_{sw} = 500 kHz (log scale)

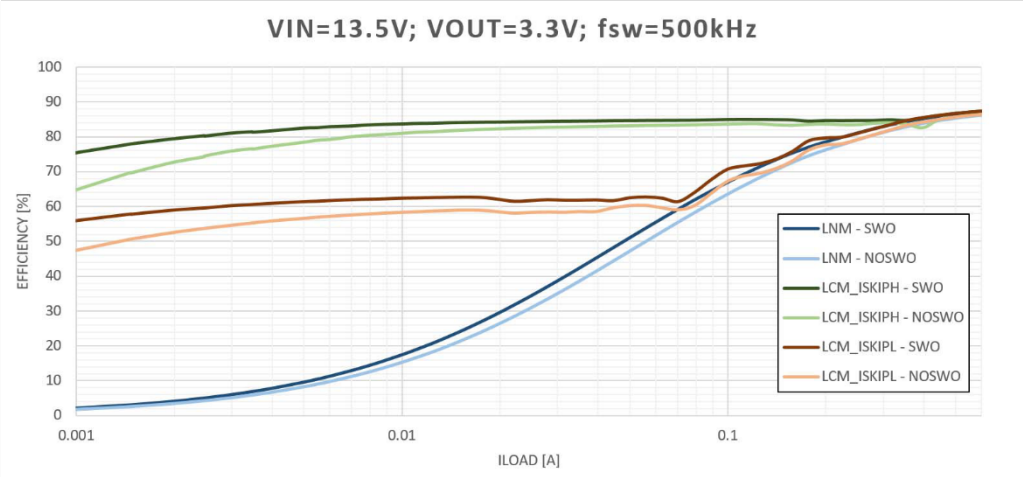


Figure 59. Efficiency: V_{IN} = 13.5 V - V_{OUT} = 5 V - f_{sw} = 500 kHz

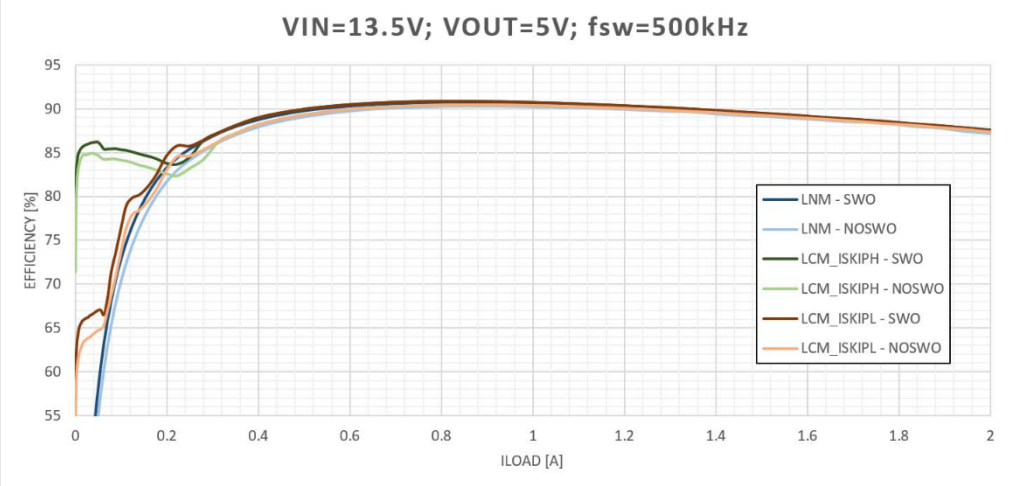


Figure 60. Efficiency: V_{IN} = 13.5 V - V_{OUT} = 5 V - f_{sw} = 500 kHz (log scale)

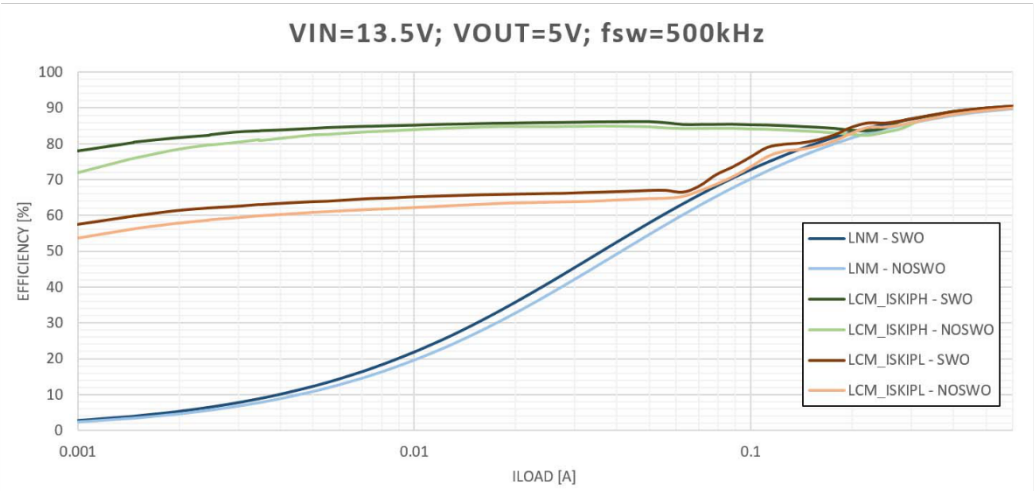


Figure 61. Efficiency: V_{IN} = 24 V - V_{OUT} = 3.3 V - f_{sw} = 500 kHz

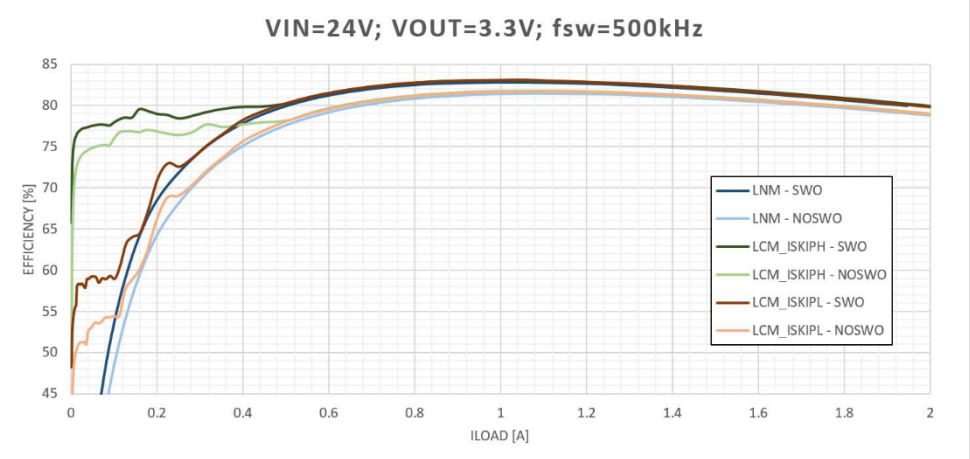


Figure 62. Efficiency: V_{IN} = 24 V - V_{OUT} = 3.3 V - f_{sw} = 500 kHz (log scale)

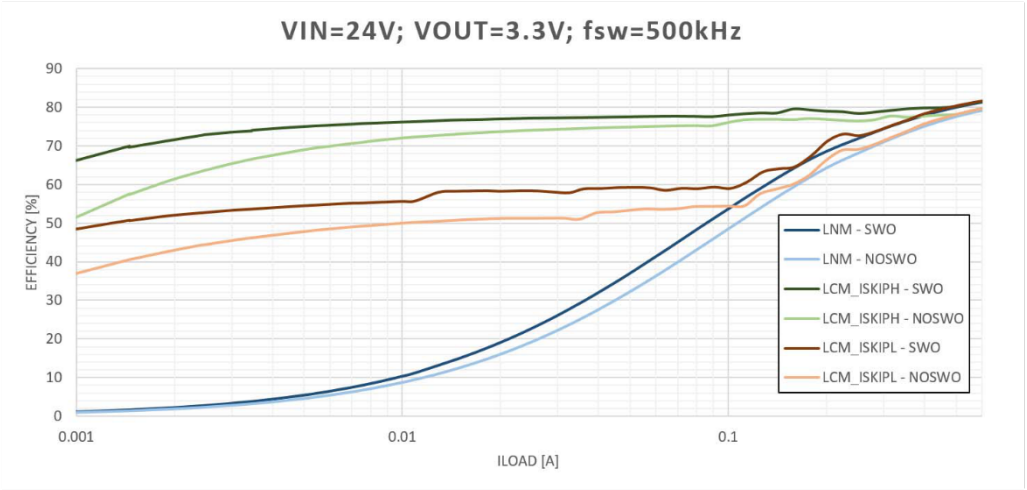


Figure 63. Efficiency: V_{IN} = 24 V - V_{OUT} = 5 V - f_{sw} = 500 kHz

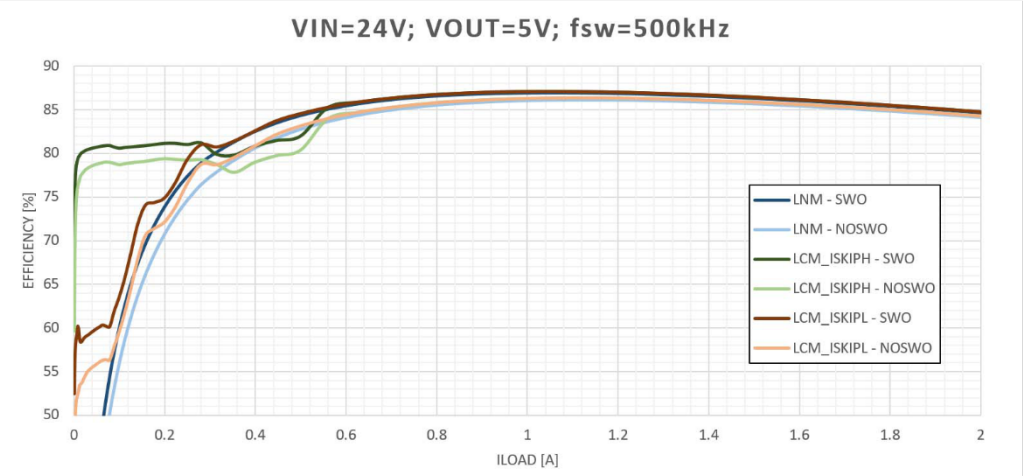
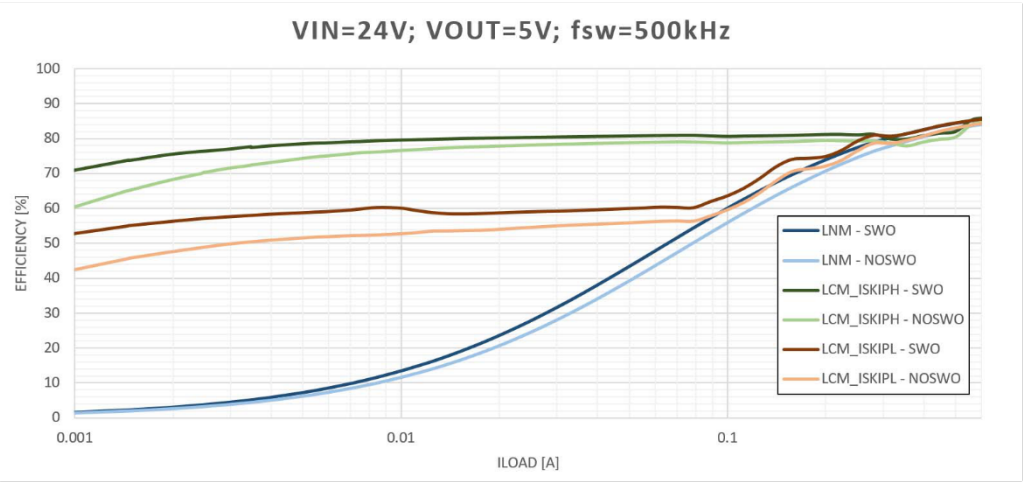


Figure 64. Efficiency: V_{IN} = 24 V - V_{OUT} = 5 V - f_{sw} = 500 kHz (log scale)



7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

7.1 HTSSOP16 package information

Figure 65. HTSSOP16 package outline

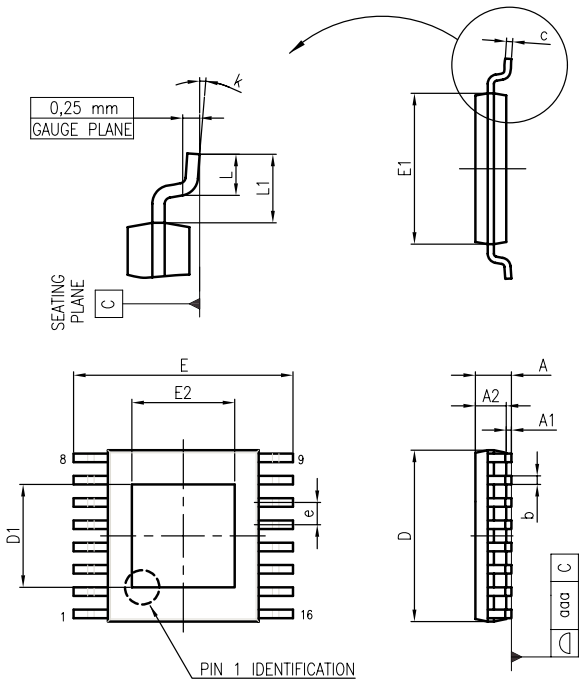


Table 22. **HTSSOP16 mechanical data**

Symbol	mm		
	Min.	Typ.	Max.
A			1.20
A1			0.15
A2	0.80	1.00	1.05
b	0.19		0.30
c	0.09		0.20
D	4.90	5.00	5.10
D1	2.8	3	3.2
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
E2	2.8	3	3.2
e		0.65	
L	0.45	0.60	0.75
L1		1.00	
K	0.00		8.00
aaa			0.10

8 Ordering information

Table 23. **Ordering information**

Part number	Package	Packing
L6986H3V3	HTSSOP16	Tube
L6986H3V3TR		Tape and reel
L6986H5V		Tube
L6986H5VTR		Tape and reel
L6986H		Tube
L6986HTR		Tape and reel

Revision history

Table 24. **Document revision history**

Date	Version	Changes
26-Mar-2019	1	Initial release.
27-Feb-2020	2	Updated $I_{Q\ OPVIN}$ Unit value in Table 5. Electrical characteristics.

Contents

List of tables

List of figures