| PCN Number: | 20181022002.0 PCN Date: October 24, 2018 | | | | | | | | |
|---|---|-------------|-------------------|--------|-----------|-------------|------------------|------------------|--|
| Title: Datasheet for TMP112 | | | | | | | | | |
| Customer Contact: | PCN Manager | | | | Dept: | | | Quality Services | |
| Change Type: | | | | | | | | | |
| Assembly Site | | | Design | | | | Wafer | Bump Site | |
| Assembly Process | | \boxtimes | Data Sheet | | | Wafer | er Bump Material | | |
| Assembly Materials | | | Part number chang | е | | | Wafer | Bump Process | |
| Mechanical Specification | | | Test Site | | | | Wafer | Fab Site | |
| Packing/Shipping/Labeling | | | Test Process | | <u>L</u> | ╛ | | Fab Materials | |
| ☐ Wafer Fab Proces | | | | | | Fab Process | | | |
| Notification Details | | | | | | | | | |
| Description of Change: | | | | | | | | | |
| Texas Instruments Incorporated is announcing an information only notification. | | | | | | | | | |
| The product datasheet(s) is being updated as summarized below. The following change history provides further details. | | | | | | | | | |
| The following change history provides further details. | | | | | | | | | |
| TEXAS INSTRUMENTS TMP112 | | | | | | | | | |
| INSTRUMENTS SBOS473H -MARCH 2009 - REVISED OCTOBER 2018 | | | | | | | | | |
| | | | | | | | | | |
| Changes from Revision G (May 2018) to Revision H Page | | | | | | | | | |
| Added content to the ADD0 pin description in the Pin Functions table | | | | | | | | | |
| Changed the supply voltage maximum value in the Absolute Maximum Ratings table from: 5 V to: 4 V | | | | | | | | | |
| Changed input voltage maximum value for the SCL, ADD0, and SDA pins in the Absolute Maximum Ratings table from: 5 V to: 4 V | | | | | | | | | |
| Changed input voltage maximum value for the ALERT pin in the Absolute Maximum Ratings table from: (V+) + 0.5 V to: ((V+) + 0.5) and ≤ 4 V | | | | | | | | | |
| Changed Junction-to-ambient thermal resistance from 200 °C/W to 210.3 °C/W | | | | | | | | | |
| Changed Junction-to-case (top) thermal resistance from 73.7 °C/W to 105.0 °C/W | | | | | | | | | |
| Changed Junction-to-board thermal resistance from 34.4 °C/W to 87.5 °C/W | | | | | | | | | |
| Changed Junction-to-top characterization parameter from 3.1 °C/W to 6.1 °C/W | | | | | | | | | |
| Changed Junction-to-board characterization parameter from 34.2 °C/W to 87.0 °C/W | | | | | | | | | |
| The datasheet number will be changing. | | | | | | | | | |
| Device Family | | 9111 | | nae Fr | nge From: | | | Change To: | |
| , | , | | SBOS473 | | | | | SBOS473H | |
| 1111 112 | | | | | | | | 350317311 | |
| These changes may be reviewed at the datasheet links provided. | | | | | | | | | |
| http://www.ti.com/product/TMP112 | | | | | | | | | |
| Reason for Change: | | | | | | | | | |
| To accurately reflect device characteristics. | | | | | | | | | |
| Anticipated impact on Fit, Form, Function, Quality or Reliability (positive / negative): | | | | | | | | | |
| No anticipated impact. This is a specification change announcement only. There are no changes to | | | | | | | | | |
| the actual device. | | | | | | | | | |
| Changes to product identification resulting from this PCN: | | | | | | | | | |
| None. | | | | | | | | | |
| Product Affected: | TMD1124 | D.C | TMD442D | TDD: 2 | | | T | MD112DIDDLT | |
| TMP112AIDRLR | TMP112AI | | | INKLK | | | | MP112BIDRLT | |
| TMP112NAIDRLR | TMP112NA | AID | RLT | | | | | | |

For questions regarding this notice, e-mails can be sent to the regional contacts shown below or your local Field Sales Representative.

| Location | E-Mail |
|--------------|--------------------------------|
| USA | PCNAmericasContact@list.ti.com |
| Europe | PCNEuropeContact@list.ti.com |
| Asia Pacific | PCNAsiaContact@list.ti.com |
| Japan | PCNJapanContact@list.ti.com |