SmartLEWIS™ RX+

TDA5240 Family

Enhanced Sensitivity Multi-Configuration Receiver

Technical Selection Guide

Application Note

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TDA5240 Family Enhanced Sensitivity Multi-Configuration Receiver

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1 Overview and General Comparison

This is a simple technical guideline for selecting the best matching member out of the SmartLEWIS TDA5240 family for your application.

The TDA5240 family consists of 3 chip sets:

- TDA5240 is the superset of this family and supports the autonomous receive mode, where the desired payload is automatically extracted and interrupts can trigger the host microcontroller to read the payload from the FIFO.
- TDA5235 has some minor restrictions compared to TDA5240:
  - TDA5235 is only capable of two independent configuration sets, while TDA5240 has four independent configuration sets.
  - TDA5235 is able to support only one RF channel within each configuration set, while TDA5240 can handle up to three RF channels per configuration sets.
- TDA5225 does not support the autonomous receive mode:
  - Only the transparent receive data is available.
  - A decision on valid data and a Clock-Data-Recovery must be applied in the application controller.
  - Payload extraction needs to be done in the application controller.

A short overview on the available features is shown in the general comparison matrix in **Figure 1**.

	High Sensitivity	Multi-Channel	Manchester Decoding	NRZ Slicer Output	Frame Sync	Digital Decoding	IF Filter integrated	5V Pads
TDA5240	X	X	X	X	X	X	X	X
TDA5235	X		X	X	X	X	X	X
TDA5225	X	X		X			X	X

Figure 1 General Comparison Matrix

Figure 2 is comparing the key features of the RF/IF system.

	TDA5225	TDA5235	TDA5240
Sensitivity (FSK, 2 kbit/s, fdev = +/- 10 kHz, BER=$2*10^{-3}$)	- 119 dBm	- 119 dBm	- 119 dBm
Sensitivity (ASK, 2 kbit/s, BER=$2*10^{-3}$)	-116 dBm Peak	-116 dBm Peak	-116 dBm Peak
PLL Type	ΣΔ PLL	ΣΔ PLL	ΣΔ PLL
Multi-Channel Resolution	Fine: 10.5 Hz	Fine: 10.5 Hz	Fine: 10.5 Hz
Receiver Type	Single/Double conversion	Single/Double conversion	Single/Double conversion
IF Frequency	10.7 MHz 274 kHz	10.7 MHz 274 kHz	10.7 MHz 274 kHz
Channel Bandwidth	50 - 300 kHz (on- chip filter) + ext. CER filter	50 - 300 kHz (on- chip filter) + ext. CER filter	50 - 300 kHz (on- chip filter) + ext. CER filter

Figure 2 RF/IF System Comparison

Detailed differences in the digital baseband processing can be seen in **Figure 3**.

	TDA5225	TDA5235	TDA5240
Max. FSK Data Rate	112 kchip/s	112 kchip/s	112 kchip/s
Max. ASK Data Rate	40 kchip/s	40 kchip/s	40 kchip/s
Number of Configurations	4	2	4
Number of RF channels per Configuration	3	1	3
Sliced baseband output (simple slicer allows NRZ processing externally)	•	•	•
Digital Slicer in Digital Baseband	(•) simple slicer only	•	•
Manchester Code (ClkRecovery)		•	•
Bi- phase Code (ClkRecovery)		•	•
Frame Synchronization Unit (TSI)		•	•
FIFO size		256 bits	256 bits
Self Polling Mode	(•) Const ON-OFF only	•	•
Fast Wake up on RSSI	•	•	•
Wake- up Generator + Wake -up Interrupt Generator	(•) simple RSSI- WU only	•	•
Interrupt Generation for Fsync, MID and EOM		•	•
RX_RUN and CLK_OUT output	•	•	•
SPI Interface	• @ 2.2MHz	• @ 2.2MHz	• @ 2.2MHz
Current consumption	12 mA	12 mA	12 mA

Figure 3 Baseband Comparison

2 Different System Approaches

For the TDA5225, only the DATA or DATA_MATCHFIL output signal can be used (transparent mode; see **Figure 4**). BER sensitivity measurements, as noted in the data sheet, use the transparent receive mode TMMF (DATA_MATCHFIL output signal), where the received data is sampled with ideal data clock. The DATA_MATCHFIL output signal will provide higher systematic jitter than the DATA output signal.

Please keep in mind, that Sensitivity in this transparent mode is significantly depending on the implemented clock and data recovery algorithm of the user software in the application controller.

TDA5235/40 can deliver high sensitivity due to internal available multi-bit signals (TDA5225 only delivers a 1-bit output signal) and a real hardware clock-recovery unit.

The autonomous receive mode of a TDA5235/40, where the host controller can stay in idle mode, leads to reduced noise of the application controller and improved system performance. Therefore the system standby power consumption can be further reduced. Especially the usage of TDA5235/40 features like Fast-Fallback or Ultrafast-Fallback further reduces the receivers On time, which has direct influence to the average current consumption.

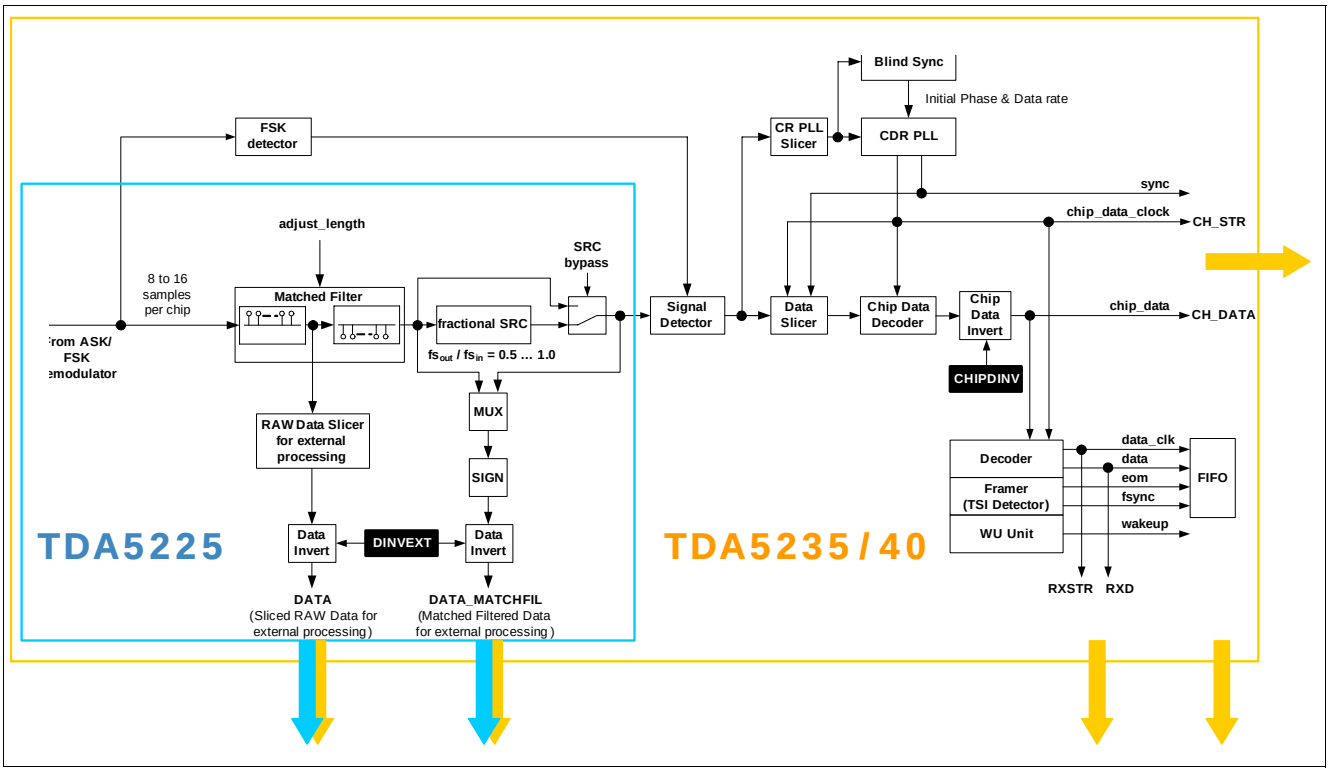

Figure 4 Output Sources of Digital Receiver

A typical TDA5225 application is shown in **Figure 5**, where the application controller is recovering clock and data.

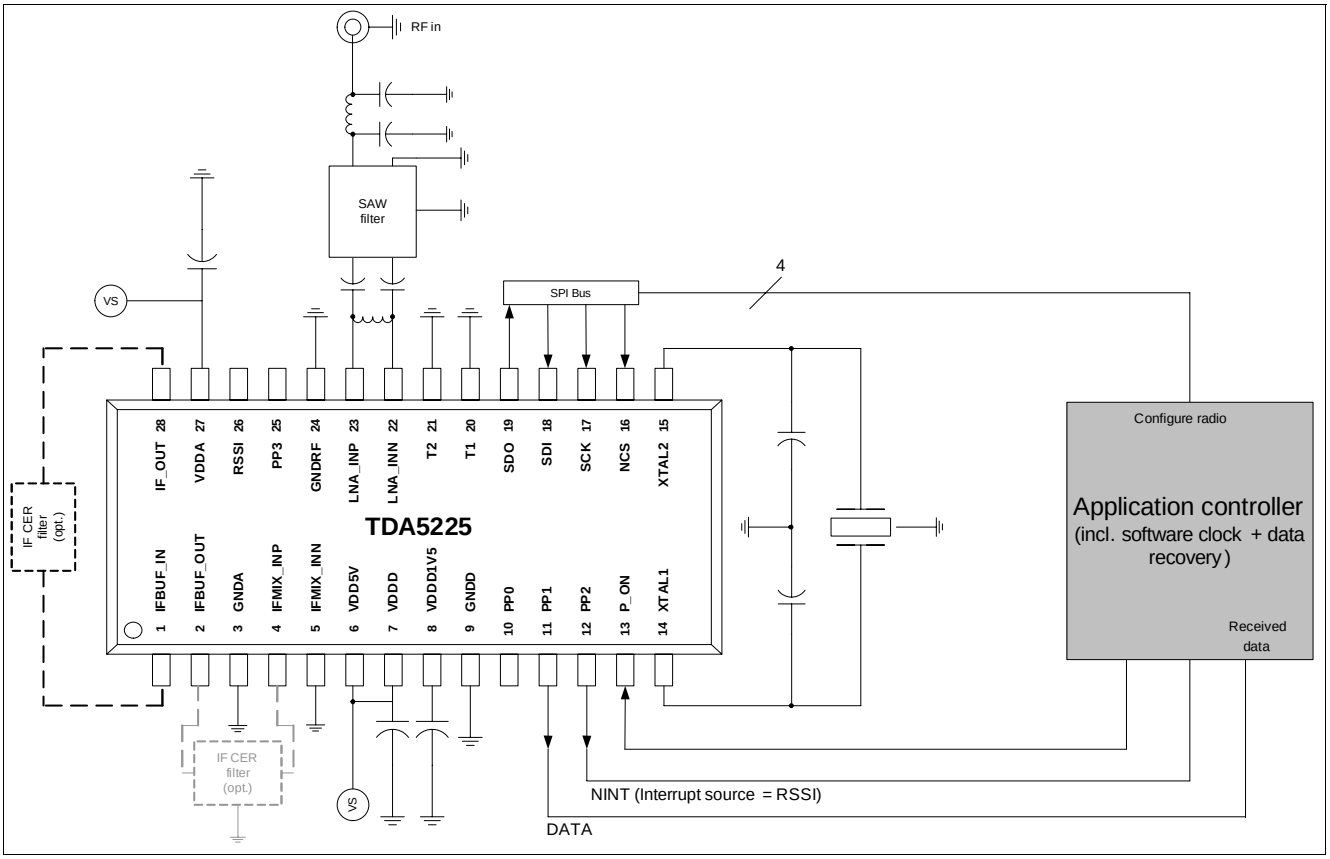

Figure 5 Typical TDA5225 Application

A power-up and start-up sequence can look like the following (Power OFF ==> DATA output):

- Power Off (P_ON = 0)
  - No RF reception is required
- Power On (P_ON = 1)
  - Initiated by application controller
  - TDA5225 has finished after 3ms in maximum (t_{Reset}, see item C9 in data sheet)
- SLEEP mode is reached (but registers are not configured for the application)
- SPI communication required to configure TDA5225 for the target application after (each) Power On cycle.
  - Required configuration time is depending on SPI speed and number of registers to configure; last command is setting the TDA5225 into Run Mode
- Run Mode
  - After 460µs (typical) the TDA5225 is ready to receive;
  - Wait for Data processing delay and Raw Data Slicer settling time
- Data at DATA output can be used for processing in the application controller

Note: After a successful start-up, also a receiver polling (on-off duty cycle) can be applied either with the built-in Self Polling feature or by switching between Run Mode Slave and Sleep Mode. In both cases the register content of the radio stays preserved.

A typical TDA5235/40 application is shown in **Figure 6**, where the application controller is only waiting for an interrupt to readout the received payload from the FIFO.

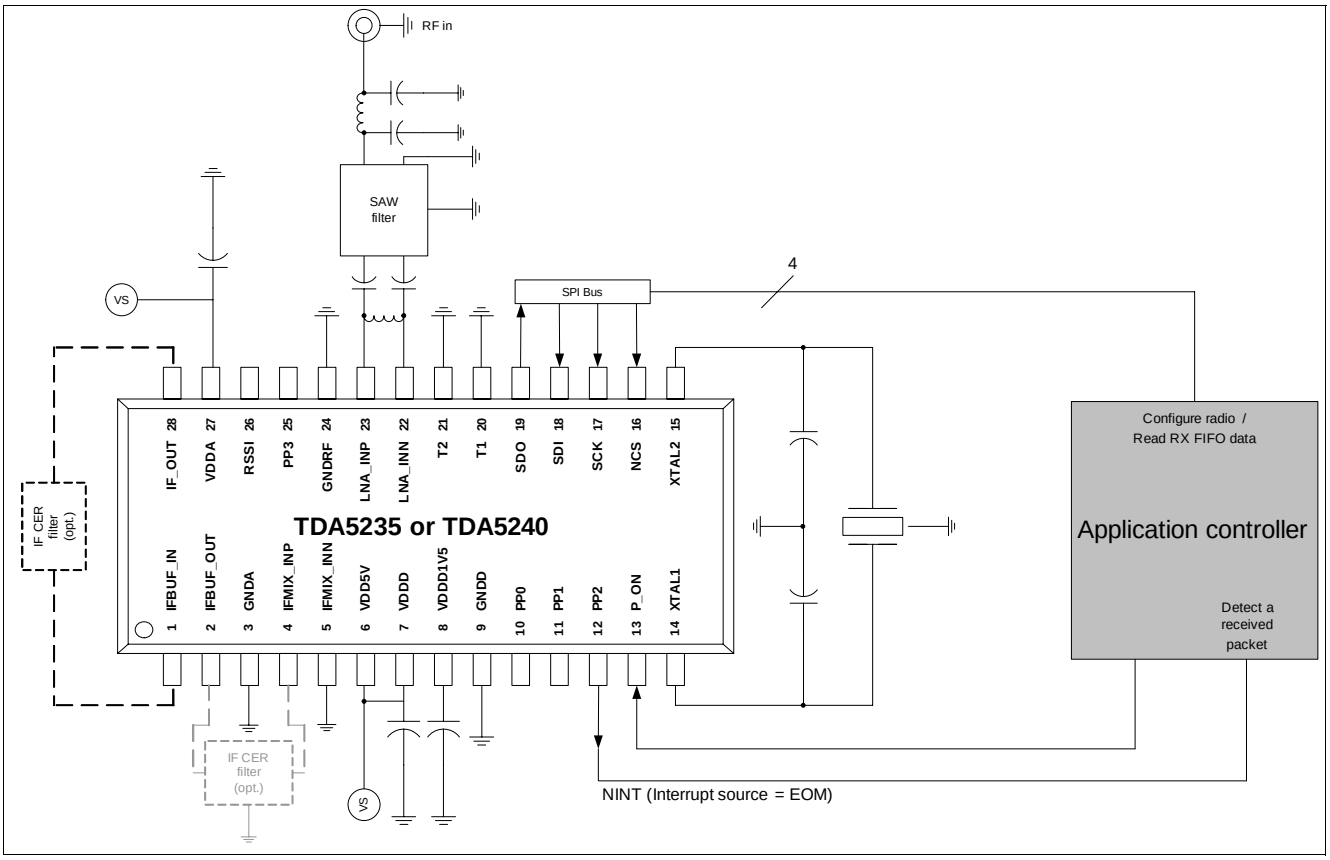

Figure 6 Typical TDA5235/40 Application

The power-up and start-up sequence can look like the following (Power OFF ==> ready to receive):

- Power Off (P_ON = 0)
  - No RF reception is required
- Power On (P_ON = 1)
  - Initiated by application controller
  - TDA5235/40 has finished after 3ms in maximum (t_{Reset}, see item C9 in data sheet)
- SLEEP mode is reached (but registers are not configured for the application)
- SPI communication required to configure TDA5235/40 for the target application after the Power On cycle.
  - Required configuration time is depending on SPI speed and number of registers to configure; last command is setting the TDA5235/40 either into Run Mode Slave or Self Polling Mode (In both cases the register content of the radio stays preserved).
- Run Mode Slave (similar is valid for Self Polling Mode)
  - After 460µs (typical) the TDA5235/40 is ready to receive;
  - The receiver is scanning autonomously for the target data and if successful, the application controller gets informed (NINT) to pick data from the FIFO via SPI.
- Self Polling Mode
  - Additionally, the receiver is automatically polling (on-off duty cycle) to further reduce the average current consumption.

3 Overall System Current Consumption

The current consumption of TDA5225 and TDA5235/40 are equal.

In a TDA5225 system the RAW Data Slicer settling time needs to be taken into account for the average current consumption.

A system using the TDA5225 will have a higher overall system current consumption, as an additional current is required for the „high performance“ software clock recovery in the application controller.

Features like FFB or UFFB are only available in TDA5235/40, but not in TDA5225. Therefore the decision on valid data must be taken by the application controller, which must stay ON for the „whole“ time of reception and consumes current at this time.

TDA5225 only has RSSI criterion for Wake-up (WU) generation. This is the weakest WU criterion and will lead to False-Alarms (= unnecessary wake-ups of the application controller) as an appropriate RSSI threshold needs to be set for not losing sensitivity (please note that RSSI shows a slight temperature dependency, which needs to be taken into account).

Therefore the overall system current consumption using a TDA5225 will always be higher compared to a system using a TDA5235 or TDA5240.

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