MITSUBISHI ELECTRIC

<DIPIPM>

MOSFET Super mini DIPIPM APPLICATION NOTE
PSM03S93E5-A / PSM05S93E5-A

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CHAPTER 1 INTRODUCTION

1.1 Features of MOSFET Super mini DIPIPM

MOSFET Super mini DIPIPM (hereinafter called DIPIPM) is the transfer molding type intelligent power module (IPM) which integrates power chips, drive and protection circuits in one package. It is favorable for AC100-240Vinput class low power motor inverter control. Since DIPIPM integrates MOSFET as switching power chip, it can realize low loss at low current operation. And also it has insulated sheet structure with very low thermal resistance and ultra small package. Thanks to them, it is most suitable for inverterized refrigerator, which continues to operate for long time at ultra low current. Main features of DIPIPM are as below.

- ***MOSFET are integrated for improving efficiency at low current.***
- ***Incorporating bootstrap diode with current limiting resistor for P-side gate driving supply***
- ***Easy to replace from current Ver.5 due to same pin compatibility and package***

Fig.1-1-1 and Fig.1-1-2 show the outline and internal cross-section structure respectively.

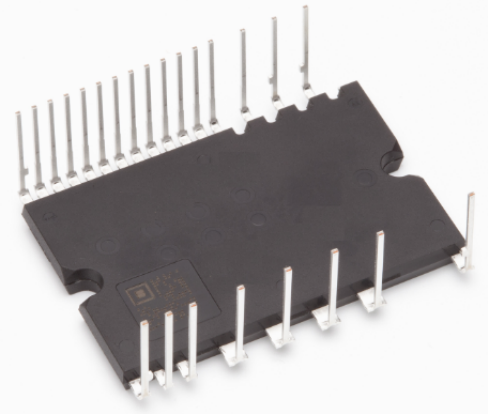


Fig.1-1-1 Package photograph

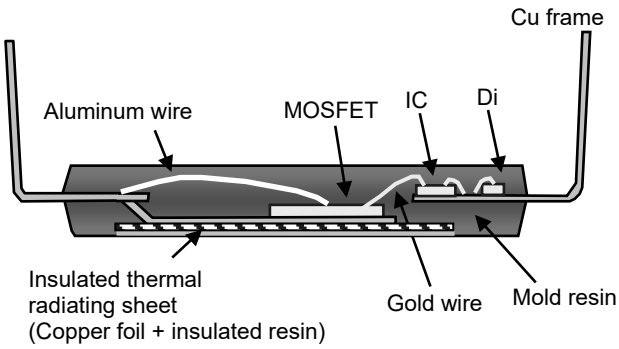


Fig.1-1-2 Internal cross-section structure

1.2 Functions

MOS DIPIPM has following functions and inner block diagram is described in Fig.1-2-1.

- For P-side:
  - Drive circuit;
  - High voltage level shift circuit;
  - Control supply under voltage (UV) lockout circuit (without fault signal output).
  - Built-in bootstrap diode (BSD) with current limiting resistor
- For N-side:
  -Drive circuit;
  -Short circuit (SC) protection circuit (by inserting external shunt resistor into main current path)
  -Control supply under voltage (UV) lockout circuit (with fault signal output)
  -Over temperature (OT) protection by monitoring LVIC temperature.
- Fault Signal Output
  -Corresponding to N-side MOSFET SC, N-side UV and OT protection.
- MOSFET Drive Supply
  -Single DC15V power supply (in the case of using bootstrap method)
- Control Input Interface
  -Schmitt-triggered 3V,5V input compatible, high active logic.
- UL recognized : UL1557 File E323585

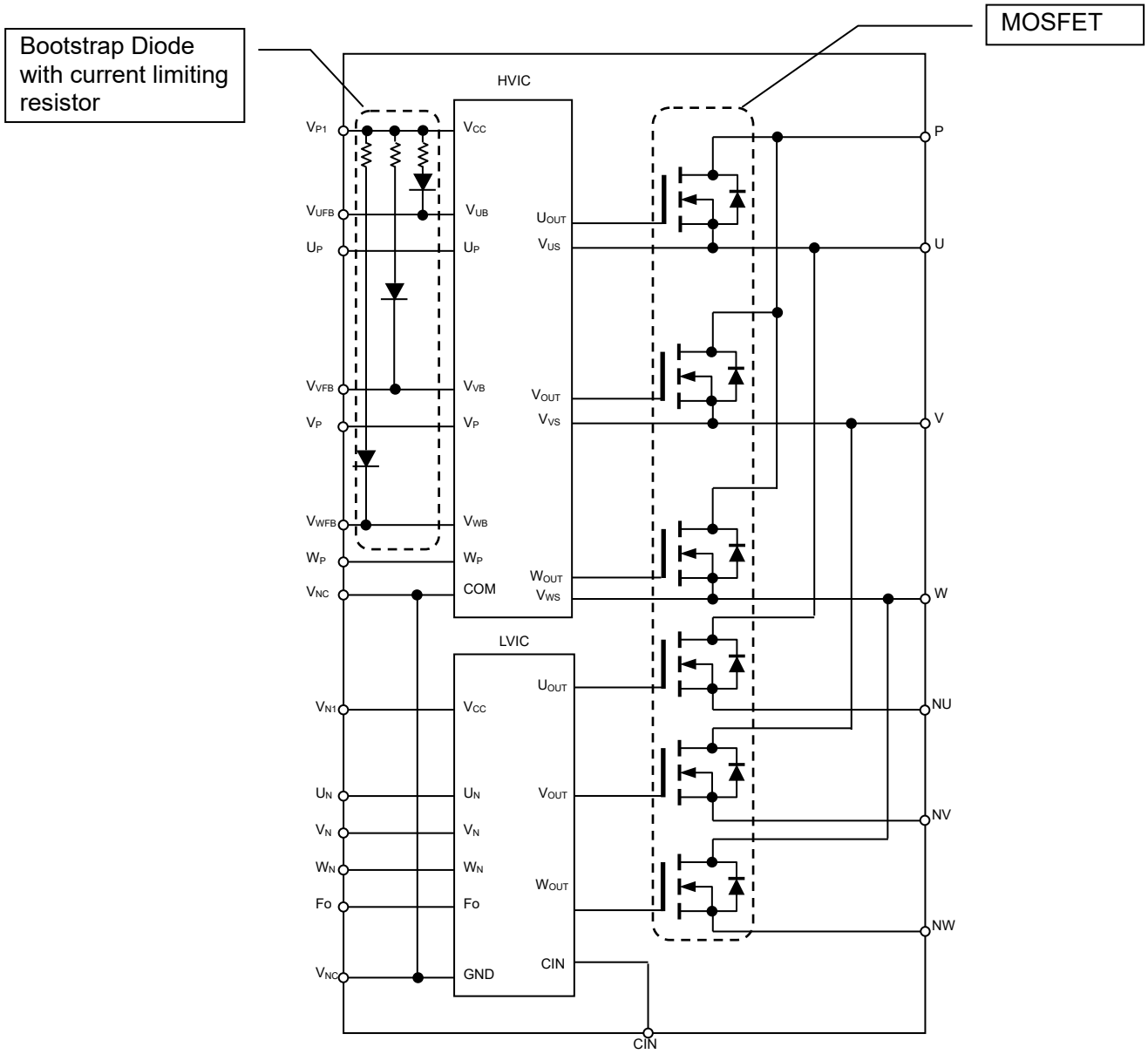


Fig.1-2-1 Inner block diagram

1.3 Target Applications

Motor drives for household electric appliances, such as refrigerators
Low power industrial motor drive such a small fan control except automotive applications

1.4 Product Line-up

Table 1-4-1 MOS DIPIPM Line-up

Type Name (Note 1)	MOSFET Rating	Motor Rating (Note 2)	Isolation Voltage
PSM03S93E5-A	3A/500V	0.2kW/220VAC	V_{iso} = 1500Vrms (Sine 60Hz, 1min All shorted pins-heat sink)
PSM05S93E5-A	5A/500V	0.4kW/220VAC	

Note 1: Suffix 'A' indicates long pin shape. Please refer to chapter 2 for details.
Note 2: The motor ratings are simulation results. It will vary by operation conditions.

CHAPTER 2 SPECIFICATIONS AND CHARACTERISTICS

2.1 MOSFET Super mini DIPIPM Specifications

MOS DIPIPM specifications are described below by using PSM05S93E5 (5A/500V) as an example. Please refer to respective datasheet for the detailed description of other types.

2.1.1 Maximum Ratings

The maximum ratings of PSM05S93E5 are shown in Table 2-1-1.

Table 2-1-1 Maximum Ratings

INVERTER PART

Symbol	Parameter	Condition	Ratings	Unit	
V_{DD}	Supply voltage	Applied between P-NU,NV,NW	400	V	(1)
$V_{DD(surge)}$	Supply voltage (surge)	Applied between P-NU,NV,NW	450	V	(2)
V_{DSS}	Drain-source voltage		500	V	(3)
$\pm I_D$	Each MOSFET drain current	T_C= 25°C (Note 1)	5	A	(4)
$\pm I_{DP}$	Each MOSFET drain current (peak)	T_C= 25°C, less than 1ms	10	A	
P_D	Drain dissipation	T_C= 25°C, per 1 chip	35.7	W	
T_{ch}	Channel temperature	(Note2)	-20~+150	°C	(5)

Note1: Pulse width and period are limited due to channel temperature.
Note2: The maximum channel temperature rating of built-in power chips is 150°C(@Tc≤100°C).However, to ensure safe operation of DIPIPM, the average channel temperature should be limited to Tch(Ave)≤125°C (@Tc≤100°C).

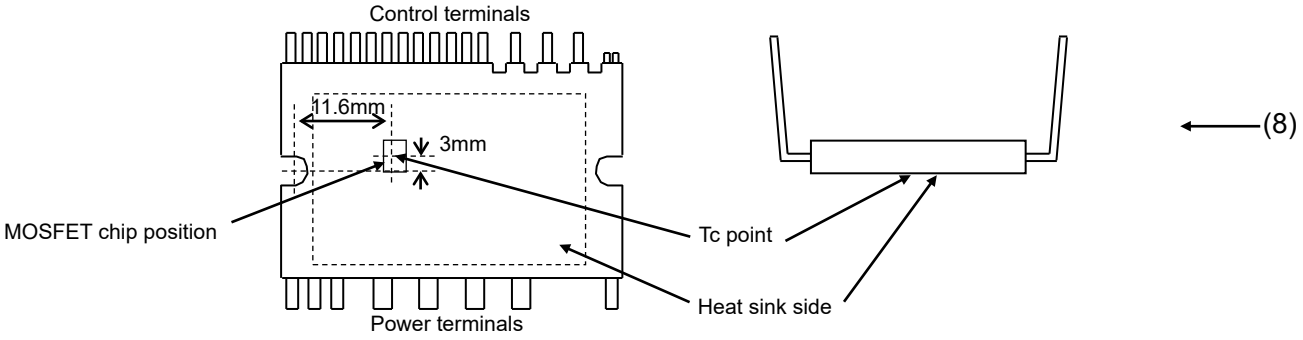
CONTROL (PROTECTION) PART

Symbol	Parameter	Condition	Ratings	Unit
V_D	Control supply voltage	Applied between V_{P1}-V_{NC}, V_{N1}-V_{NC}	20	V
V_{DB}	Control supply voltage	Applied between V_{UFB}-U, V_{VFB}-V, V_{WFB}-W	20	V
V_{IN}	Input voltage	Applied between U_P, V_P, W_P-V_{PC}, U_N, V_N, W_N-V_{NC}	-0.5~V_D+0.5	V
V_{FO}	Fault output supply voltage	Applied between F_O-V_{NC}	-0.5~V_D+0.5	V
I_{FO}	Fault output current	Sink current at F_O terminal	1	mA
V_{SC}	Current sensing input voltage	Applied between CIN-V_{NC}	-0.5~V_D+0.5	V

TOTAL SYSTEM

Symbol	Parameter	Condition	Ratings	Unit	
$V_{DD(PROT)}$	Self protection supply voltage limit (Short circuit protection capability)	V_D = 13.5~16.5V, Inverter Part Tch = 125°C, non-repetitive, less than 2μs	400	V	(6)
T_C	Module case operation temperature	Measurement point of Tc is provided in Fig.1	-20~+100	°C	
T_{stg}	Storage temperature		-40~+125	°C	
V_{iso}	Isolation voltage	60Hz, Sinusoidal, AC 1min, between connected all pins and heat sink plate	1500	V_{rms}	(7)

Tc measurement position



(1) V_{DD} Maximum voltage can be biased between P-N. A voltage suppressing circuit such as a brake circuit is necessary if P-N voltage exceeds this value.

(2) $V_{DD(surge)}$ Maximum P-N surge voltage in switching state. If P-N voltage exceeds this voltage, a snubber circuit is necessary to absorb the surge so that the surge voltage is kept under this voltage.

(3) V_{DSS} Maximum sustained drain-source voltage of built-in MOSFET

(4) $\pm I_D$ Allowable DC current flowing at drain electrode (Tc=25°C) Pulse width and period are limited due to junction temperature T_{ch}.

(5) Tch Maximum channel temperature rating is 150°C.But for safe operation, it is recommended to limit the average channel temperature up to 125°C. Repetitive temperature variation ΔTch affects life time of power cycle.

(6) $V_{DD(PROT)}$ Maximum supply voltage for turning off MOSFET safely in the case of an SC or OC fault. The power chip might be damaged if supply voltage exceeded this specification.

(7) Isolation voltage Isolation voltage of Super mini DIPIPM is the voltage between all shorted pins and copper surface of DIPIPM. The maximum rating of isolation voltage of Super mini DIPIPM is 1500Vrms. But if such as convex shape heat radiation fin will be used for enlarging clearance between outer terminals and heat radiation fin (2.5mm or more is recommended), it is able to correspond isolation voltage 2500Vrms. Super mini DIPIPM is recognized by UL at the condition 2500Vrms with convex shape heat radiation fin.

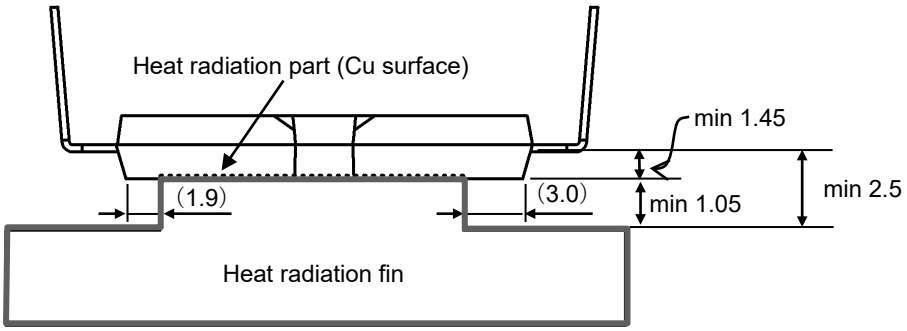


Fig.2-1-1 In the case of using convex fin (unit: mm)

(8) Tc position Tc (case temperature) is defined to be the temperature just beneath the specified power chip. Please mount a thermocouple on the heat sink surface at the defined position to get accurate temperature information. Due to the control schemes such different control between P and N-side, there is the possibility that highest Tc point is different from above point. In such cases, it is necessary to change the measuring point to that under the highest power chip.

[Power chip position]
Fig.2-1-2 indicates the position of the each power chips. (This figure is the view from laser marked side.)

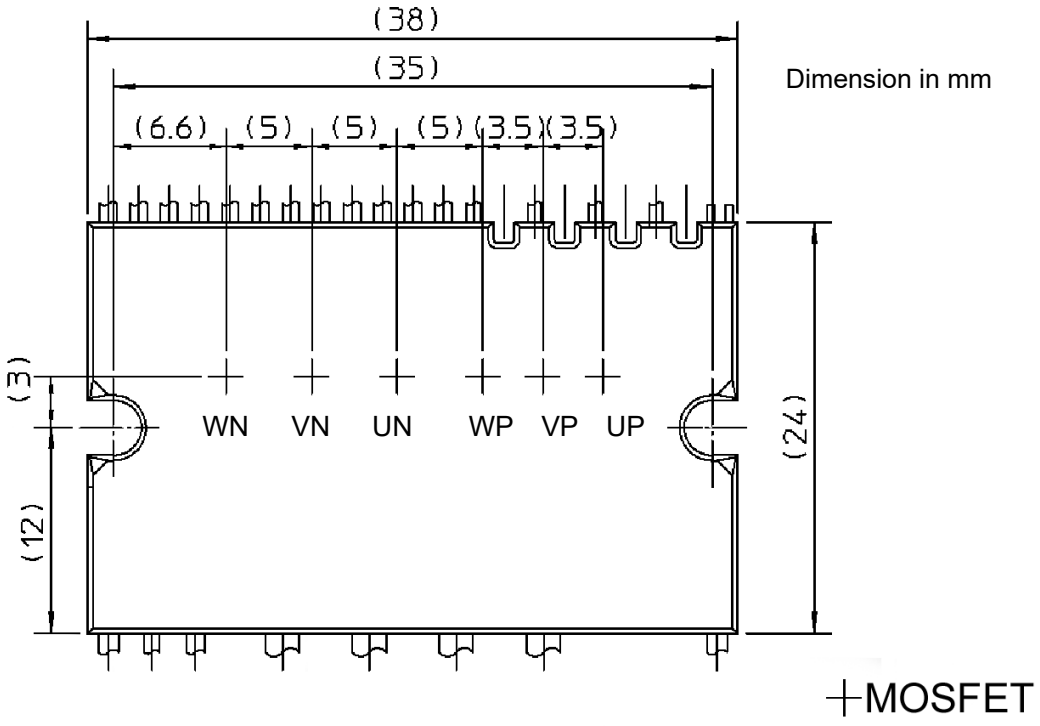


Fig.2-1-2 Power chip position

2.1.2 Thermal Resistance

Table 2-1-2 shows the thermal resistance of PSM05S93E5.

Table 2-1-2 Thermal resistance of PSM05S93E5

THERMAL RESISTANCE

Symbol	Parameter	Condition	Limits			Unit
			Min.	Typ.	Max.	
$R_{th(ch-c)Q}$	Junction to case thermal resistance (Note)	1/6 module	-	-	2.8	K/W

Note : Grease with good thermal conductivity and long-term endurance should be applied evenly with about +100μm~+200μm on the contacting surface of DIPIPM and heat sink. The contacting thermal resistance between DIPIPM case and heat sink Rth(c-f) is determined by the thickness and the thermal conductivity of the applied grease. For reference, Rth(c-f) is about 0.3K/W (per 1/6 module, grease thickness: 20μm, thermal conductivity: 1.0W/m•k).

The above data shows the thermal resistance between chip channel and case at steady state. The thermal resistance goes into saturation in about 10 seconds. The unsaturated thermal resistance is called as transient thermal impedance which is shown in Fig.2-1-3. Zth(j-c)* is the normalized value of the transient thermal impedance. (Zth(j-c)*= Zth(j-c) / Rth(j-c)max)

For example, the MOSFET transient thermal impedance of PSM05S93E5 in 0.3s is 2.8×0.8=2.2K/W.

The transient thermal impedance isn't used for constantly current, but for short period current (ms order). (e.g. In the cases at motor starting, at motor lock・・・)

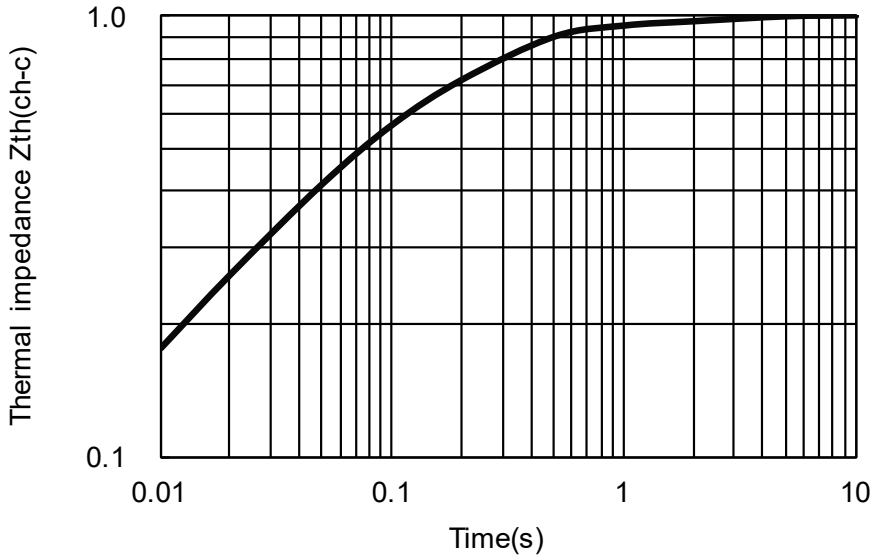


Fig.2-1-3 Typical transient thermal impedance

2.1.3 Electric Characteristics and Recommended Conditions

Table 2-1-3 shows the typical static characteristics and switching characteristics of PSM05S93E5.

Table 2-1-3 Static characteristics and switching characteristics of PSM05S93E5

INVERTER PART (Tch = 25°C, unless otherwise noted)

Symbol	Parameter	Condition		Limits			Unit
				Min.	Typ.	Max.	
$V_{DS(on)}$	Drain-source on-state resistance	V_D=V_{DB} = 15V, V_{IN}= 5V, I_D= 5A	Tch= 25°C	-	0.60	0.80	Ω
			Tch= 125°C	-	1.30	1.70	
V_{SD}	Source-drain voltage drop	V_{IN}= 0V, -I_D= 5A		-	0.90	1.30	V
t_{on}	Switching times	V_{DD}= 300V, V_D= V_{DB}= 15V I_D= 5A, Tch= 125°C, V_{IN}= 0↔5V Inductive Load (upper-lower arm)		0.65	1.15	1.65	μs
$t_{C(on)}$				-	0.35	0.55	μs
t_{off}				-	1.00	1.50	μs
$t_{C(off)}$				-	0.10	0.20	μs
t_{rr}				-	0.25	-	μs
I_{DSS}	Drain-source cut-off current	V_{DS}=V_{DSS}	Tch= 25°C	-	-	1	mA
			Tch= 125°C	-	-	10	

Switching time definition and performance test method are shown in Fig.2-1-4 and 2-1-5.
Switching characteristics are measured by half bridge circuit with inductance load.

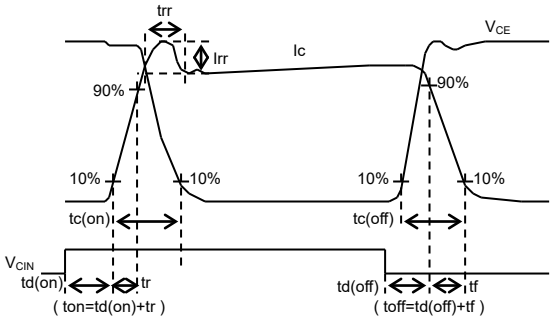


Fig.2-1-4 Switching time definition

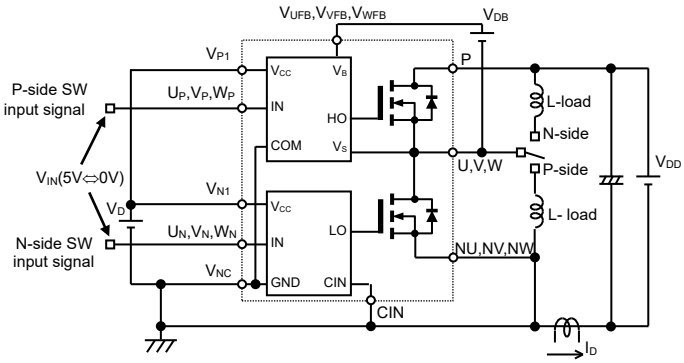


Fig.2-1-5 Evaluation circuit (inductive load)
Short A for N-side MOSFET, and short B for P-side MOSFET evaluation

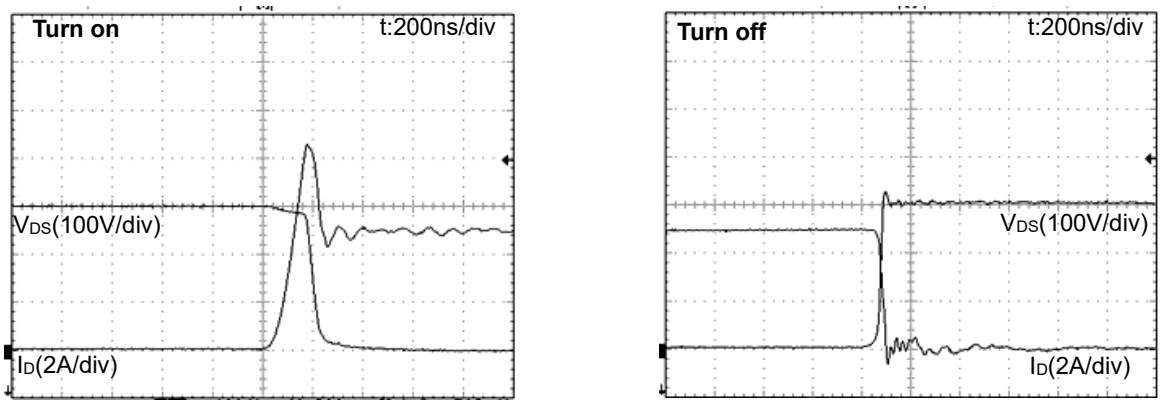


Fig.2-1-6 Typical switching waveform (PSM05S93E5)
Conditions: V_{DD}=300V, V_D=V_{DB}=15V, Tch=25°C, I_D=5A, Inductive load half-bridge circuit

Table 2-1-4 shows the typical control part characteristics of PSM05S93E5.

Table 2-1-4 Control (Protection) characteristics of PSM05S93E5

CONTROL (PROTECTION) PART (Tch = 25°C, unless otherwise noted)

Symbol	Parameter	Condition		Limits			Unit
				Min.	Typ.	Max.	
I_D	Circuit current	Total of V_{P1}-V_{NC}, V_{N1}-V_{NC}	V_D=15V, V_{IN}=0V	-	-	2.80	mA
			V_D=15V, V_{IN}=5V	-	-	2.80	
I_{DB}		Each part of V_{UFB}-U, V_{VFB}-V, V_{WFB}-W	V_D=V_{DB}=15V, V_{IN}=0V	-	-	0.10	
			V_D=V_{DB}=15V, V_{IN}=5V	-	-	0.10	
$V_{SC(ref)}$	Short circuit trip level	V_D = 15V (Note 1)		0.43	0.48	0.53	V
UV_{DBt}	P-side Control supply under-voltage protection(UV)	Tch ≤125°C	Trip level	7.0	10.0	12.0	V
UV_{DBr}			Reset level	7.0	10.0	12.0	V
UV_{Dt}	N-side Control supply under-voltage protection(UV)		Trip level	10.3	-	12.5	V
UV_{Dr}			Reset level	10.8	-	13.0	V
OT_t	Overt temperature protection (Note2)	V_D = 15V	Trip level	100	120	140	°C
OT_{rh}		Detect LVIC temperature	Hysteresis of trip-reset	-	10	-	°C
V_{FOH}	Fault output voltage	V_{SC} = 0V, F_O terminal pulled up to 5V by 10kΩ		4.9	-	-	V
V_{FOL}		V_{SC} = 1V, I_{FO} = 1mA		-	-	0.95	V
t_{FO}	Fault output pulse width	(Note 3)		20	-	-	μs
I_{IN}	Input current	V_{IN} = 5V		0.70	1.00	1.50	mA
$V_{th(on)}$	ON threshold voltage	Applied between U_P, V_P, W_P, U_N, V_N, W_N-V_{NC}		-	2.10	2.60	V
$V_{th(off)}$	OFF threshold voltage			0.80	1.30	-	
$V_{th(hys)}$	ON/OFF threshold hysteresis voltage			0.35	0.65	-	
V_F	Bootstrap Di forward voltage	I_F=10mA including voltage drop by limiting resistor		1.1	1.7	2.3	V
R	Built-in limiting resistance	Included in bootstrap Di		80	100	120	Ω

Note 1 : SC protection works only for N-side MOSFET. Please select the external shunt resistance such that the SC trip-level is less than 1.7 times of the current rating.

2 : When the LVIC temperature exceeds OT trip temperature level(OT_t), OT protection works and Fo outputs. In that case if the heat sink dropped off or fixed loosely, don't reuse that DIPIPM. (There is a possibility that channel temperature of power chips exceeded maximum Tch(150°C).

3 : Fault signal Fo outputs when SC, UV or OT protection works. Fo pulse width is different for each protection modes. At SC failure, Fo pulse width is a fixed width (=minimum 20μs), but at UV or OT failure, Fo outputs continuously until recovering from UV or OT state. (But minimum Fo pulse width is 20μs.)

Recommended operating conditions of PSM05S93E5 are given in Table 2-1-5.

Although these conditions are the recommended but not the necessary ones, it is highly recommended to operate the modules within these conditions so as to ensure MOS DIPIPM safe operation.

Table 2-1-5 Recommended operating conditions of PSM05S93E5

RECOMMENDED OPERATION CONDITIONS

Symbol	Parameter	Condition		Limits			Unit
				Min.	Typ.	Max.	
V_{DD}	Supply voltage	Applied between P-NU, NV, NW		0	300	400	V
V_D	Control supply voltage	Applied between V_{P1}-V_{NC}, V_{N1}-V_{NC}		13.5	15.0	16.5	V
V_{DB}	Control supply voltage	Applied between V_{UFB}-U, V_{VFB}-V, V_{WFB}-W		13.0	15.0	18.5	V
ΔV_D, ΔV_{DB}	Control supply variation			-1	-	+1	V/μs
t_{dead}	Arm shoot-through blocking time	For each input signal		1.0	-	-	μs
f_{PWM}	PWM input frequency	T_C ≤ 100°C, Tch ≤ 125°C		-	-	20	kHz
I_O	Allowable r.m.s. current	V_{DD} = 300V, V_D = 15V, P.F = 0.8, Sinusoidal PWM T_C ≤ 100°C, Tch ≤ 125°C (Note1)	f_{PWM}= 5kHz	-	-	2.5	Arms
			f_{PWM}= 15kHz	-	-	2.0	
PWIN(on)	Minimum input pulse width	(Note 2)		0.7	-	-	μs
PWIN(off)				0.7	-	-	
V_{NC}	V_{NC} variation	Between V_{NC}-NU, NV, NW (including surge)		-5.0	-	+5.0	V
Tch	Channel temperature			-20	-	+125	°C

Note 1: Allowable r.m.s. current depends on the actual application conditions.

2: DIPIPM might not make response if the input signal pulse width is less than PWIN(on), PWIN(off).

About Control supply variation

If high frequency noise superimposed to the control supply line, IC malfunction might happen and cause DIPIPM erroneous operation. To avoid such problem, line ripple voltage should meet the following specifications:

dV/dt ≤ +/-1V/μs, Vripple≤2Vp-p

2.1.4 Mechanical Characteristics and Ratings

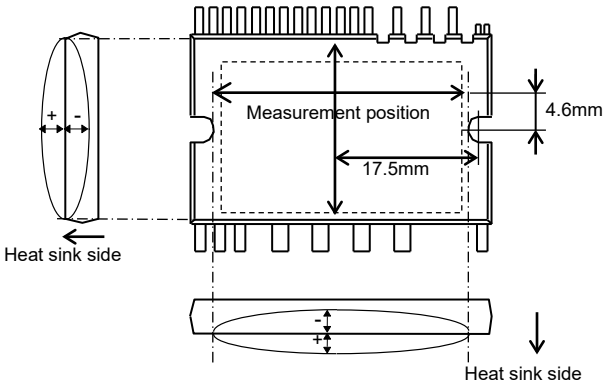
The mechanical characteristics and ratings are shown in Table 2-1-6.
Please refer to Section 2.4 for the detailed mounting instruction of MOS DIPIPM.

Table 2-1-6 Mechanical characteristics and ratings of PSM05S93E5

MECHANICAL CHARACTERISTICS AND RATINGS

Parameter	Condition		Limits			Unit
			Min.	Typ.	Max.	
Mounting torque	Mounting screw : M3 (Note 1)	Recommended 0.69N·m	0.59	-	0.78	N·m
Terminal pulling strength	Control terminal: Load 4.9N Power terminal: Load 9.8N	EIAJ-ED-4701	10	-	-	s
Terminal bending strength	Control terminal: Load 2.45N Power terminal: Load 4.9N 90deg. bend	EIAJ-ED-4701	2	-	-	times
Weight			-	8.5	-	g
Heat-sink flatness		(Note 2)	-50	-	100	μm

Note 1: Plain washers (ISO 7089~7094) are recommended.
Note 2: Measurement point of heat sink flatness



2.2 Protective Functions and Operating Sequence

MOS DIPIPM has Short circuit (SC), Under Voltage of control supply (UV) and Over Temperature (OT) for protection function. The operating principle and sequence are described below.

2.2.1 Short Circuit Protection

1. General

DIPIPM uses external shunt resistor for the current detection as shown in Fig.2-2-1. The internal protection circuit inside the IC captures the excessive large current by comparing the CIN voltage generated at the shunt resistor with the referenced SC trip voltage, and perform protection automatically. The threshold voltage trip level of the SC protection Vsc(ref) is typ. 0.48V.

In case of SC protection happens, all the gates of N-side three phase MOSFETs are interrupted together with fault signal output. To prevent DIPIPM erroneous protection due to normal switching noise and/or recovery current, it is necessary to set an RC filter (time constant: 1.5μ~2μs is recommended) to the CIN terminal input (Fig.2-2-1, 2-2-2). Also, please make the pattern wiring around the shunt resistor as short as possible.

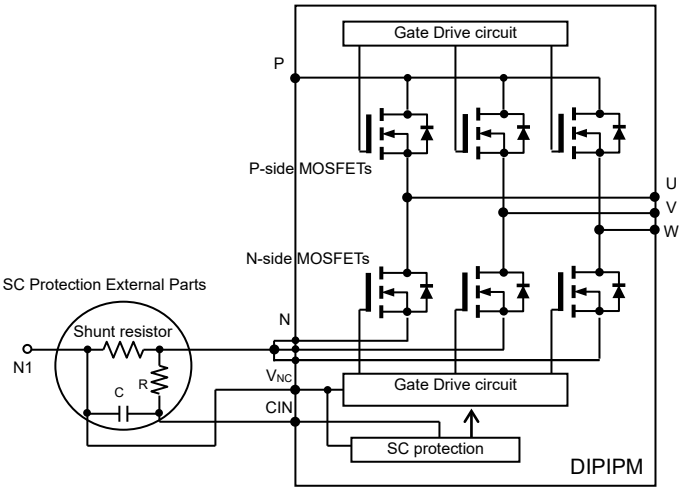


Fig.2-2-1 SC protecting circuit

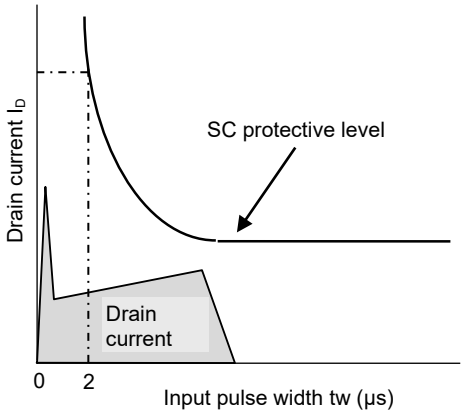


Fig.2-2-2 Filter time constant setting

2. SC protection Sequence

SC protection (N-side only with the external shunt resistor and RC filter)

a1. Normal operation: MOSFET ON and carrying current.

a2. Short circuit current detection (SC trigger).
(It is recommended to set RC time constant 1.5~2.0μs so that MOSFET shut down within 2.0μs when SC.)

a3. All N-side MOSFETs' gate are hard interrupted.

a4. All N-side MOSFETs turn OFF.

a5. Fo outputs for t_{Fo}=minimum 20μs.

a6. Input = "L". MOSFET OFF

a7. Fo finishes output, but MOSFETs don't turn on until inputting next ON signal (L→H).
(MOSFET of each phase can return to normal state by inputting ON signal to each phase.)

a8. Normal operation: MOSFET ON and outputs current.

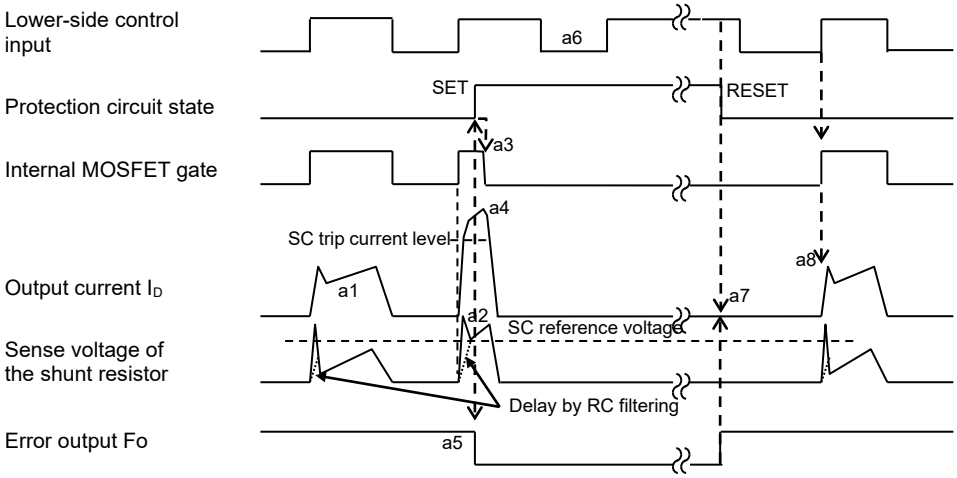


Fig.2-2-3 SC protection timing chart

3. Determination of Shunt Resistance

(1) Shunt resistance

The value of current sensing resistance is calculated by the following expression:

$$R_{Shunt} = V_{SC(ref)}/SC$$

where $V_{SC(ref)}$ is the referenced SC trip voltage.

The maximum SC trip level SC(max) should be set less than the MOSFET minimum saturation current which is 1.7 times as large as the rated current. For example, the SC(max) of PSM05S93E5 should be set to 5A x1.7=8.5A. The parameters ($V_{SC(ref)}$, R_{Shunt}) dispersion should be considered when designing the SC trip level.

For example of PSM05S93E5, there is +/-0.05V dispersion in the spec of $V_{SC(ref)}$ as shown in Table 2-2-1.

Table 2-2-1 Specification for $V_{SC(ref)}$ (unit: V)

Condition	Min	Typ	Max
at Tch=25°C, VD=15V	0.43	0.48	0.53

Then, the range of SC trip level can be calculated by the following expressions:

$R_{Shunt(min)}=V_{SC(ref)\ max}$ /SC(max)

$R_{Shunt(typ)}= R_{Shunt(min)}$ / 0.95* then SC(typ) = $V_{SC(ref)\ typ}$ / $R_{Shunt(typ)}$

$R_{Shunt(max)}= R_{Shunt(typ)}$ x 1.05* then SC(min)= $V_{SC(ref)\ min}$ / $R_{Shunt(max)}$

*)This is the case that shunt resistance dispersion is within +/-5%.

So the SC trip level range is described as Table 2-2-2.

Table 2-2-2 Operative SC Range (R_{Shunt}=62.4mΩ (min), 65.7mΩ (typ), 69.0mΩ(max)

Condition	min.	typ.	Max.
at Tch=25°C	6.2A	7.3A	8.5A

(e.g. 62.4mΩ ($R_{shunt(min)}$)= 0.53V (=$V_{SC(max)}$) / 8.5A(=SC(max))

There is the possibility that the actual SC protection level becomes less than the calculated value. This is considered due to the resonant signals caused mainly by parasitic inductance and parasitic capacity. It is recommended to make a confirmation of the resistance by prototype experiment.

(2) RC Filter Time Constant

It is necessary to set an RC filter in the SC sensing circuit in order to prevent malfunction of SC protection due to noise interference. The RC time constant is determined depending on the applying time of noise interference and the SCSOA of the DIPIPM.

When the voltage drop on the external shunt resistor exceeds the SC trip level, The time (t1) that the CIN terminal voltage rises to the referenced SC trip level can be calculated by the following expression:

$$V_{SC} = R_{shunt} \cdot I_c \cdot (1 - \varepsilon^{-\frac{t1}{\tau}})$$

$$t1 = -\tau \cdot \ln(1 - \frac{V_{SC}}{R_{shunt} \cdot I_c})$$

Vsc : the CIN terminal input voltage, Ic : the peak current, τ : the RC time constant

On the other hand, the typical time delay t2 (from Vsc voltage reaches Vsc(ref) to MOSFET gate shutdown) of IC is shown in Table 2-2-3.

Table 2-2-3 Internal time delay of IC

Item	min	typ	max	Unit
IC transfer delay time	-	-	0.5	μs

Therefore, the total delay time from an SC level current happened to the MOSFET gate shutdown becomes:

t_{TOTAL}=t1+t2

2.2.2 Control Supply UV Protection

The UV protection is designed to prevent unexpected operating behavior as described in Table 2-2-4.
Both P-side and N-side have UV protecting function. However, fault signal (Fo) output only corresponds to N-side UV protection. Fo output continuously during UV state.
In addition, there is a noise filter (typ. 10μs) integrated in the UV protection circuit to prevent instantaneous UV erroneous trip. Therefore, the control signals are still transferred in the initial 10μs after UV happened.

Table 2-2-4 DIPIPM operating behavior versus control supply voltage

Control supply voltage	Operating behavior
0-4.0V (P, N)	In this voltage range, built-in control IC may not work properly. Normal operating of each protection function (UV, Fo output etc.) is not also assured. Normally MOSFET does not work. But external noise may cause DIPIPM malfunction (turns ON), so DC-link voltage need to start up after control supply starts-up.
4.0-UV_{Dt} (N), UV_{DBt} (P)	UV function becomes active and output Fo (N-side only). Even if control signals are applied, MOSFET does not work
UV_{Dt} (N)-13.5V UV_{DBt} (P)-13.0V	MOSFET can work. However, conducting loss and switching loss will increase, and result extra temperature rise at this state,.
13.5-16.5V (N) 13.0-18.5V (P)	Recommended conditions.
16.5-20.0V (N) 18.5-20.0V (P)	MOSFET works. However, switching speed becomes fast and saturation current becomes large at this state, increasing SC broken risk.
20.0V- (P, N)	The control circuit will be destroyed.

Ripple Voltage Limitation of Control Supply

If high frequency noise superimposed to the control supply line, IC malfunction might happen and cause DIPIPM erroneous operation. To avoid such problem happens, line ripple voltage should meet the following specifications:

$$dV/dt \leq +/-1V/\mu s, \quad Vripple \leq 2Vp\text{-}p$$

[N-side UV Protection Sequence]

a1. Control supply voltage V_D exceeds under voltage reset level (UV_{Dr}), but MOSFET turns ON by next ON signal (L→H).(MOSFET of each phase can return to normal state by inputting ON signal to each phase.)
a2. Normal operation: MOSFET ON and carrying current.
a3. V_D level dips to under voltage trip level. (UV_{Dt}).
a4. All N-side MOSFETs turn OFF in spite of control input condition.
a5. Fo outputs for t_{Fo}=minimum 20μs, but output is extended during V_D keeps below UV_{Dr}.
a6. V_D level reaches UV_{Dr}.
a7. Normal operation: MOSFET ON and outputs current.

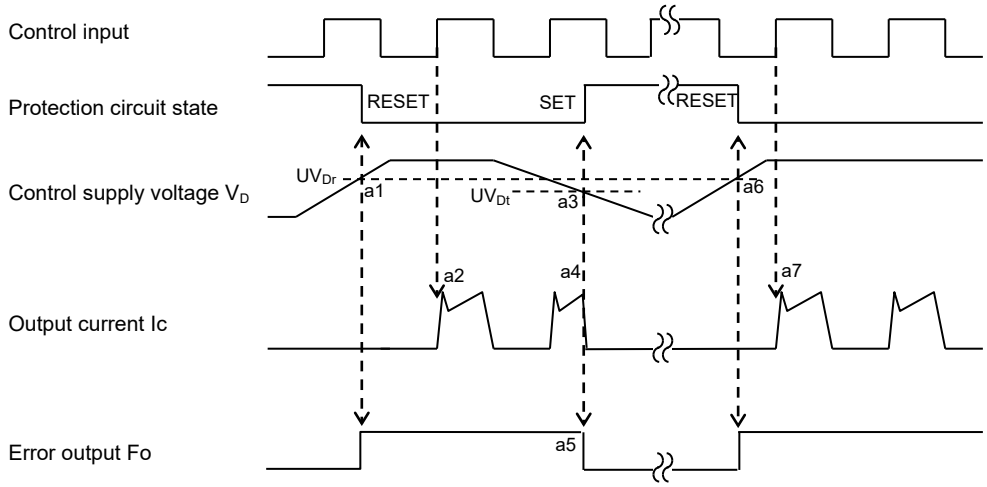


Fig.2-2-4 Timing chart of N-side UV protection

[P-side UV Protection Sequence]

a1. Control supply voltage V_{DB} rises. After the voltage reaches under voltage reset level UV_{DBr}, MOSFET turns on by next ON signal (L→H).
a2. Normal operation: MOSFET ON and outputs current.
a3. V_{DB} level dips to under voltage trip level (UV_{DBt}).
a4. MOSFET of the correspond phase only turns OFF in spite of control input signal level, but there is no F_O signal output.
a5. V_{DB} level reaches UV_{DBr}.
a6. Normal operation: MOSFET ON and outputs current.

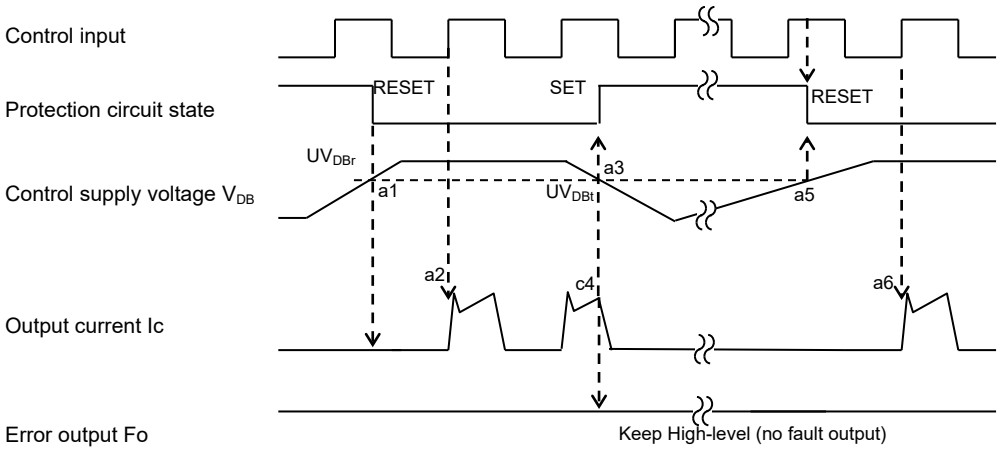


Fig.2-2-5 Timing Chart of P-side UV protection

2.2.3 OT Protection

DIPIPM series have OT (over temperature) protection function by monitoring LVIC temperature rise.
While LVIC temperature exceeds and keeps over OT trip temperature, error signal Fo outputs and all N-side MOSFETs are shut down without reference to input signal. (P-side MOSFETs are not shut down)
The specification of OT trip temperature and its sequence are described in Table 2-2-5 and Fig.2-2-6.

Table 2-2-5 OT trip temperature specification

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Over temperature protection	OT_t	V_D=15V, At temperature of LVIC	Trip level	100	120	140	°C
	OT_{rh}		Trip/reset hysteresis	-	10	-	

[OT Protection Sequence]
a1. Normal operation: MOSFET ON and outputs current.
a2. LVIC temperature exceeds over temperature trip level(OT_t).
a3. All N-side MOSFETs turn OFF in spite of control input condition.
a4. Fo outputs for t_{Fo}=minimum 20μs, but output is extended during LVIC temperature keeps over OT_t.
a5. LVIC temperature drops to over temperature reset level.
a6. Normal operation: MOSFET turns on by next ON signal (L→H).
(MOSFET of each phase can return to normal state by inputting ON signal to each phase.)

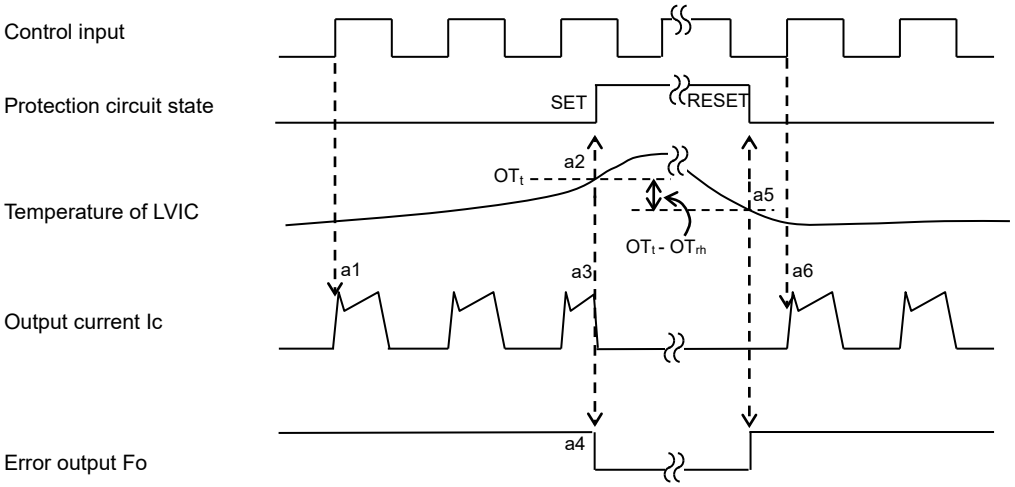


Fig.2-2-6 Timing Chart of OT protection

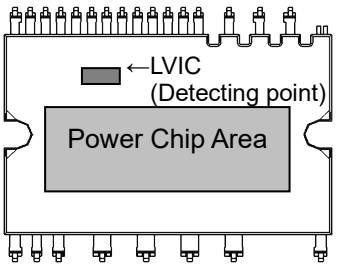


Fig.2-2-7 Temperature detecting point

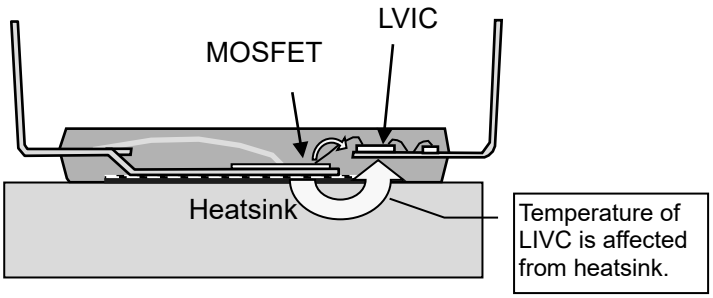


Fig.2-2-8 Thermal conducting from power chips

Precaution about this OT protection function

(1)This OT protection will not work effectively in the case of rapid temperature rise like motor lock or over current. (This protection monitors LVIC temperature, so it cannot respond to rapid temperature rise of power chips.)

(2)If the cooling system is abnormal state (e.g. heat sink comes off, fixed loosely, or cooling fun stops) when OT protection works, can't reuse the DIPIPM. (Because the channel temperature of power chips will exceeded the maximum rating of Tch(150°C).)

2.3 Package Outlines

2.3.1 Package outlines

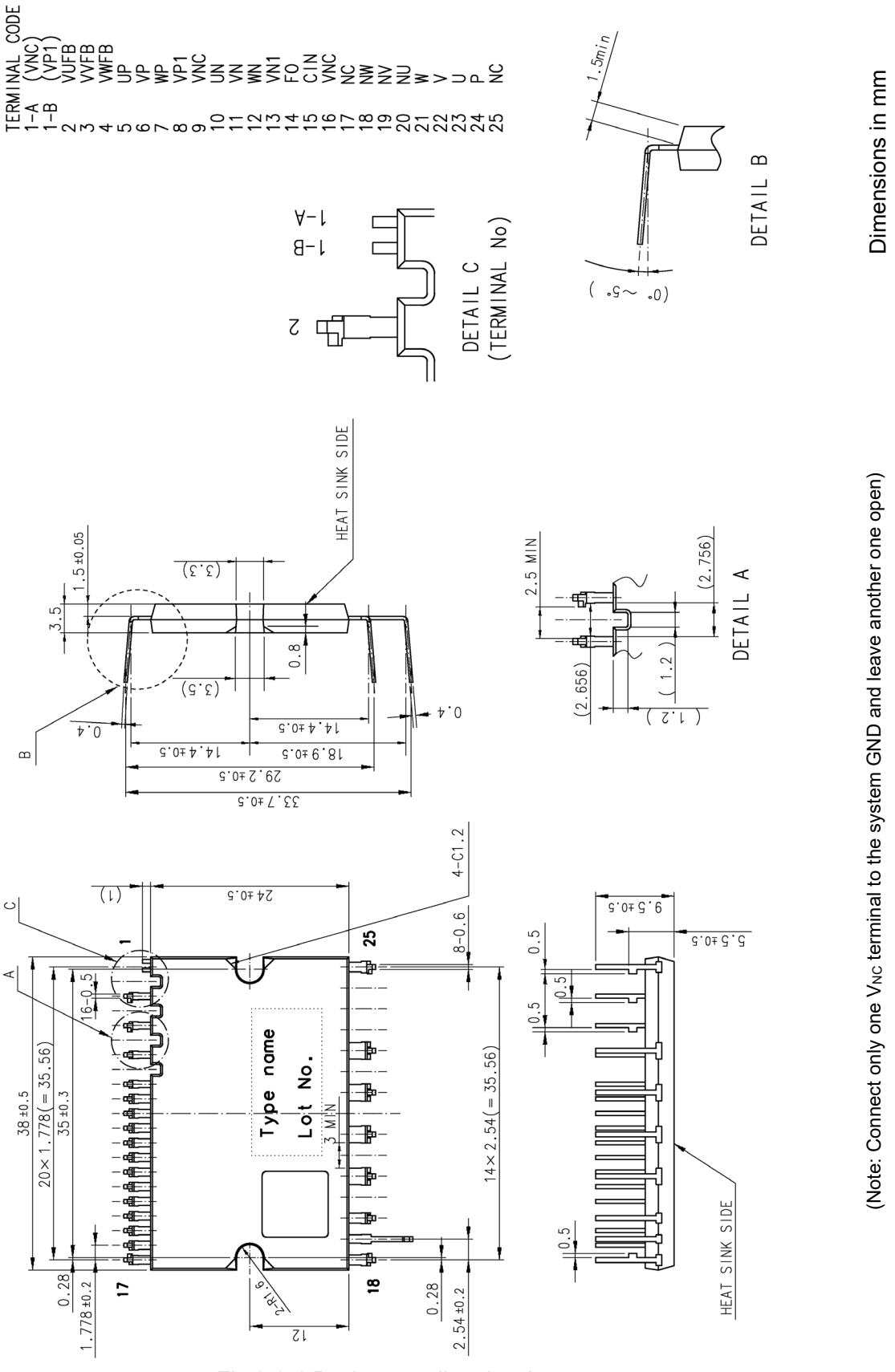


Fig.2-3-1 Package outline drawing

2.3.2 Marking

The laser marking specification of DIP Ver.6 is described in Fig.2-3-2. Company name, Type name, Lot number, Made of origin, and 2D code mark are marked in the upper side of module.

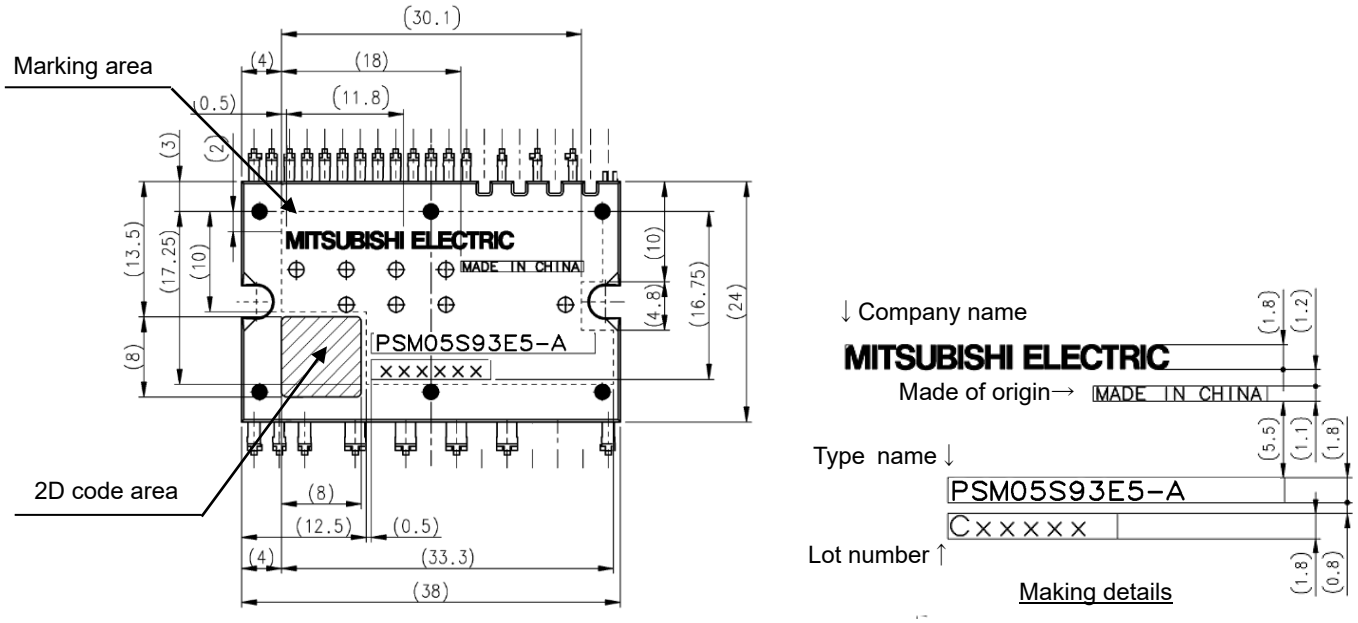


Fig.2-3-2 Laser marking view

The Lot number indicates production year, month, running number and country of origin.
The detailed is described as below.

(Example) H 3 9 AA1

- AA1 → Running number
- 9 → Product month (however O: October, N: November, D: December)
- 3 → Last figure of Product year (e.g. 2013)
- H → Factory identification
  - No mark : Manufactured at the factory in Japan
  - C : Manufactured at the factory A in China
  - H : Manufactured at the factory B in China

2.3.3 Terminal Description

Table 2-3-1 Terminal description

Pin	Name	Description
1-A	(V_{NC})*2	Inner used terminal It has control GND potential, so it should be left no connection.
1-B	(V_{P1})*2	Inner used terminal It has control supply potential, so it should be left no connection.
2	V_{UFB}	U-phase P-side drive supply positive terminal
3	V_{VFB}	V-phase P-side drive supply positive terminal
4	V_{WFB}	W-phase P-side drive supply positive terminal
5	U_P	U-phase P-side control input terminal
6	V_P	V-phase P-side control input terminal
7	W_P	W-phase P-side control input terminal
8	V_{P1}	P-side control supply positive terminal
9	V_{NC}*1	P-side control supply GND terminal
10	U_N	U-phase N-side control input terminal
11	V_N	V-phase N-side control input terminal
12	W_N	W-phase N-side control input terminal
13	V_{N1}	N-side control supply positive terminal
14	F_O	Fault signal output terminal
15	CIN	SC trip voltage detecting terminal
16	V_{NC}*1	N-side control supply GND terminal
17	NC	No connection (There isn't any connection inside DIPIPM.)
18	NW	WN-phase MOSFET emitter
19	NV	VN-phase MOSFET emitter
20	NU	UN-phase MOSFET emitter
21	W	W-phase output terminal(W-phase drive supply GND)
22	V	V-phase output terminal (V-phase drive supply GND)
23	U	U-phase output terminal (U-phase drive supply GND)
24	P	Inverter DC-link positive terminal
25	NC	No connection (There isn't any connection inside DIPIPM.)

*1) Connect only one V_{NC} terminal to the system GND and leave another one open.
*2) No.1-A,1-B are inner used terminals, so it is necessary to leave no connection.

Table 2-3-2 Detailed description of input and output terminals

Item	Symbol	Description
P-side drive supply positive terminal P-side drive supply GND terminal	V_{UFB}-U V_{VFB}-V V_{WFB}-W	• Drive supply terminals for P-side MOSFETs. • By mounting bootstrap capacitor, individual isolated power supplies are not needed for the P-side MOSFET drive. Each bootstrap capacitor is charged by the N-side V_D supply when potential of outpurt terminal is almost GND level. • Abnormal operation might happen if the V_D supply is not aptly stabilized or has insufficient current capability due to ripple or surge. In order to prevent malfunction, a bypass capacitor with favorable frequency and temperature characteristics should be mounted very closely to each pair of these terminals. • Inserting a Zener diode (24V/1W) between each pair of control supply terminals is helpful to prevent control IC from surge destruction.
P-side control supply terminal N-side control supply terminal	V_{P1} V_{N1}	• Control supply terminals for the built-in HVIC and LVIC. • In order to prevent malfunction caused by noise and ripple in the supply voltage, a bypass capacitor with favorable frequency characteristics should be mounted very closely to these terminals. • Carefully design the supply so that the voltage ripple caused by noise or by system operation is within the specified minimum limitation. • It is recommended to insert a Zener diode (24V/1W) between each pair of control supply terminals to prevent surge destruction.
N-side control GND terminal	V_{NC}	• Control ground terminal for the built-in HVIC and LVIC. • Ensure that line current of the power circuit does not flow through this terminal in order to avoid noise influences. • Connect only one V_{NC} terminal (9 or 16pin) to the GND, and leave another one open.
Control input terminal	U_P,V_P,W_P U_N,V_N,W_N	• Control signal input terminals.Voltage input type. • These terminals are internally connected to Schmitt trigger circuit. • The wiring of each input should be as short as possible to protect the DIPIPM from noise interference. • Use RC filter in case of signal oscillation. (Pay attention to threshold voltage of input terminal, because input circuit has pull down resistor (min 3.3kΩ))
Short-circuit trip voltage detecting terminal	CIN	• For inverter part SC protection, input the potential of shuint resistor to CIN terminal through RC filter (for the noise immunity). • The time constant of RC filter is recommended to be up to 2μs.
Fault signal output terminal	F_O	• Fault signal output terminal. • Fo signal line should be pulled up to a 5V logic supply with over 5kΩ resistor (for limitting the Fo sink current I_{Fo} up to 1mA.) Normally 10kΩ is recommended.
Inverter DC-link positive terminal	P	• DC-link positive power supply terminal. • Internally connected to the collectors of all P-side MOSFETs. • To suppress surge voltage caused by DC-link wiring or PCB pattern inductance, smoothing capacitor should be located very closely to the P and N terminal of DIPIPM. It is also effective to add small film capacitor with good frequency characteristics.
Inverter DC-link negative terminal	NU,NV,NW	• Open emitter terminal of each N-side MOSFET • Usually, these terminals are connected to the power GND through individual shunt resistor.
Inverter power output terminal	U, V, W	• Inverter output terminals for connection to inverter load (e.g. motor). • Each terminal is internally connected to the intermidiate point of the corresponding MOSFET half bridge arm.

Note: Use oscilloscope to check voltage waveform of each power supply terminals and P&N terminals, the time division of OSC should be set to about 1μs/div. Please ensure the voltage (including surge) not exceed the specified limitation.

2.4 Mounting Method

This section shows the electric spacing and mounting precautions of MOS DIPIPM.

2.4.1 Electric Spacing

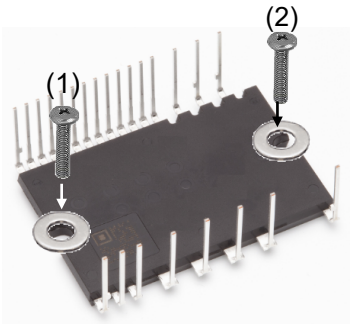
The electric spacing specification of DIPIPM is shown in Table 2-4-1

Table 2-4-1 Minimum insulation distance of DIPIPM

	Clearance (mm)	Creepage (mm)
Between live terminals with high potential	2.50	3.00
Between terminals and heat sink	1.45	1.50

2.4.2 Mounting Method and Precautions

When installing the module to the heat sink, excessive or uneven fastening force might apply stress to inside chips. Then it will lead to a broken or degradation of the chips or insulation structure. The recommended fastening procedure is shown in Fig.2-4-1. When fastening, it is necessary to use the torque wrench and fasten up to the specified torque. And pay attention to the foreign particle on the contact surface between the module and the heat sink. Even if the fixing of heatsink was done by proper procedure and condition, there is a possibility of damaging the package because of tightening by unexpected excessive toruque or tucking particle. For ensuring safety it is recommended to conduct the confirmation test(e.g. insulation inspection) on the final product after fixing the DIPIPM with the heatsink.



Temporary fastening
(1)→(2)

Permanent fastening
(1)→(2)

Note: Generally, the temporary fastening torque is set to 20-30% of the maximum torque rating.
Not care the order of fastening (1) or (2), but need to fasten alternately.

Fig.2-4-1 Recommended screw fastening order

Table 2-4-2 Mounting torque and heat sink flatness specifications

Item	Condition	Min.	Typ.	Max.	Unit
Mounting torque	Recommended 0.69N·m, Screw : M3	0.59	-	0.78	N·m
Flatness of outer heat sink	Refer Fig.2-4-2	-50	-	+100	μm

Note : Recommend to use plain washer (ISO7089-7094) in fastening the screws.

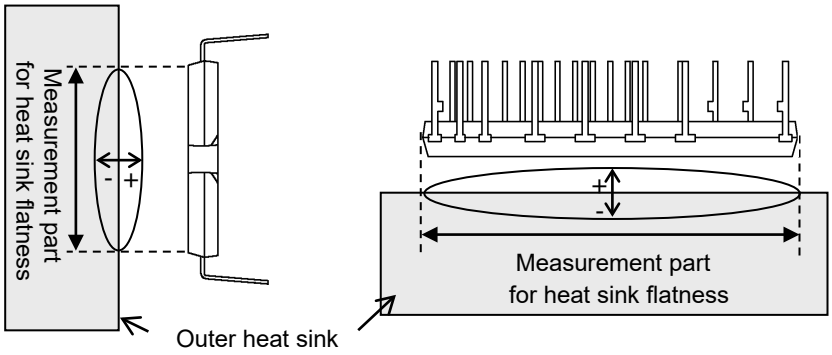


Fig.2-4-2 Measurement point of heat sink flatness

In order to get effective heat dissipation, it is necessary to enlarge the contact area as much as possible to minimize the contact thermal resistance. Regarding the heat sink flatness (warp/concavity and convexity) on the module installation surface, the surface finishing-treatment should be within Rz12.

Evenly apply thermally-conductive grease with 100μ-200μm thickness over the contact surface between a module and a heat sink, which is also useful for preventing corrosion. Furthermore, the grease should be with stable quality and long-term endurance within wide operating temperature range. The contacting thermal resistance between DIPIPM case and heat sink Rth(c-f) is determined by the thickness and the thermal conductivity of the applied grease. For reference, Rth(c-f) is about 0.3K/W (per 1/6 module, grease thickness: 20μm, thermal conductivity: 1.0W/m·k). When applying grease and fixing heat sink, pay attention not to take air into grease. It might lead to make contact thermal resistance worse or loosen fixing in operation.

2.4.3 Soldering Conditions

The recommended soldering condition is mentioned as below.
(Note: The reflow soldering cannot be recommended for DIPIPM.)

(1) Flow (wave) Soldering

MOS DIPIPM is tested on the condition described in Table 2-4-3 about the soldering thermostability, so the recommended conditions for flow (wave) soldering are soldering temperature is up to 265°C and the immersion time is within 11s.

However, the condition might need some adjustment based on flow condition of solder, the speed of the conveyer, the land pattern and the through hole shape on the PCB, etc.

It is necessary to confirm whether it is appropriate or not for your real PCB finally.

Table 2-4-3 Reliability test specification

Item	Condition
Soldering thermostability	260±5°C, 10±1s

(2) Hand soldering

Since the temperature impressed upon the DIPIPM may changes based on the soldering iron types (wattages, shape of soldering tip, etc.) and the land pattern on PCB, the unambiguous hand soldering condition cannot be decided.

As a general requirement of the temperature profile for hand soldering, the temperature of the root of the DIPIPM terminal should be kept under 150°C for considering glass transition temperature (Tg) of the package molding resin and the thermal withstand capability of internal chips. Therefore, it is necessary to check the DIPIPM terminal root temperature, solderability and so on in your real PCB, when configure the soldering temperature profile. (It is recommended to set the soldering time as short as possible.)

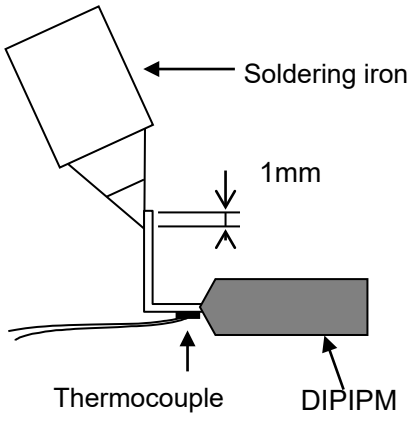
For reference, the evaluation example of hand soldering with 50W soldering iron is described as below.

[Evaluation method]

a. Sample: Super mini DIPIPM (Short lead type)

b. Evaluation procedure

- Put the soldering tip of 50W iron (temperature set to 350/400°C) on the terminal within 1mm from the toe. (The lowest heat capacity terminal (=control terminal) is selected.)
- Measure the temperature rise of the terminal root part by the thermocouple installed on the terminal root.



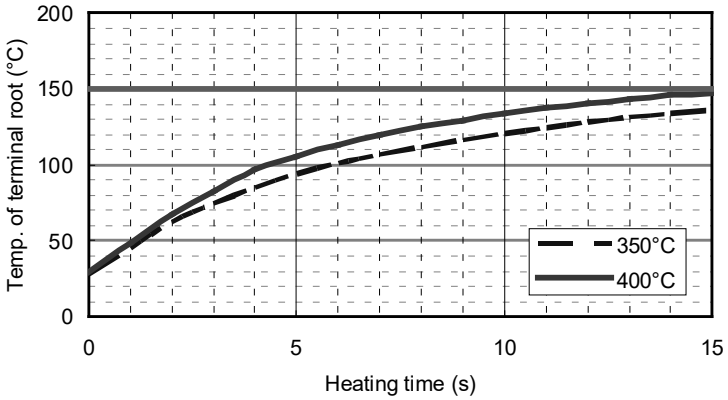


Fig.2-4-3 Heating and measuring point Fig.2-4-4 Temperature alteration of the terminal root (Example)

[Note]

For soldering iron, it is recommended to select one for semiconductor soldering (12~24V low voltage type, and the earthed iron tip) and with temperature adjustment function.

CHAPTER 3 SYSTEM APPLICATION GUIDANCE

3.1 Application Guidance

This chapter states the MOS DIPIPM application method and interface circuit design hints.

3.1.1 System connection

C1: Electrolytic type with good temperature and frequency characteristics.
Note: the capacitance also depends on the PWM control strategy of the application system
C2:0.22μ-2μF ceramic capacitor with good temperature, frequency and DC bias characteristics
C3: For snubber, 0.1μ-0.22μF capacitor (e.g. film capacitor)
D1:Zener diode 24V/1W for surge absorber

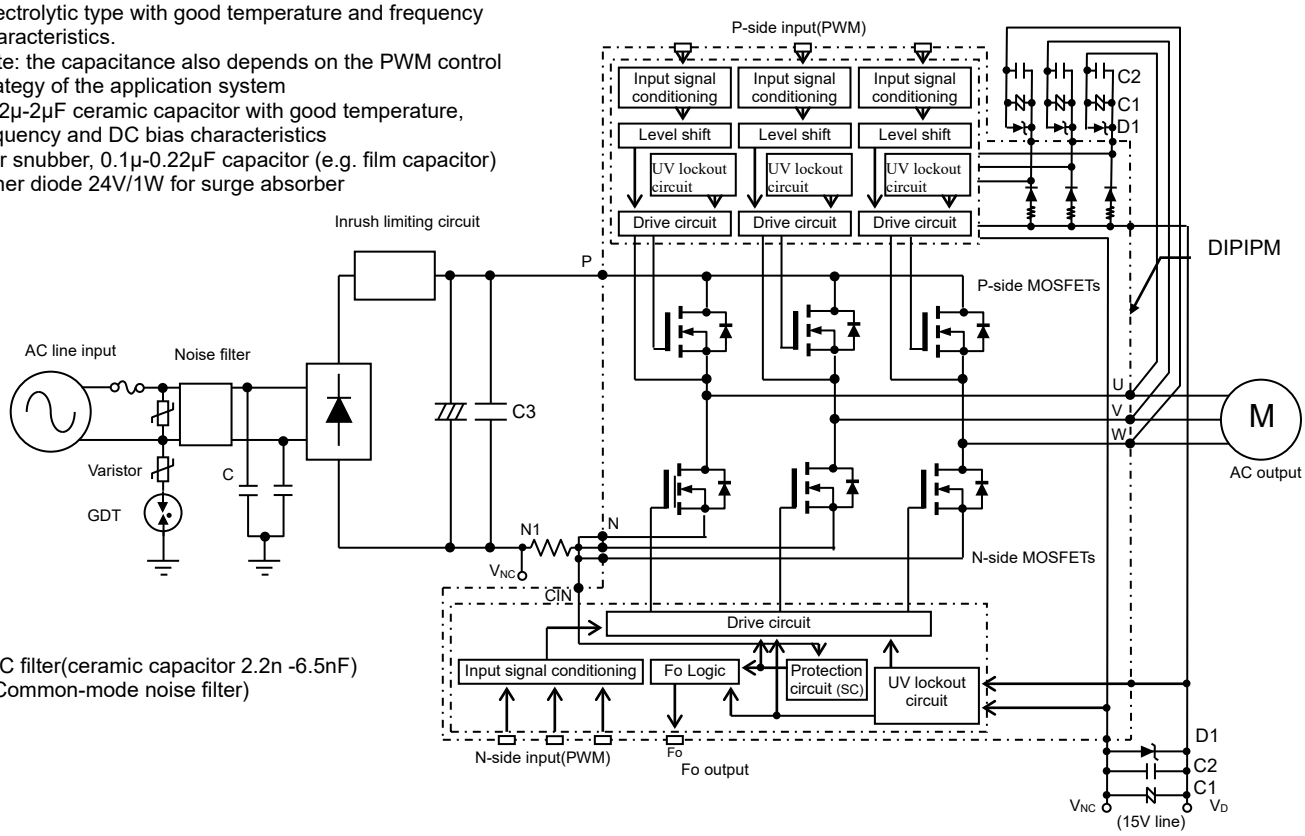


Fig.3-1-1 Application System block diagram

3.1.2 Interface Circuit (Direct Coupling Interface example for using one shunt resistor)

Fig.3-1-2 shows a typical application circuit of interface schematic, in which control signals are transferred directly input from a controller (e.g. MCU, DSP).

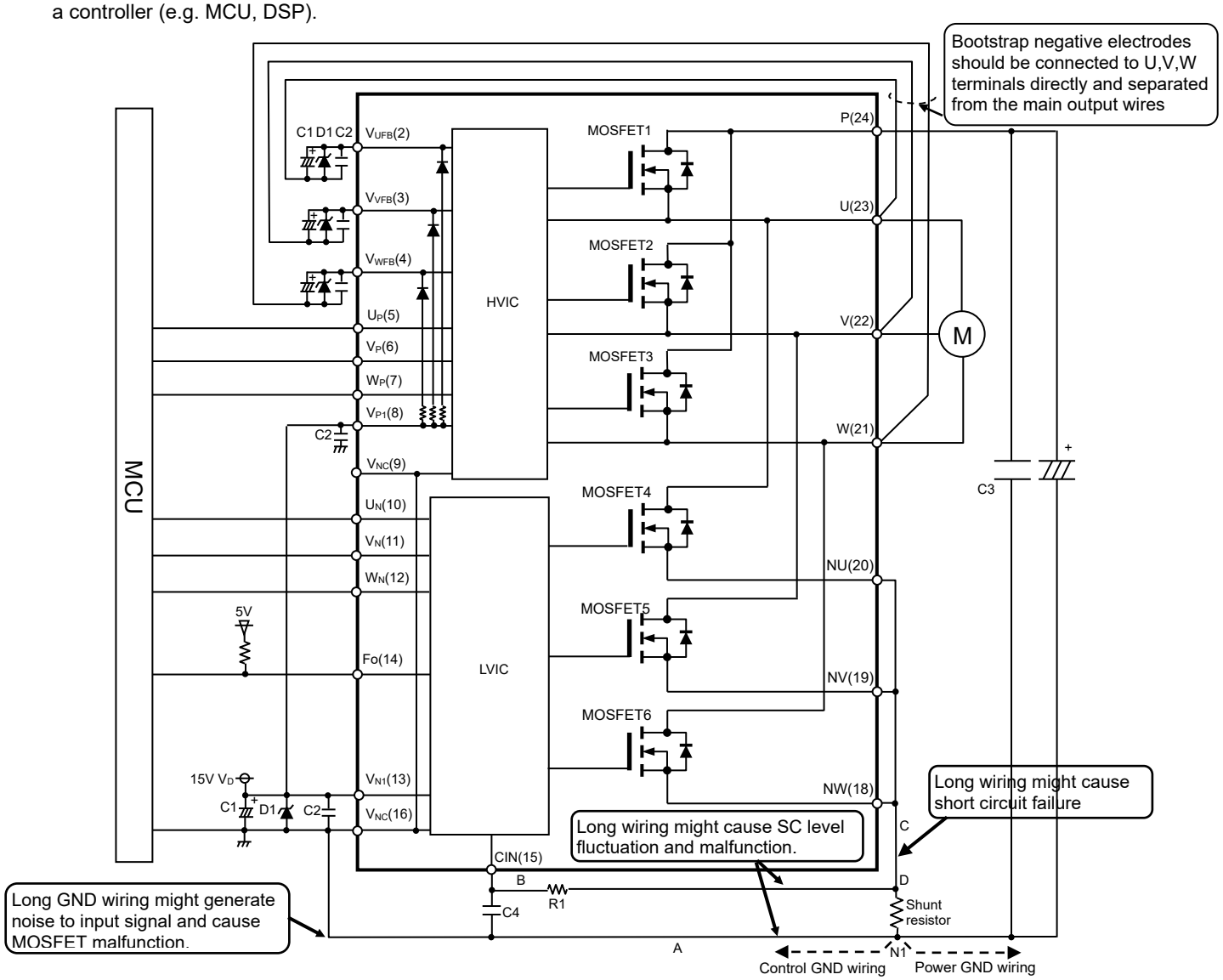


Fig.3-1-2 Interface circuit example in the case of using with one shunt resistor

(1) If control GND is connected with power GND by common broad pattern, it may cause malfunction by power GND fluctuation. It is recommended to connect control GND and power GND at only a point N1 (near the terminal of shunt resistor).

(2) It is recommended to insert a Zener diode D1(24V/1W) between each pair of control supply terminals to prevent surge destruction.

(3) To prevent surge destruction, the wiring between the smoothing capacitor and the P, N1 terminals should be as short as possible. Generally a 0.1-0.22μF snubber capacitor C3 between the P-N1 terminals is recommended.

(4) R1, C4 of RC filter for preventing protection circuit malfunction is recommended to select tight tolerance, temp-compensated type. The time constant R1C4 should be set so that SC current is shut down within 2μs. (1.5μs~2μs is general value.) SC interrupting time might vary with the wiring pattern, so the enough evaluation on the real system is necessary.

(5) To prevent malfunction, the wiring of A, B, C should be as short as possible.

(6) The point D at which the wiring to CIN filter is divided should be near the terminal of shunt resistor. NU, NV, NW terminals should be connected at near NU, NV, NW terminals.

(7) All capacitors should be mounted as close to the terminals as possible. (C1: good temperature, frequency characteristic electrolytic type and C2:0.22μ-2μF, good temperature, frequency and DC bias characteristic ceramic type are recommended.)

(8) Input drive is High-active type. There is a minimum 3.3kΩ pull-down resistor in the input circuit of IC. To prevent malfunction, the wiring of each input should be as short as possible. When using RC coupling circuit, make sure the input signal level meet the turn-on and turn-off threshold voltage.

(9) Fo output is open drain type. It should be pulled up to MCU or control power supply (e.g. 5V,15V) by a resistor that makes I_{Fo} up to 1mA. (I_{FO} is estimated roughly by the formula of control power supply voltage divided by pull-up resistance. In the case of pulled up to 5V, 10kΩ (5kΩ or more) is recommended.)

(10) Thanks to built-in HVIC, direct coupling to MCU without any opto-coupler or transformer isolation is possible.

(11) Two V_{NC} terminals (9 & 16 pin) are connected inside DIPIPM, please connect either one to the 15V power supply GND outside and leave another one open.

(12) If high frequency noise superimposed to the control supply line, IC malfunction might happen and cause DIPIPM erroneous operation. To avoid such problem, line ripple voltage should meet dV/dt ≤+/-1V/μs, Vripple≤2Vp-p.

3.1.3 Interface Circuit (Example of Opto-coupler Isolated Interface)

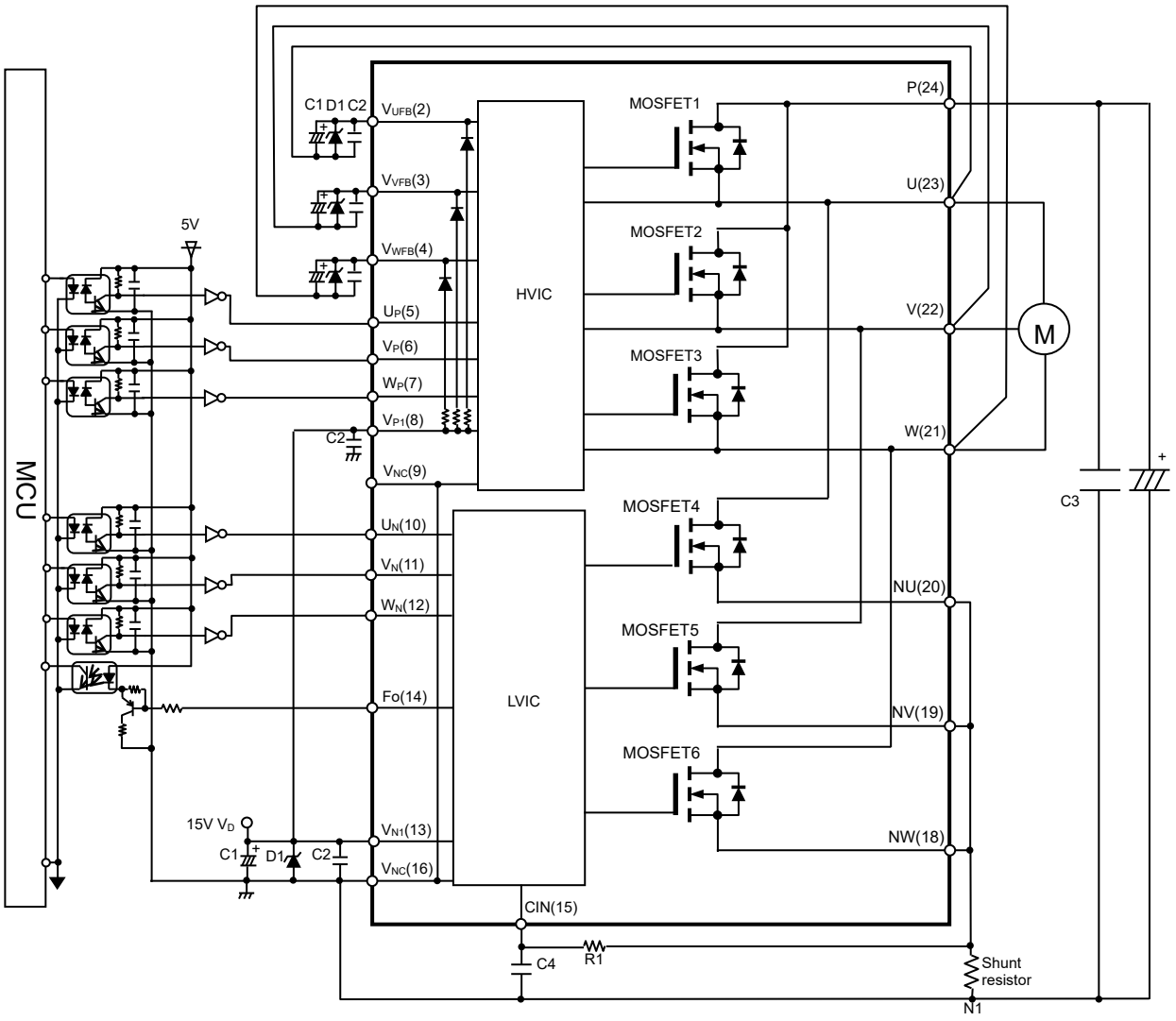


Fig.3-1-3 Interface circuit example with opto-coupler

Note:
(1) High speed (high CMR) opto-coupler is recommended.
(2) Fo terminal sink current for inverter part is max.1mA.

3.1.4 External SC Protection Circuit with Using Three Shunt Resistors

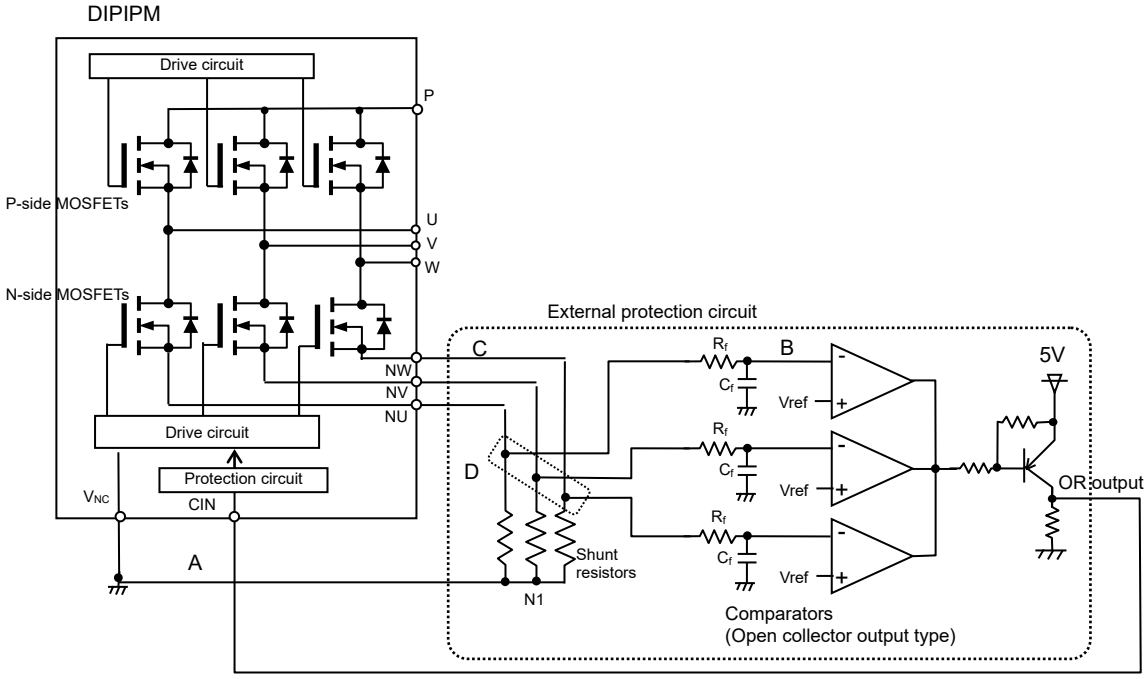


Fig.3-1-4 Interface circuit example

Note:
(1) It is necessary to set the time constant R_fC_f of external comparator input so that MOSFET stop within 2μs when short circuit occurs. SC interrupting time might vary with the wiring pattern, comparator speed and so on.
(2) The threshold voltage Vref should be set up the same rating of short circuit trip level (Vsc(ref) typ. 0.48V).
(3) Select the external shunt resistance so that SC trip-level is less than specified value.
(4) To avoid malfunction, the wiring A, B, C should be as short as possible.
(5) The point D at which the wiring to comparator is divided should be near the terminal of shunt resistor.
(6) OR output high level should be over 0.53V (=maximum Vsc(ref)).
(7) GND of Comparator, Vref circuit and Cf should be not connected to noisy power GND but to control GND wiring.

3.1.5 Circuits of Signal Input Terminals and Fo Terminal

(1) Internal Circuit of Control Input Terminals

MOS DIPIPM is high-active input logic. A 3.3kΩ(min) pull-down resistor is built-in each input circuits of the DIPIPM as shown in Fig.3-1-5 , so external pull-down resistor is not needed.

Furthermore, by lowering the turn on and turn off threshold value of input signal as shown in Table 3-1-1, a direct coupling to 3V class microcomputer or DSP becomes possible.

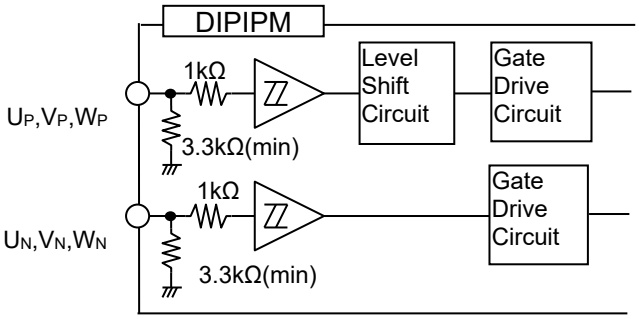


Fig.3-1-5 Internal structure of control input terminals

Table 3-1-1 Input threshold voltage ratings(Tch=25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Turn-on threshold voltage	Vth(on)	U_P,V_P,W_P-V_{NC} terminals U_N,V_N,W_N-V_{NC} terminals	-	2.1	2.6	V
Turn-off threshold voltage	Vth(off)		0.8	1.3	-	
Threshold voltage hysterisis	Vth(hys)		0.35	0.65	-	

Note: There are specifications for the minimum input pulse width in MOS DIPIPM. DIPIPM might make no response if the input signal pulse width (both on and off) is less than the specified value. Please refer to the datasheet for the specification.

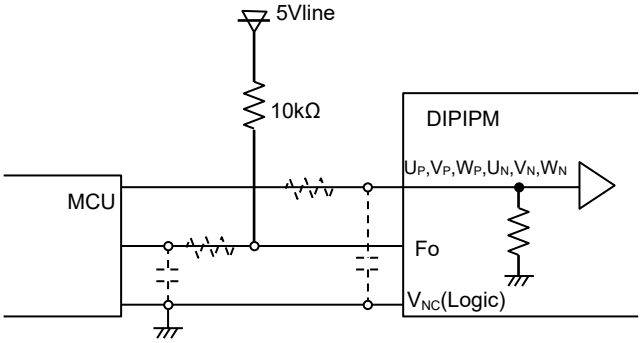


Fig.3-1-6 Control input connection

Note: The RC coupling (parts shown in the dotted line) at each input depends on user's PWM control strategy and the wiring impedance of the printed circuit board.
The DIPIPM signal input section integrates a 3.3kΩ(min) pull-down resistor. Therefore, when using an external filtering resistor, please pay attention to the signal voltage drop at input terminal.

(2) Internal Circuit of Fo Terminal

F_O terminal is an open drain type, it should be pulled up to a 5V supply as shown in Fig.3-1-6. Fig.3-1-7 shows the typical V-I characteristics of Fo terminal. The maximum sink current of Fo terminal is 1mA.
If the opto-coupler is applied to this output, please pay attention to the opto-coupler drive ability.

Table 3-1-2 Electric characteristics of Fo terminal

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Fault output voltage	V_{FOH}	V_{SC}=0V,Fo=10kΩ,5V pulled-up	4.9	-	-	V
	V_{FOL}	V_{SC}=1V,Fo=1mA	-	-	0.95	V

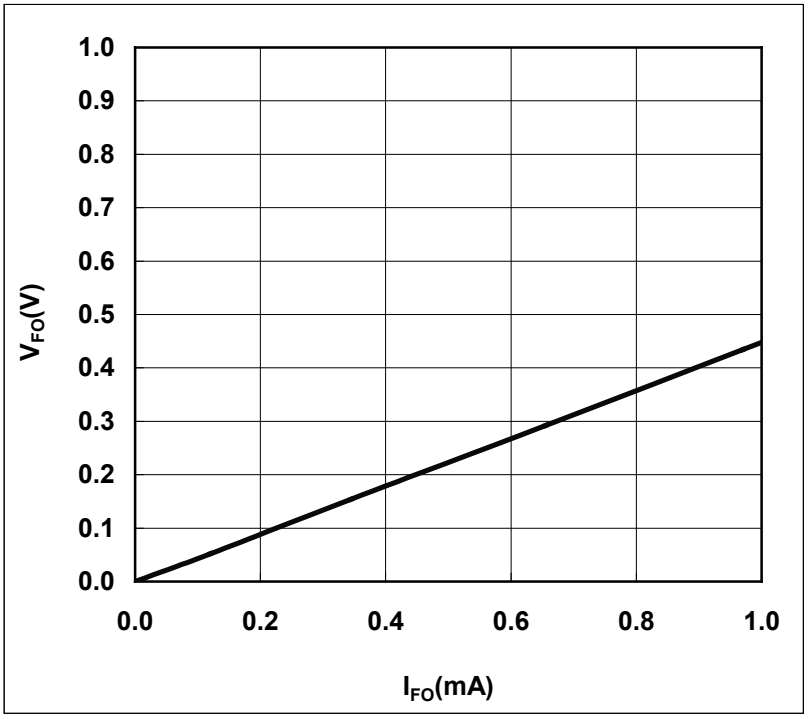


Fig.3-1-7 Fo terminal typical V-I characteristics (V_D=15V, Tch=25°C)

3.1.6 Snubber Circuit

In order to prevent MOS DIPIPM from destruction by extra surge, the wiring length between the smoothing capacitor and DIPIPM P terminal – N1 points (shunt resistor terminal) should be as short as possible. Also, a 0.1μ~0.22μF/630V snubber capacitor should be mounted in the DC-link and near to P, N1.

There are two positions ((1)or(2)) to mount a snubber capacitor as shown in Fig.3-1-8. Snubber capacitor should be installed in the position (2) so as to suppress surge voltage effectively. However, the charging and discharging currents generated by the wiring inductance and the snubber capacitor will flow through the shunt resistor, which might cause erroneous protection if this current is large enough.

In order to suppress the surge voltage maximally, the wiring at part-A (including shunt resistor parasitic inductance) and part-B should be as small as possible. A better wiring example is shown in location (3).

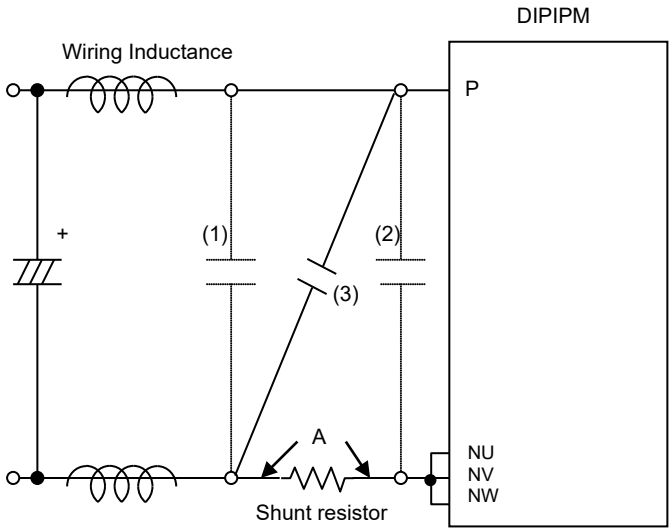


Fig.3-1-8 Recommended snubber circuit location

3.1.7 Recommended Wiring Method around Shunt Resistor

External shunt resistor is applied to detect short-circuit accident. The long wiring between NU, NV, NW terminal and N1 point causes so much large surge that might damage built-in IC. (MOSFET has faster turn off speed, so it tends to generate larger surge.) The wiring between NU,NV,NW terminal and N1 point should be as short as possible and low inductance type resistor such as leadless SMD resistor is strongly recommended, so that total parasitic inductance including inductance of shunt resistor becomes 10nH or less.

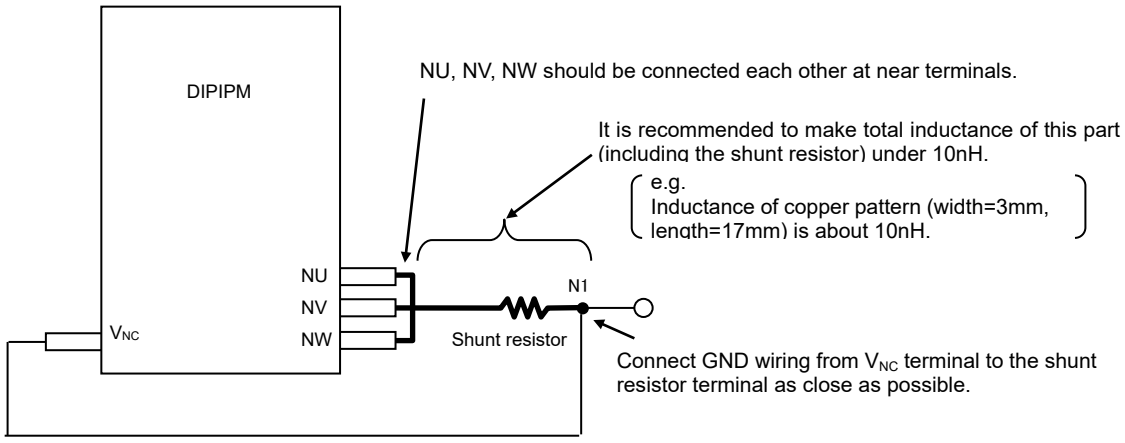


Fig.3-1-9 Wiring instruction (In the case of using with one shunt resistor)

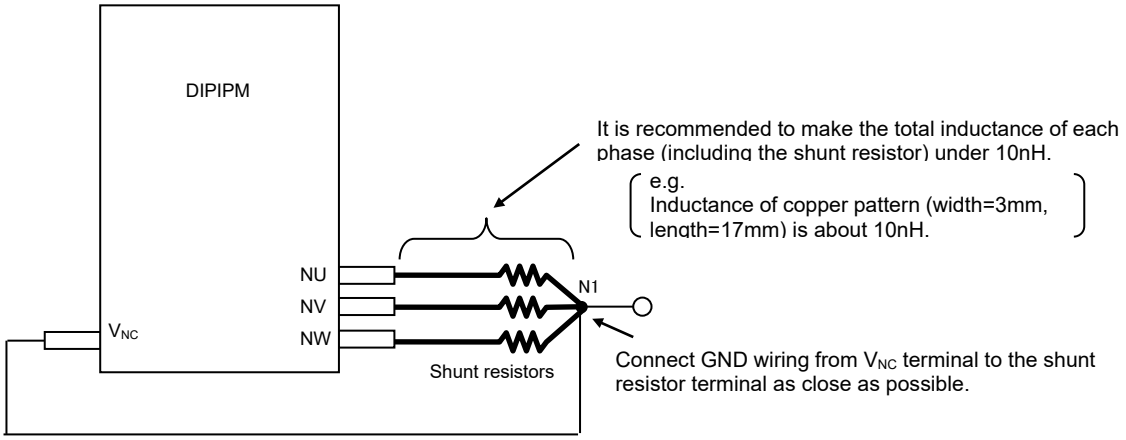


Fig.3-1-10 Wiring instruction (In the case of using with three shunt resistors)

Influence of pattern wiring around the shunt resistor is shown below.

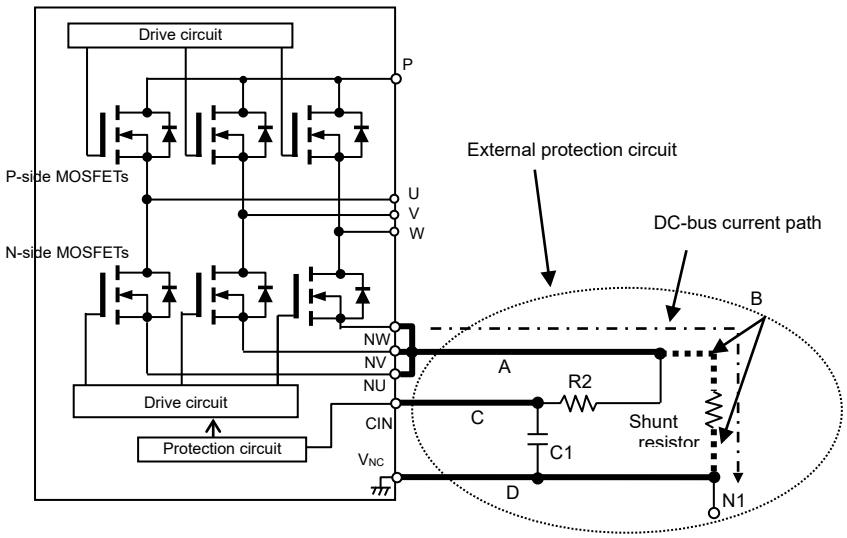


Fig.3-1-11 External protection circuit

(1) Influence of the part-A wiring

The ground of N-side MOSFET gate is V_{NC}. If part-A wiring pattern in Fig.3-1-11 is too long, extra voltage generated by the wiring parasitic inductance will result the potential of MOSFET source variation during switching operation. Please install shunt resistor as close to the N terminal as possible.

(2) Influence of the part-B wiring

The part-B wiring affects SC protection level. SC protection works by detecting the voltage of the CIN terminals. If part-B wiring is too long, extra surge voltage generated by the wiring inductance will lead to deterioration of SC protection level. It is necessary to connect CIN and V_{NC} terminals directly to the two ends of shunt resistor and avoid long wiring.

(3) Influence of the part-C wiring pattern

R2C1 filter is added to remove noise influence occurring on shunt resistor. Filter effect will dropdown and noise will easily superimpose on the wiring if part-C wiring is too long. It is necessary to install the R2C1 filter near CIN, V_{NC} terminals as close as possible.

(4) Influence of the part-D wiring pattern

Part-D wiring pattern gives influence to all the items described above, maximally shorten the GND wiring is expected.

3.1.8 Precaution for Wiring on PCB

This section shows main points to notice about PCB patterning.

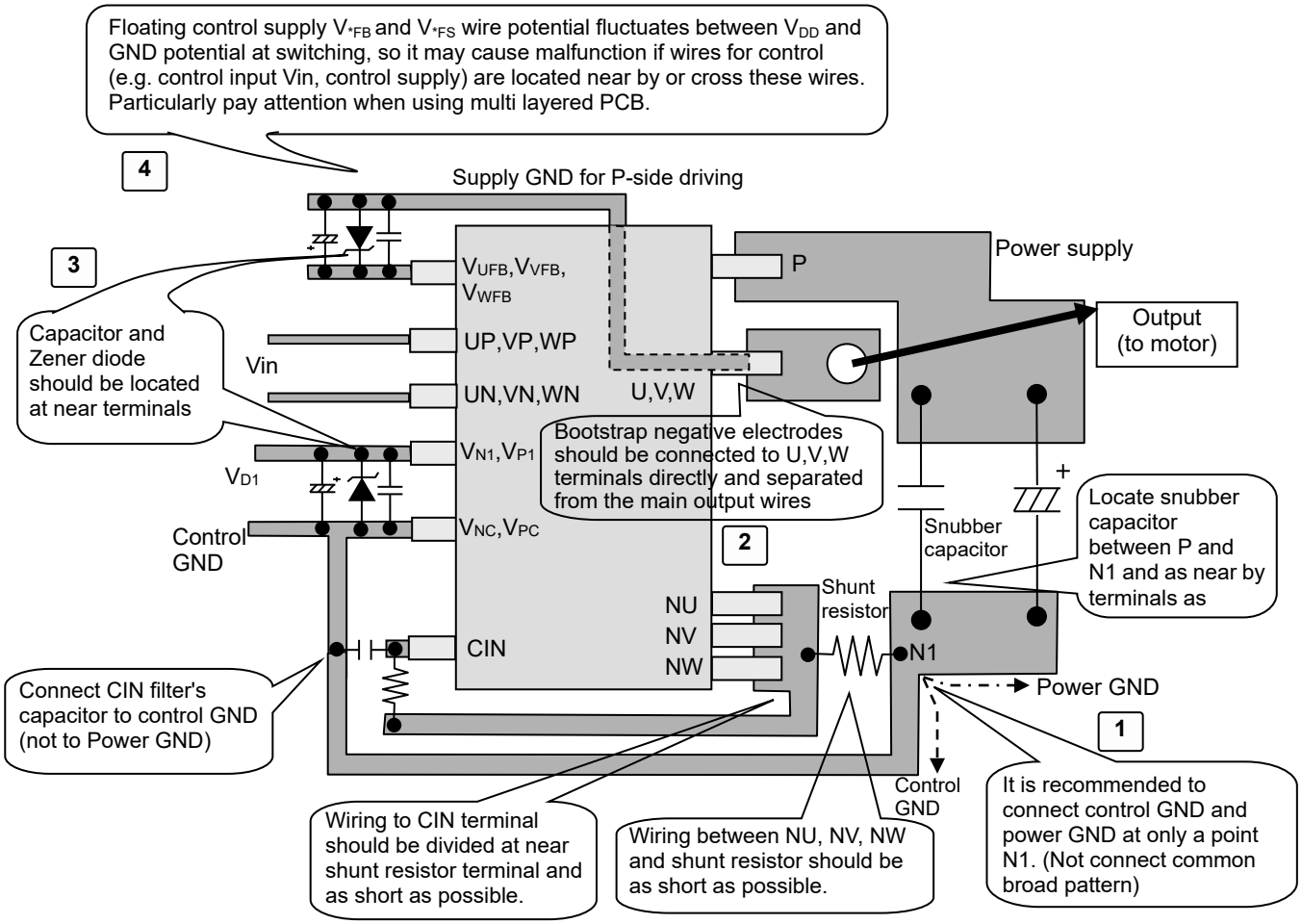


Fig.3-1-12 Precaution for wiring on PCB

Table 3-1-3 The case example of trouble due to PCB pattern

	Case example	Matter of trouble
1	•Control GND pattern overlaps power GND pattern.	The surge, generated by the wiring pattern and di/dt of noncontiguous big current flows to power GND, transfers to control GND pattern. It causes the control GND level fluctuation, so that the input signal based on the control GND fluctuates too. Then the arm short might occur.
	•Ground loop pattern exists.	Stray current flows to GND loop pattern, so that the control GND level and input signal level (based on the GND) fluctuates. Then the arm short might occur.
2	•Large inductance of wiring between N and N1 terminal	Long wiring pattern has big parasitic inductance and generates high surge when switching. This surge causes the matter as below. •HVIC malfunction due to VS voltage (output terminal potential) dropping excessively. •IC surge destruction SMD type shunt resistor, which has small parasitic inductance, is strongly recommended because of faster switching speed of MOSFET.
3	Capacitors or zener diodes are nothing or located far from the terminals.	IC surge destruction or malfunction might occur.
4	The input lines are located parallel and close to the floating supply lines for P-side drive.	Cross talk noise might be transferred through the capacitance between these floating supply lines and input lines to DIPIPM. Then incorrect signals are input to DIPIPM input, and arm short (short circuit) might occur.

3.1.9 Parallel operation of MOS DIPIPM

Fig.3-1-13 shows the circuitry of parallel connection of two DIPIPMs. Route (1) and (2) indicate the gate charging path of low-side MOSFET in DIPIPM No.1 & 2 respectively. In the case of DIPIPM 1, the parasitic inductance becomes large by long wiring and it might have a negative effect on DIPIPM's switching operation. (Chare operation of bootstrap capacitor for high-side might be affected too.) Also, such a wiring makes DIPIPM be affected by noise easily, then it might lead to malfunction. If more DIPIPMs are connected in parallel, GND pattern becomes longer and the influence to other circuit (protection circuit etc.) by the fluctuation of GND potential is conceivable, therefore parallel connection is not recommended.

Because DIPIPM doesn't consider the fluctuation of characteristics between each phases definitely, it cannot be recommended to drive same load by parallel connection with other phase MOSFET or MOSFET of other DIPIPM.

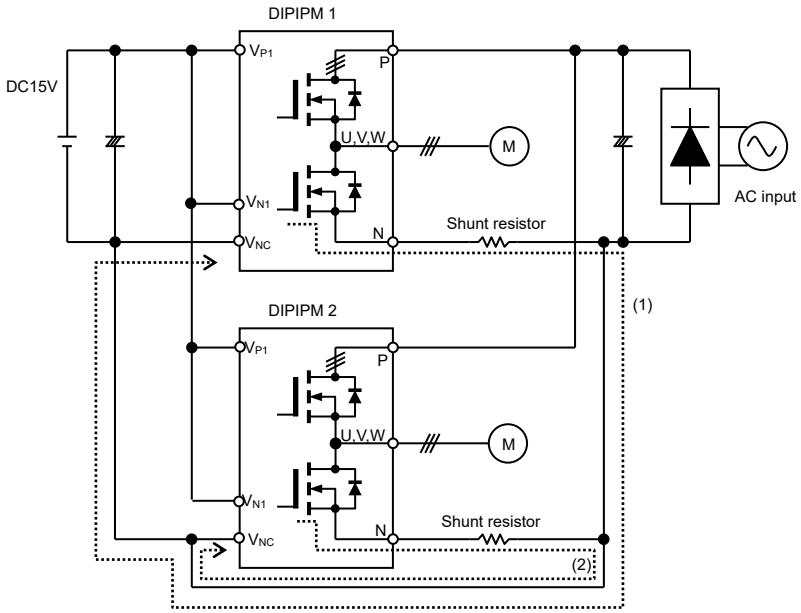


Fig.3-1-13 Parallel operation

3.1.10 SOA of MOS DIPIPM

The following describes the SOA (Safety Operating Area) of the MOS DIPIPM.

V_{DSS} : Maximum rating of MOSFET drain-source voltage

V_{DD} : Supply voltage applied on P-N terminals

$V_{DD(surge)}$: Total amount of V_{DD} and surge voltage generated by the wiring inductance and the DC-link capacitor.

$V_{DD(PROT)}$: DC-link voltage that DIPIPM can protect itself.

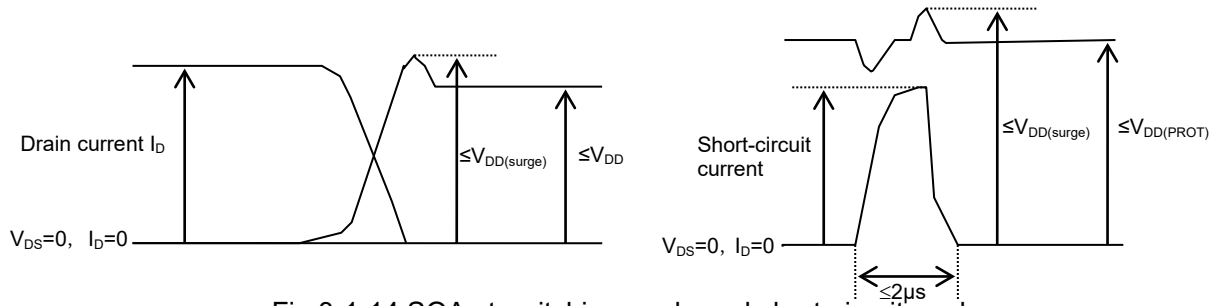


Fig.3-1-14 SOA at switching mode and short-circuit mode

In case of switching

V_{DSS} represents the maximum voltage rating (500V) of the MOSFET. By subtracting the surge voltage (50V or less) generated by internal wiring inductance from V_{DSS} is $V_{DD(surge)}$, that is 450V. Furthermore, by subtracting the surge voltage (50V or less) generated by the wiring inductor between DIPIPM and DC-link capacitor from $V_{DD(surge)}$ derives V_{DD}, that is 400V.

In case of Short-circuit

V_{DSS} represents the maximum voltage rating (500V) of the MOSFET. By subtracting the surge voltage (50V or less) generated by internal wiring inductor from V_{DSS} is $V_{DD(surge)}$, that is, 450V. Furthermore, by subtracting the surge voltage (50V or less) generated by the wiring inductor between the DIPIPM and the electrolytic capacitor from $V_{DD(surge)}$ derives V_{DD}, that is, 400V.

3.1.11 SCSOA

The typical SCSOA performance curves of MOS DIPIPM are shown as below.
(Conditions: V_{DD}=400V, Tch=125°C at initial state, V_{DD}(surge)≤450V(surge included), non-repetitive,2m load.)
In the case of PSM05S93E5, it can shut down safely an SC current that is about 12 times of its current rating under the conditions only if the MOSFET conducting period is less than 14.7μs. Since the SCSOA operation area will vary with the control supply voltage, DC-link voltage, and etc, it is necessary to set time constant of RC filter with a margin.

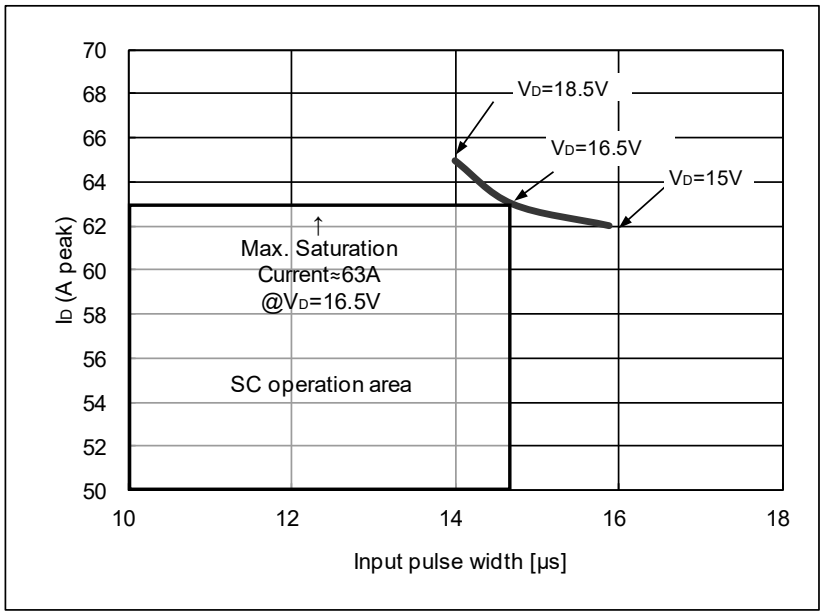


Fig.3-1-15 Typical SCSOA curve of PSM05S93E5

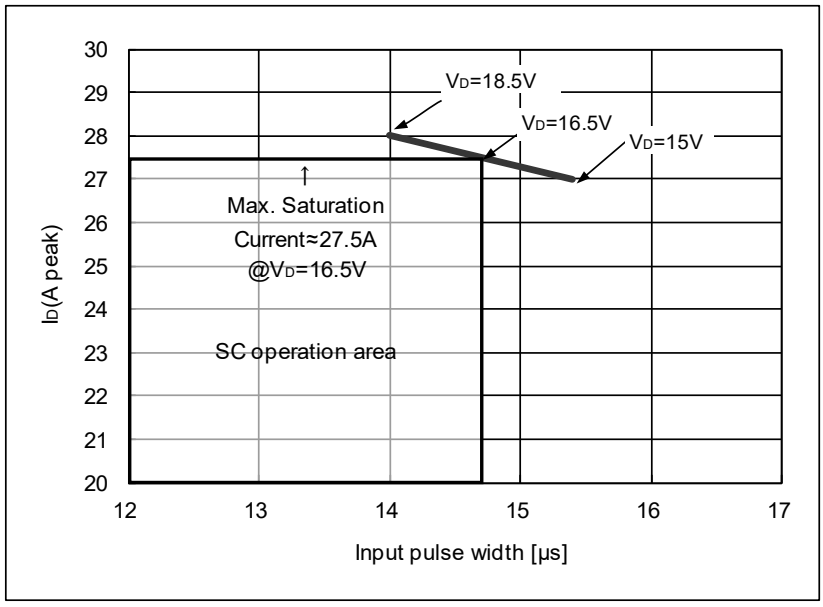


Fig.3-1-16 Typical SCSOA curve of PSM03S93E5

3.1.12 Power Life Cycles

When DIPIPM is in operation, repetitive temperature variation will happens on the MOSFET channels (ΔTch). The amplitude and the times of the channel temperature variation affect the device lifetime. Fig.3-1-17 shows the MOSFET power cycle curve as a function of average channel temperature variation (ΔTch).
(The curve is a regression curve based on 3 points of ΔTch=46, 88, 98K with regarding to failure rate of 0.1%, 1% and 10%. These data are obtained from the reliability test of intermittent conducting operation)

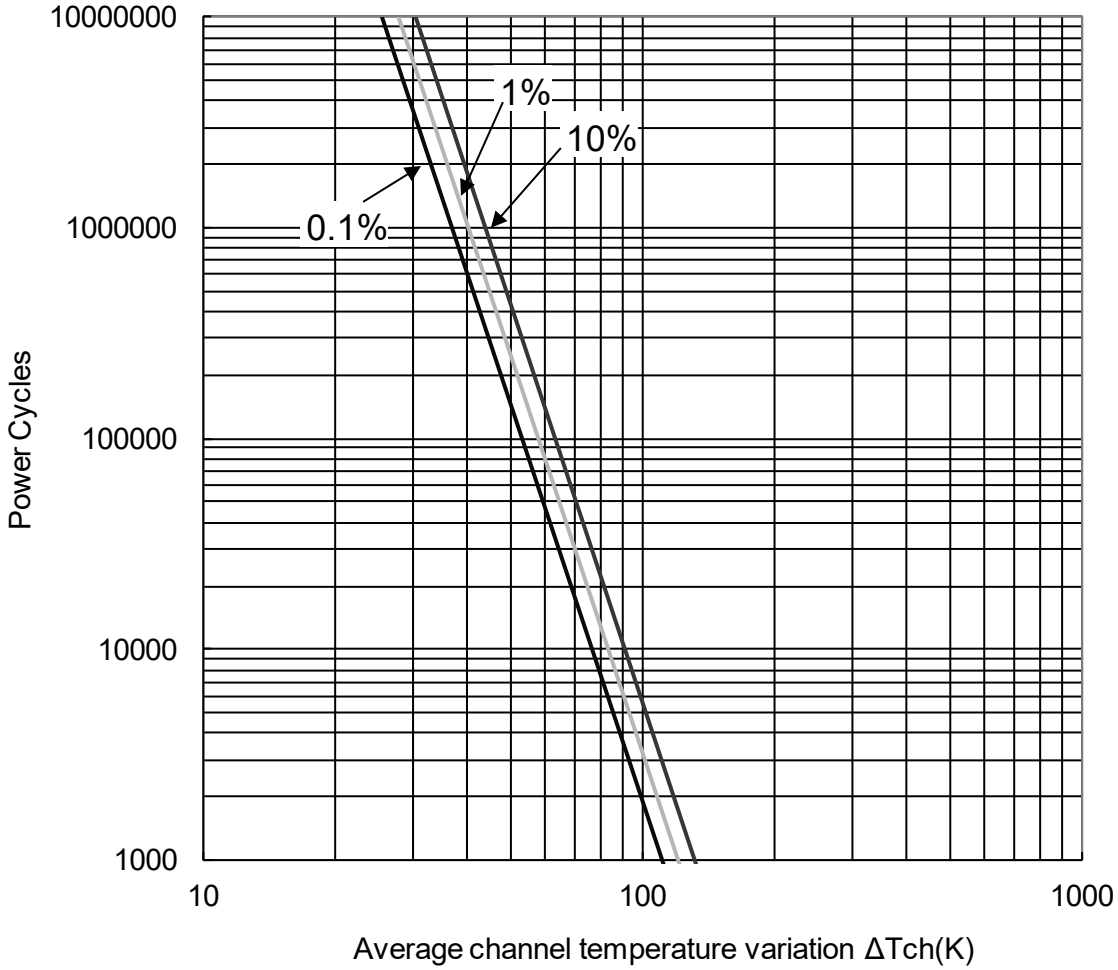


Fig.3-1-17 Power cycle curve

3.2 Power Loss and Thermal Dissipation Calculation

3.2.1 Power Loss Calculation

Simple expressions for calculating average power loss are given below:

● Scope

The power loss calculation intends to provide users a way of selecting a matched power device for their VVVF inverter application. However, it is not expected to use for limit thermal dissipation design.

● Assumptions

(1) PWM controlled VVVF inverter with sinusoidal output;
(2) PWM signals are generated by the comparison of sine waveform and triangular waveform.
(3) Duty amplitude of PWM signals varies between $\frac{1-D}{2} \sim \frac{1+D}{2}$ (%/100), (D: modulation depth).
(4) Output current various with Icp·sinx and it does not include ripple.
(5) Power factor of load output current is cosθ, ideal inductive load is used for switching.

● Expressions Derivation

PWM signal duty is a function of phase angle x as $\frac{1+\mathrm{D}\times\sin\mathrm{x}}{2}$ which is equivalent to the output voltage variation. From the power factor cosθ, the output current and its corresponding PWM duty at any phase angle x can be obtained as below:

$$Output\ \ current = I_{DP} \times \sin x$$

$$PWM\ \ \ Duty = \frac{1 + D \times \sin(x + \theta)}{2}$$

Then, V_{DS} and V_{SD} at the phase x can be calculated by using a linear approximation:

$$V_{DS} = V_{DS}(@\, I_{DP} \times \sin x)$$

$$V_{SD} = (-1) \times V_{SD}(@\, I_{SDP}(= I_{DP}) \times \sin x)$$

Thus, the static loss of Tr part of MOSFET is given by:

$$\frac{1}{2\pi}\int_0^{\pi} (I_{DP} \times \sin x) \times V_{DS} @\, I_{DP} \times \sin x) \times \frac{1 + D\sin(x + \theta)}{2} \bullet dx$$

Similarly, the static loss of free-wheeling diode part is given by:

$$\frac{1}{2\pi}\int_{\pi}^{2\pi} ((-1) \times I_{DP} \times \sin x)((-1) \times V_{SD}(@\, I_{DP} \times \sin x) \times \frac{1 + D\sin(x + \theta)}{2} \bullet dx$$

On the other hand, the dynamic loss of Tr part of MOSFET, which does not depend on PWM duty, is given by:

$$\frac{1}{2\pi}\int_0^{\pi} (Psw(on)(@\, I_{DP} \times \sin x) + Psw(off)(@\, I_{DP} \times \sin x)) \times fc \bullet dx$$

Recovery loss of FWDi part can be approximated by the ideal wave form shown in Fig.3-2-1, and its dynamic loss can be calculated by the following expression:

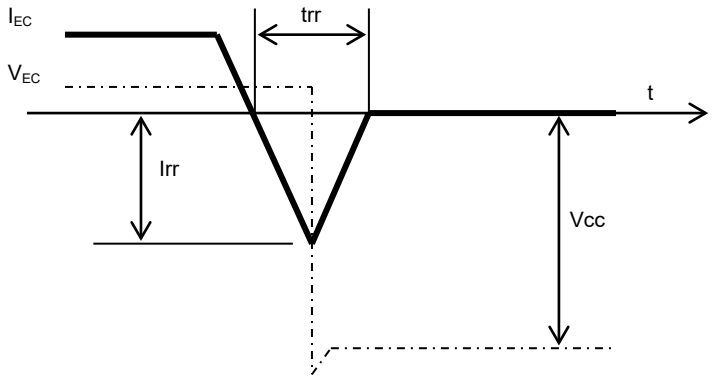


Fig.3-2-1 Ideal FWDi part recovery wave form

$$Psw = \frac{Irr \times V_{DD} \times trr}{4}$$

Recovery occurs only in the half cycle of the output current, thus the dynamic loss is calculated by:

$$\frac{1}{2}\int_{\pi}^{2\pi} \frac{Irr(@\, I_{DP} \times \sin x) \times V_{DD} \times trr(@\, I_{DP} \times \sin x)}{4} \times fc \bullet dx$$

$$= \frac{1}{8}\int_{\rho}^{2\pi} Irr(@\, I_{DP} \times \sin x) \times V_{DD} \times trr(@\, I_{DP} \times \sin x) \times fc \bullet dx$$

- Attention of applying the power loss simulation for inverter designs

  - Divide the output current period into fine-steps and calculate the losses at each step based on the actual values of PWM duty, output current, V_{DS}, V_{SD}, and Psw corresponding to the output current. The worst condition is most important.
  - PWM duty depends on the signal generating way.
  - The relationship between output current waveform or output current and PWM duty changes with the way of signal generating, load, and other various factors. Thus, calculation should be carried out on the basis of actual waveform data.
  - MOSFET works as Tr and Di by one chip, so its loss becomes the sum of Tr part and Di part loss.
  - V_{DS},V_{SD} and Psw(on, off) should be the values at Tch=125°C.

3.2.2 Temperature Rise Considerations and Calculation Example

Fig.3-2-2 shows the typical characteristics of allowable motor rms current versus carrier frequency under the following inverter operating conditions based on power loss simulation results.

Conditions: V_{DD}=300V, V_D=V_{DB}=15V, $V_{CE(sat)}$=Typ., Switching loss=Typ., Tch=125°C, Tf=100°C, Rth(j-c)=Max., Rth(c-f)=0.3K/W (per 1/6 module), P.F=0.8, 3-phase PWM modulation, 60Hz sine waveform output

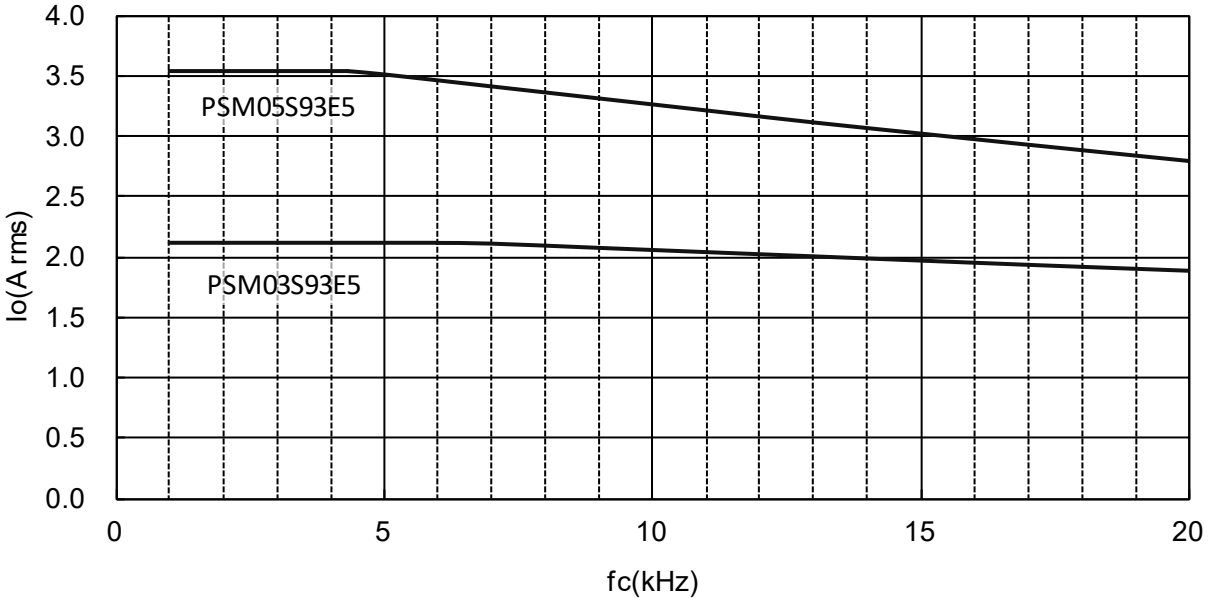


Fig.3-2-2 Effective current-carrier frequency characteristics

Fig.3-2-2 shows an example of estimating allowable inverter output rms current under different carrier frequency and permissible maximum operating temperature condition (Tf=100°C. Tch=125°C). The results may change for different control strategy and motor types. Anyway please ensure that there is no large current over device rating flowing continuously.

Inverter loss can be calclated by the free power loss simulation software will be uploaded to the web site. URL: http://www.mitsubishielectric.com/semiconductors/

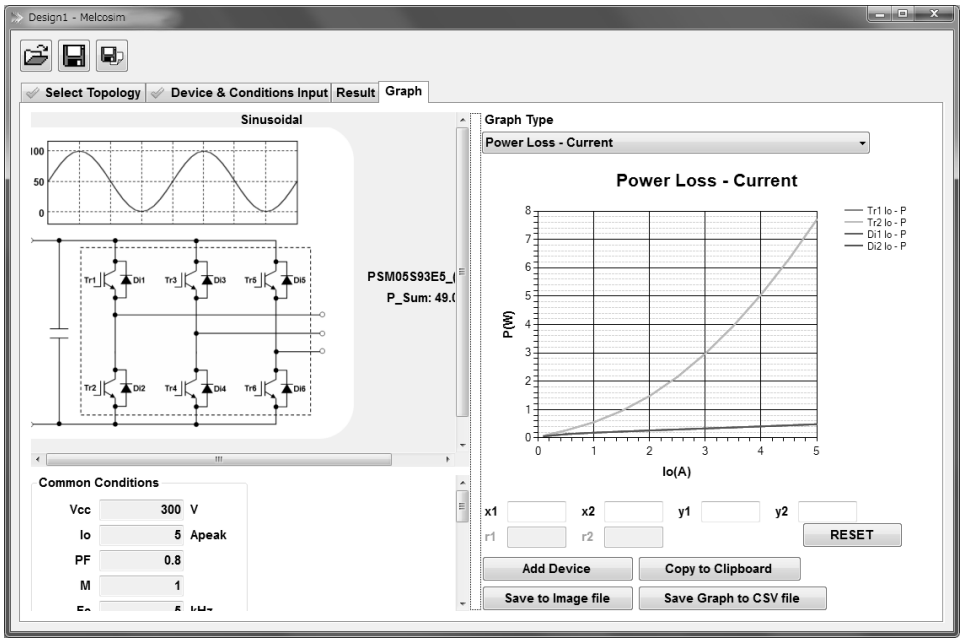


Fig.3-2-3 Loss simulator screen image

3.3 Noise and ESD Withstand Capability

3.3.1 Evaluation Circuit of Noise Withstand Capability

MOS DIPIPM series have been confirmed to be with over +/-2.0kV noise withstand capability by the noise evaluation under the conditions shown in Fig.3-3-1. However, noise withstand capability greatly depends on the test environment, the wiring patterns of control substrate, parts layout, and other factors; therefore an additional confirmation on prototype is necessary.

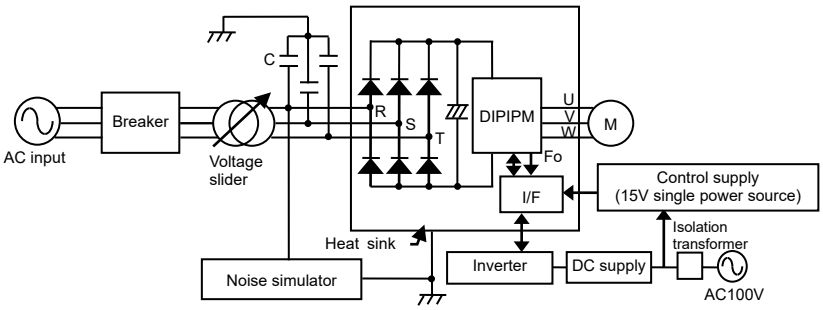


Fig.3-3-1 Noise withstand capability evaluation circuit

Note:

C1: AC line common-mode filter 4700pF, PWM signals are input from microcomputer by using opto-couplers, 15V single power supply, Test is performed with IM

Test conditions

V_{DD}=300V, V_D=15V, Ta=25°C, no load

Scheme of applying noise: From AC line (R, S, T), Period T=16ms, Pulse width tw=0.05-1μs, input in random.

3.3.2 Countermeasures and Precautions

MOS DIPIPM improves noise withstand capabilities by means of reducing parts quantity, lowering internal wiring parasitic inductance, and reducing leakage current. But when the noise affects on the control terminals of DIPIPM (due to wiring pattern on PCB), the short circuit or malfunction of SC protection may occur. In that case, below countermeasures are recommended.

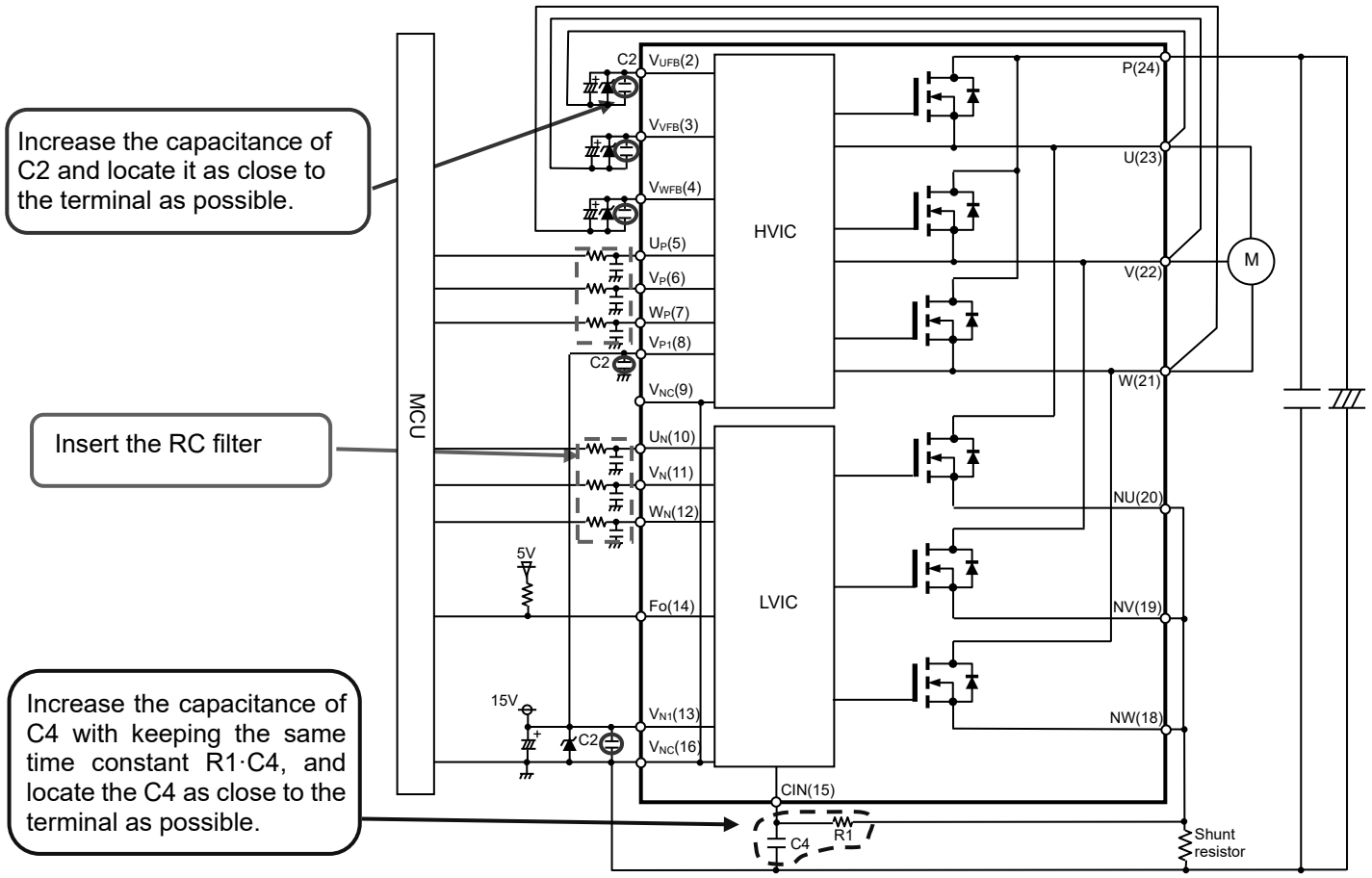


Fig.3-3-2 Example of countermeasures for inverter part

3.3.3 Static Electricity Withstand Capability

Withstand capability against static electricity is confirmed by the following tests shown in Fig.3-3-3, 4. The results (typical data) are described in Table 3-3-1.

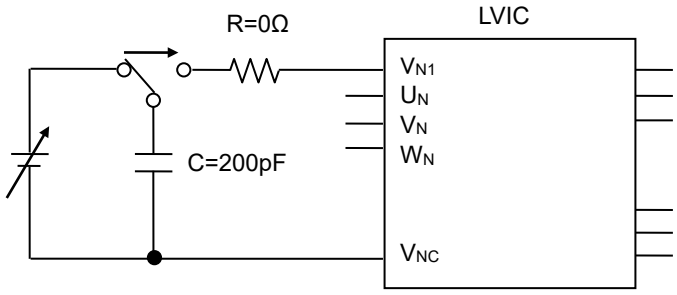


Fig.3-3-3 LVIC terminal Surge Test circuit

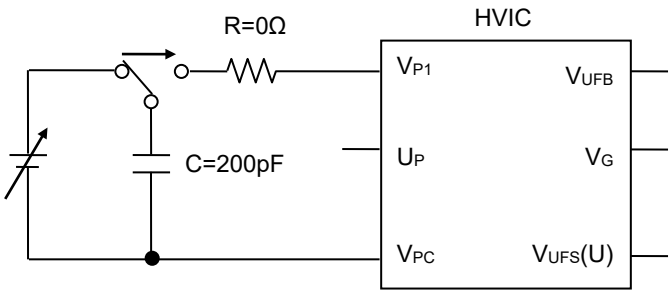


Fig.3-3-4 HVIC terminal Surge Test circuit

Conditions: Surge voltage increases by degree and only one-shot surge pulse is impressed at each surge voltage. (Limit voltage of surge simulator: ±4.0kV, Judgment method; change in V-I characteristic)

Table 3-3-1 Typical ESD capability

[Control terminal part] Common data for PSM03/PSM05 because of all types have same interface circuit.

Terminals	+	-
UP, VP, WP-V_{NC}	0.6	0.7
V_{P1} – V_{NC}	1.3	1.1
V_{UFB}-U, V_{VFB}-V,V_{WFB}-W	1.5	1.9
UN, VN, WN-V_{NC}	0.6	0.6
V_{N1}-V_{NC}	4.0 or more	2.8
CIN-V_{NC}	0.3	0.5
Fo-V_{NC}	0.5	1.1

[Power terminal part]
PSM05S93E5

Terminals	+	-
P-NU,NV,NW	1.8	3.2
U-NU, V-NV, W-NW	4.0 or more	4.0 or more

PSM03S93E5

Terminals	+	-
P-NU,NV,NW	1.4	3.9
U-NU, V-NV, W-NW	4.0 or more	4.0 or more

CHAPTER 4 Bootstrap Circuit Operation

4.1 Bootstrap Circuit Operation

For three phase inverter circuit driving, normally four isolated control supplies (three for P-side driving and one for N-side driving) are necessary. But using floating control supply with bootstrap circuit can reduce the number of isolated control supplies from four to one (N-side control supply).

Bootstrap circuit consists of a bootstrap diode(BSD), a bootstrap capacitor(BSC) and a current limiting resistor. (MOSFET Super mini DIPIPM series integrates BSD and limiting resistor and can make bootstrap circuit by adding outer BSC only.) It uses the BSC as a control supply for driving P-side MOSFET. The BSC supplies gate charge when P-side MOSFET turning ON and circuit current of logic circuit on P-side driving IC. (Fig.4-1-2) Since a capacitor is used as substitute for isolated supply, its supply capability is limited. This floating supply driving with bootstrap circuit is suitable for small supply current products like DIPIPM.

Charge consumed by driving circuit is re-charged from N-side 15V control supply to BSC via current limiting resistor and BSD when voltage of output terminal (U, V or W) goes down to GND potential in inverter operation. But there is the possibility that enough charge doesn't perform due to the conditions such as switching sequence, capacitance of BSC and so on. Deficient charge leads to low voltage of BSC and might work under voltage protection (UV). This situation makes the loss of P-side MOSFET increase by low gate voltage or stop switching. So it is necessary to consider and evaluate enough for designing bootstrap circuit. For more detail information about driving by the bootstrap circuit, refer the DIPIPM application note "*Bootstrap Circuit Design Manual*"

The BSD characteristics for MOSFET Super mini DIPIPM series and the circuit current characteristics in switching situation of P-side MOSFET are described as below.

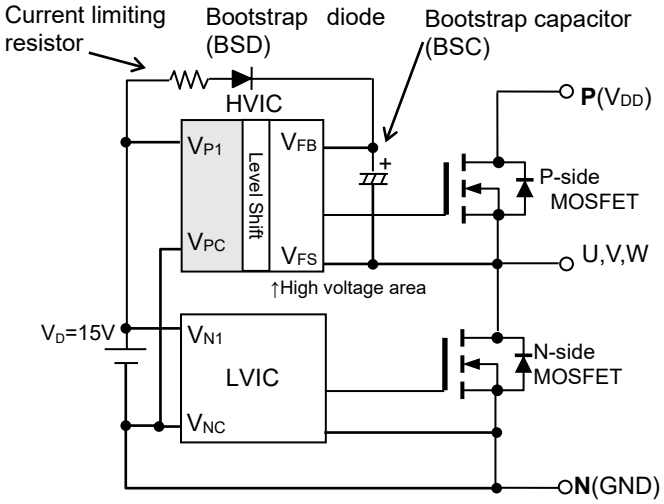


Fig.4-1-1 Bootstrap Circuit Diagram

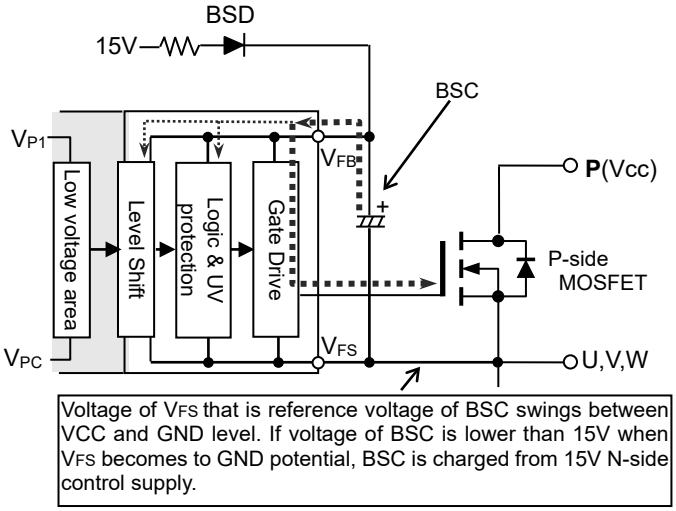


Fig.4-1-2 Bootstrap Circuit Diagram

4.2 Bootstrap Supply Circuit Current at Switching State

Bootstrap supply circuit current I_{DB} at steady state is maximum 0.1mA for this series. But at switching state, because gate charge and discharge are repeated by switching, the circuit current exceeds 0.1mA and increases proportional to carrier frequency. For reference, Fig.4-2-1,2 show I_{DB} - carrier frequency fc characteristics for PSM05S93E5 and PSM03S93E5.

Conditions: V_D=V_{DB}=15V, Tch=125°C, MOSFET ON Duty=10, 30, 50, 70, 90%

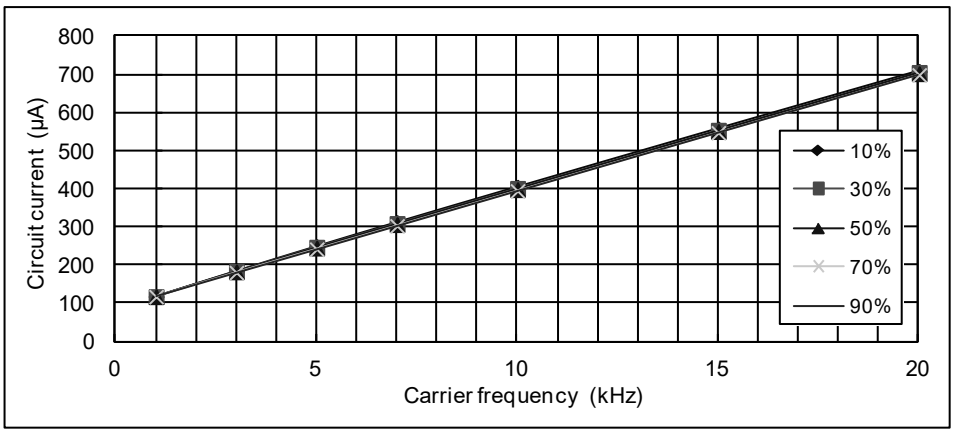


Fig.4-2-1 I_{DB} vs. Carrier frequency for PSM05S93E5

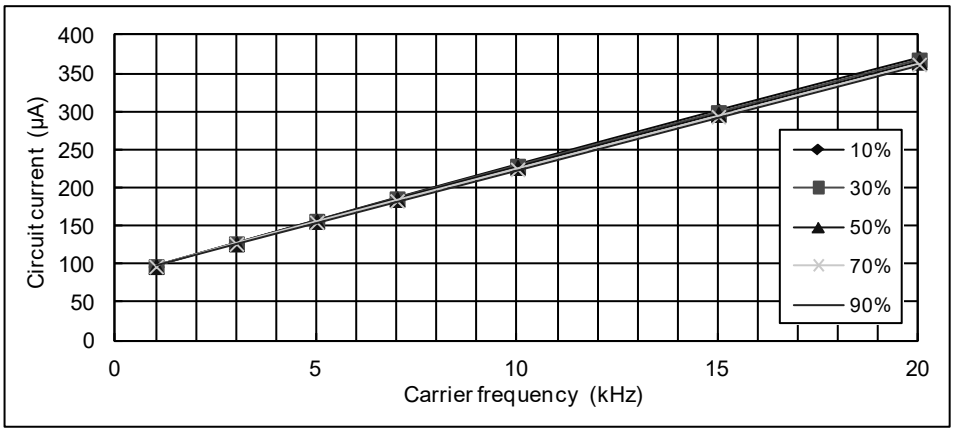


Fig.4-2-2 I_{DB} vs. Carrier frequency for PSM03S93E5

4.3 Note for designing the bootstrap circuit

When each device for bootstrap circuit is designed, it is necessary to consider various conditions such as temperature characteristics, change by lifetime, variation and so on. Note for designing these devices are listed as below. For more detail information about driving by the bootstrap circuit, refer the DIPIPM application note "*Bootstrap Circuit Design Manual*"

(1) Bootstrap capacitor

Electrolytic capacitors are used for BSC generally. And recently ceramic capacitors with large capacitance are also applied. But DC bias characteristic of the ceramic capacitor when applying DC voltage is considerably different from that of electrolytic capacitor. (Especially large capacitance type) Some differences of capacitance characteristics between electrolytic and ceramic capacitors are listed in Table 4-3-1.

Table 4-3-1 Differences of capacitance characteristics between electrolytic and ceramic capacitors

	Electrolytic capacitor	Ceramic capacitor (large capacitance type)
Temperature characteristics (Ta:-20~ 85°C)	• Aluminum type: Low temp.: -10% High temp: +10% • Conductive polymer aluminum solid type: Low temp.: -5% High temp: +10%	Different due to temp. characteristics rank Low temp.: -5%~0% High temp.: -5%~-10% (in the case of B,X5R,X7R ranks)
DC bias characteristics (Applying DC15V)	Nothing within rating voltage	Different due to temp. characteristics, rating voltage, package size and so on **-70%**~-15%

DC bias characteristic of electrolytic capacitor is not matter. But it is necessary to note ripple capability by repetitive charge and discharge, life time which is greatly affected by ambient temperature and so on. Above characteristics are just example data which are obtained from the WEB, please refer to the capacitor manufacturers about detailed characteristics.

(2) Bootstrap diode

MOS DIPIPM integrates bootstrap diode for P-side driving supply. This BSD incorporates current limiting resistor (typ. 100Ω). The V_F-I_F characteristics (including voltage drop by built-in current limiting resistor) is shown in Fig.4-3-1 and Table 4-3-2.

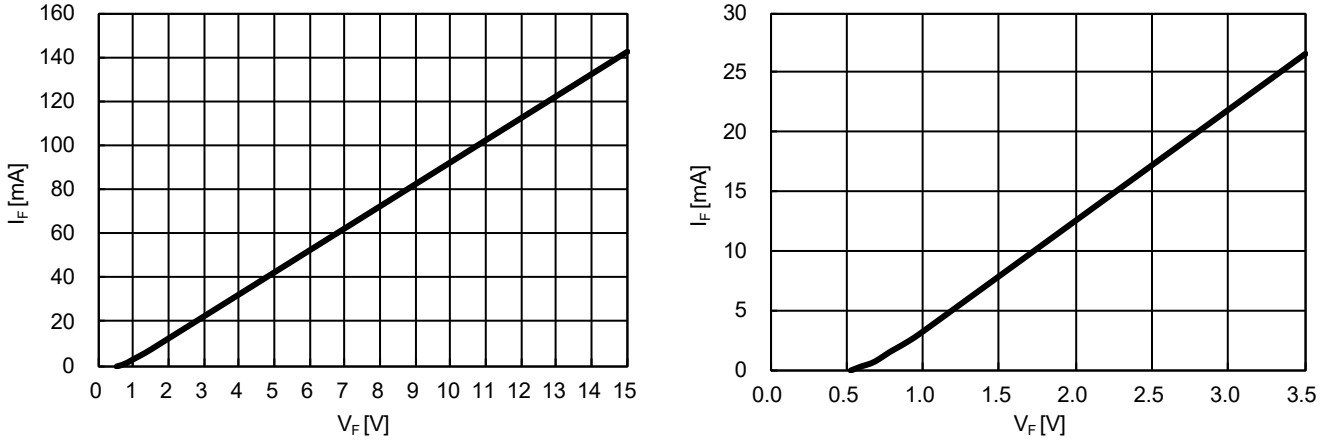


Fig.4-3-1 V_F-I_F curve for bootstrap Diode (The right figure is enlarged view)

Table 4-3-2 Electric characteristics of built-in bootstrap diode

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Bootstrap Di forward voltage	V_F	I_F=10mA including voltage drop by limiting resistor	1.1	1.7	2.3	V
Built-in limiting resistance	R	Included in bootstrap Di	80	100	120	Ω

4.4 Initial charging in bootstrap circuit

In the case of applying bootstrap circuit, it is necessary to charge to the BSC initially because voltage of BSC is 0V at initial state or it may go down to the trip level of under voltage protection after long suspending period (even 1s). BSC charging is performed by turning on all N-side MOSFET normally. When outer load (e.g. motor) is connected to the DIPIPM, BSC charging may be performed by turning on only one phase N-side MOSFET since potential of all output terminals will go down to GND level through the wiring in the motor. But its charging efficiency might become lower due to some cause. (e.g. wiring resistance of motor)

There are mainly two procedures for BSC charging. One is performed by one long pulse, and another is conducted by multiple short pulses. Multi pulse method is used when there are some restriction like control supply capability and so on.

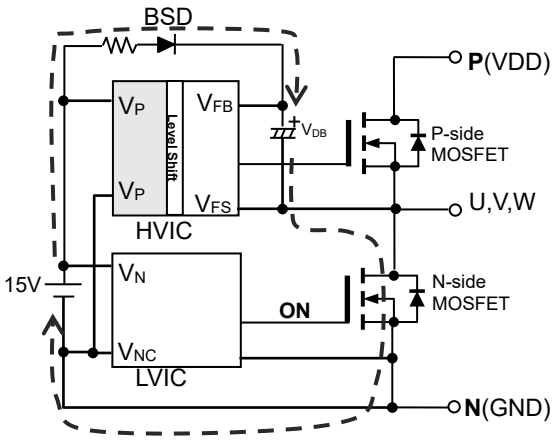


Fig.4-4-1 Initial charging root

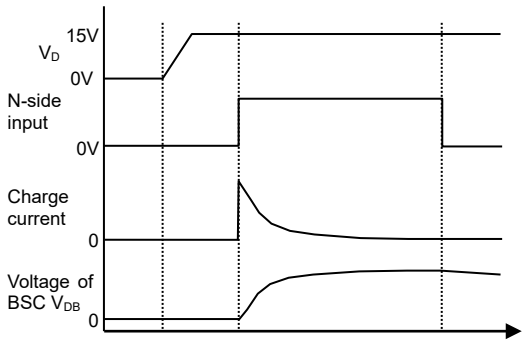


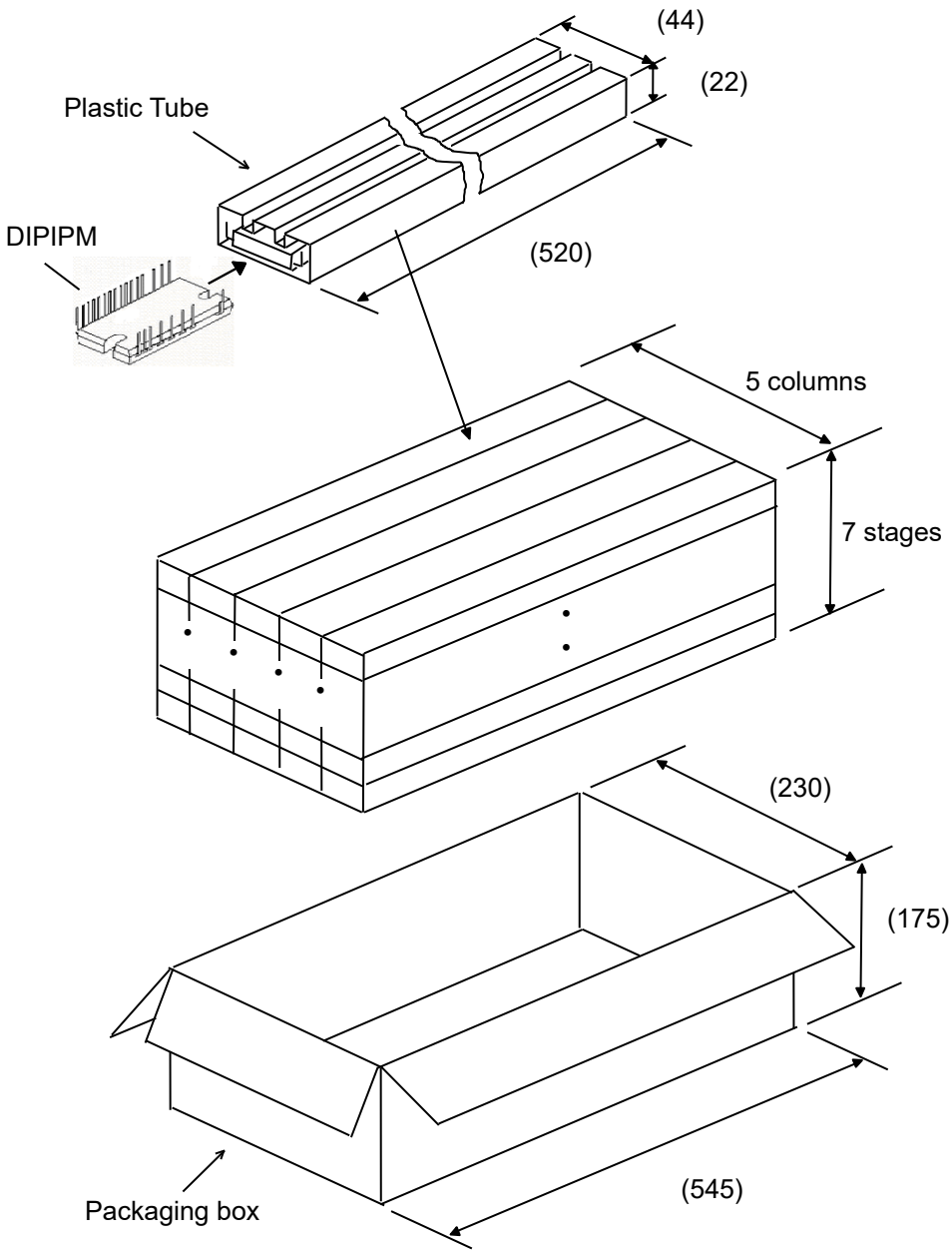
Fig.4-4-2 Example of waveform by one charging pulse

Initial charging needs to be performed until voltage of BSC exceeds recommended minimum supply voltage 13V. (It is recommended to charge as high as possible with consideration for voltage drop between the end of charging and start of inverter operation.)

After BSC was charged, it is recommended to input one ON pulse to the P-side input for reset of internal IC state before starting system. Iput pulse width is needed to be longer than allowable minimum input pulse width PWIN(on). (e.g. 0.7μs or more for MOSFET Super mini DIPIPM.)

CHAPTER 5 PACKAGE HANDLING

5.1 Packaging Specification



Quantity:

12pcs per 1 tube

Total amount in one box (max):

Tube Quantity: 5 × 7=35pcs
IPM Quantity: 35 × 12=420pcs

When it isn't fully filled by tubes at top stage, cardboard spacers or empty tubes are inserted for filling the space of top stage.

Weight (max):

About 8.5g per 1pcs of DIPIPM
About 200g per 1 tube
About 8.3kg per 1 box

Spacers are put on the top and bottom of the box. If there is some space on top of the box, additional buffer materials are also inserted.

Fig.5-1 Packaging Specification

5.2 Handling Precautions

⚠ Cautions	
Transportation	・Put package boxes in the correct direction. Putting them upside down, leaning them or giving them uneven stress might cause electrode terminals to be deformed or resin case to be damaged. ・Throwing or dropping the packaging boxes might cause the devices to be damaged. ・Wetting the packaging boxes might cause the breakdown of devices when operating. Pay attention not to wet them when transporting on a rainy or a snowy day.
Storage	・We recommend temperature and humidity in the ranges 5-35°C and 45-75%, respectively, for the storage of modules. The quality or reliability of the modules might decline if the storage conditions are much different from the above.
Long storage	・When storing modules for a long time (more than one year), keep them dry. Also, when using them after long storage, make sure that there is no visible flaw, stain or rust, etc. on their exterior.
Surroundings	・Keep modules away from places where water or organic solvent may attach to them directly or where corrosive gas, explosive gas, fine dust or salt, etc. may exist. They might cause serious problems.
Flame resistance	・The epoxy resin and the case materials are flame-resistant type (UL standard 94-V0), but they are not noninflammable.
Static electricity	・ICs and power chips with MOS gate structure are used for the DIPIPM power modules. Please keep the following notices to prevent modules from being damaged by static electricity. (1)Precautions against the device destruction caused by the ESD When the ESD of human bodies, packaging and etc. are applied to terminal, it may damage and destroy devices. The basis of anti-electrostatic is to inhibit generating static electricity possibly and quick dissipation of the charged electricity. ・Containers that charge static electricity easily should not be used for transit and for storage. ・Terminals should be always shorted with a carbon cloth or the like until just before using the module. Never touch terminals with bare hands. ・Should not be taking out DIPIPM from tubes until just before using DIPIPM and never touch terminals with bare hands. ・During assembly and after taking out DIPIPM from tubes, always earth the equipment and your body. It is recommended to cover the work bench and its surrounding floor with earthed conductive mats. ・When the terminals are open on the printed circuit board with mounted modules, the modules might be damaged by static electricity on the printed circuit board. ・If using a soldering iron, earth its tip. (2)Notice when the control terminals are open ・When the control terminals are open, do not apply voltage between the drain and source. It might cause malfunction. ・Short the terminals before taking a module off.

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