# PCA8546

## 4 x 44 automotive LCD driver

**Rev. 2 — 29 September 2021**                                          **Product data sheet**

## 1  General description

The PCA8546 is a peripheral device which generates the drive signals for any multiplexed LCD containing up to four backplanes, and up to 176 elements. The PCA8546 is compatible with most microcontrollers and communicates via the two-line bidirectional I$^2$C-bus (PCA8546A) or a three line unidirectional SPI-bus (PCA8546B). Communication overheads are minimized using a display RAM with auto-incremented addressing.

For a selection of NXP LCD segment drivers, see Table 37.

## 2  Features and benefits

- AEC-Q100 grade 3 compliant for automotive applications
- Single-chip 176 elements LCD controller and driver
- Wide range for digital power supply: from 1.8 V to 5.5 V
- LCD supply range from 2.5 V up to 9 V
- LCD and logic supplies may be separated
- Low power consumption
- Four backplanes and selectable display bias configuration
- On-chip RAM for display data storage
- 400 kHz I$^2$C-bus interface (PCA8546A)
- 5 MHz SPI-bus interface (PCA8546B)
- Programmable frame frequency in the range of 60 Hz to 300 Hz in steps of about 10 Hz; factory calibrated
- 176 segments driven allowing:
    - up to 22 7-segment alphanumeric characters
    - up to 11 14-segment alphanumeric characters
    - any graphics of up to 176 elements
- Manufactured in silicon gate CMOS process
- Extended operating temperature range up to 95 °C

## 3  Applications

- Climate control
- Car radio
- Dashboard display

## 4 Ordering information

**Table 1. Ordering information**

| Type number | Interface type | Topside mark | Package | | |
|---|---|---|---|---|---|
| | | | **Name** | **Description** | **Version** |
| PCA8546ATT/A | I$^2$C-bus | PCA8546ATT | TSSOP56 | plastic thin shrink small outline package; 56 leads; body width 6.1 mm | SOT364-1 |
| PCA8546BTT/A | SPI-bus | PCA8546BTT | TSSOP56 | plastic thin shrink small outline package; 56 leads; body width 6.1 mm | SOT364-1 |

### 4.1 Ordering options

**Table 2. Ordering options**

| Type number | Orderable part number | Package | Packing method[1] | Minimum order quantity | Temperature |
|---|---|---|---|---|---|
| PCA8546ATT/A | PCA8546ATT/AJ[2] | TSSOP56 | reel 13 inch q1 non dry pack | 2000 | $T_{amb}$ = -40 °C to +95 °C |
| | PCA8546ATT/AY | TSSOP56 | reel 13 inch q1 dry pack | 2000 | $T_{amb}$ = -40 °C to +95 °C |
| PCA8546BTT/A | PCA8546BTT/AJ[3] | TSSOP56 | reel 13 inch q1 non dry pack | 2000 | $T_{amb}$ = -40 °C to +95 °C |
| | PCA8546BTT/AY | TSSOP56 | reel 13 inch q1 dry pack | 2000 | $T_{amb}$ = -40 °C to +95 °C |

[1] Standard packing quantities and other packaging data are available at www.nxp.com/packages/.
[2] Discontinuation Notice 202107021DN - drop in replacement is PCA8546ATT/AY - this is documented in PCN202102010F01.
[3] Discontinuation Notice 202107021DN - drop in replacement is PCA8546BTT/AY - this is documented in PCN202102010F01.

PCA8546

**Product data sheet** **Rev. 2 — 29 September 2021**
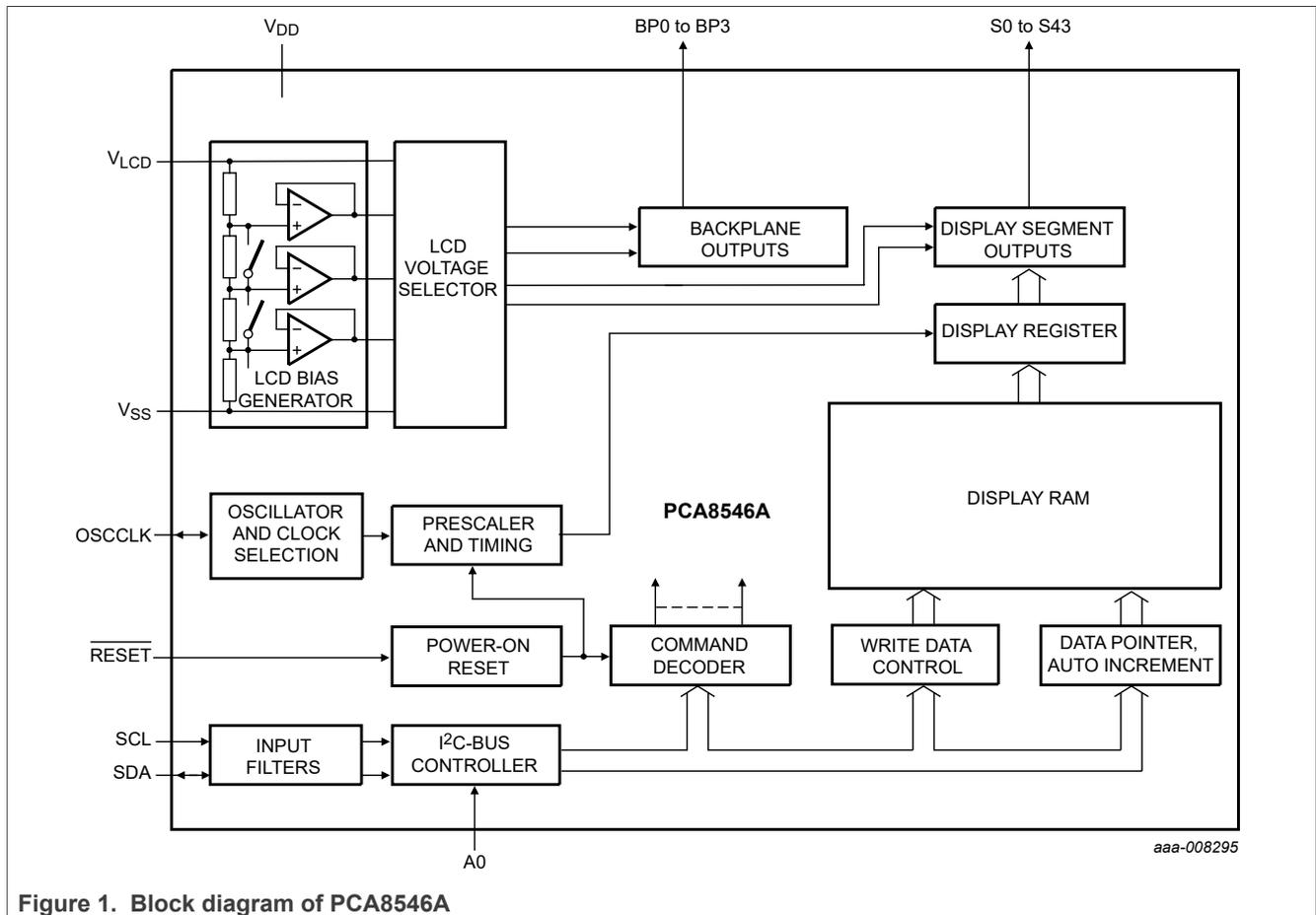
2 / 60

## 5    Block diagram



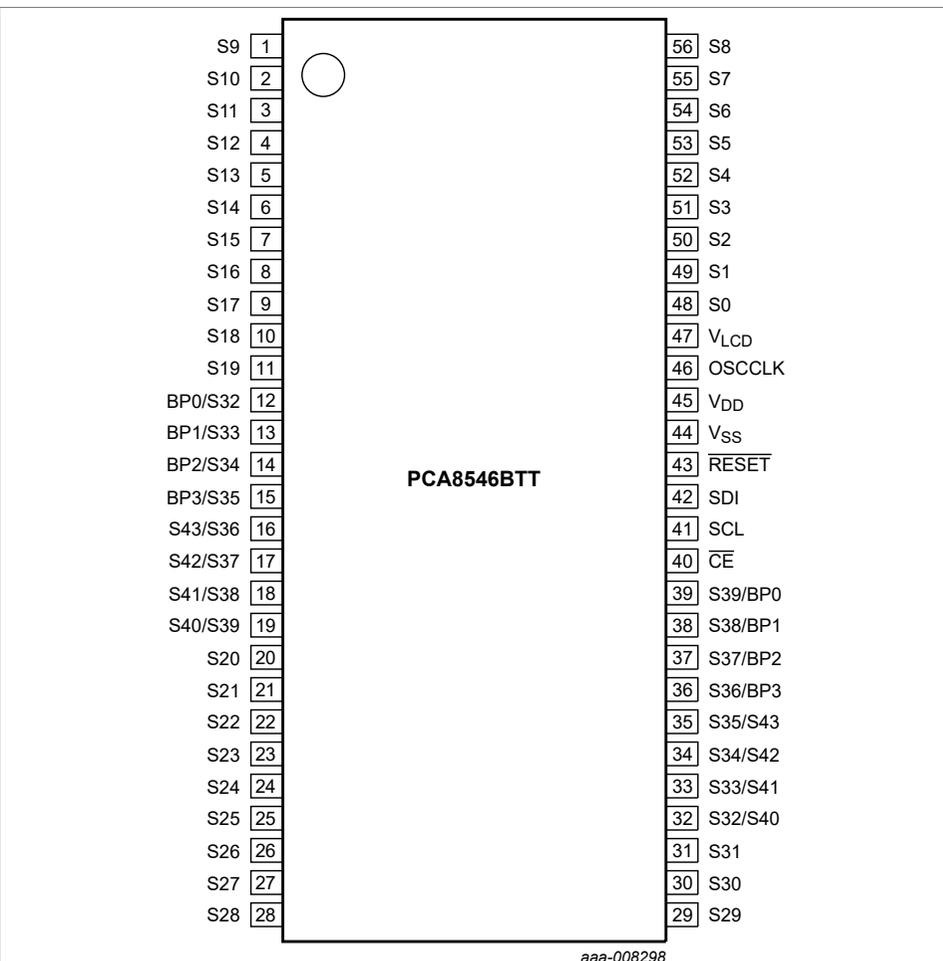**Figure 1. Block diagram of PCA8546A**
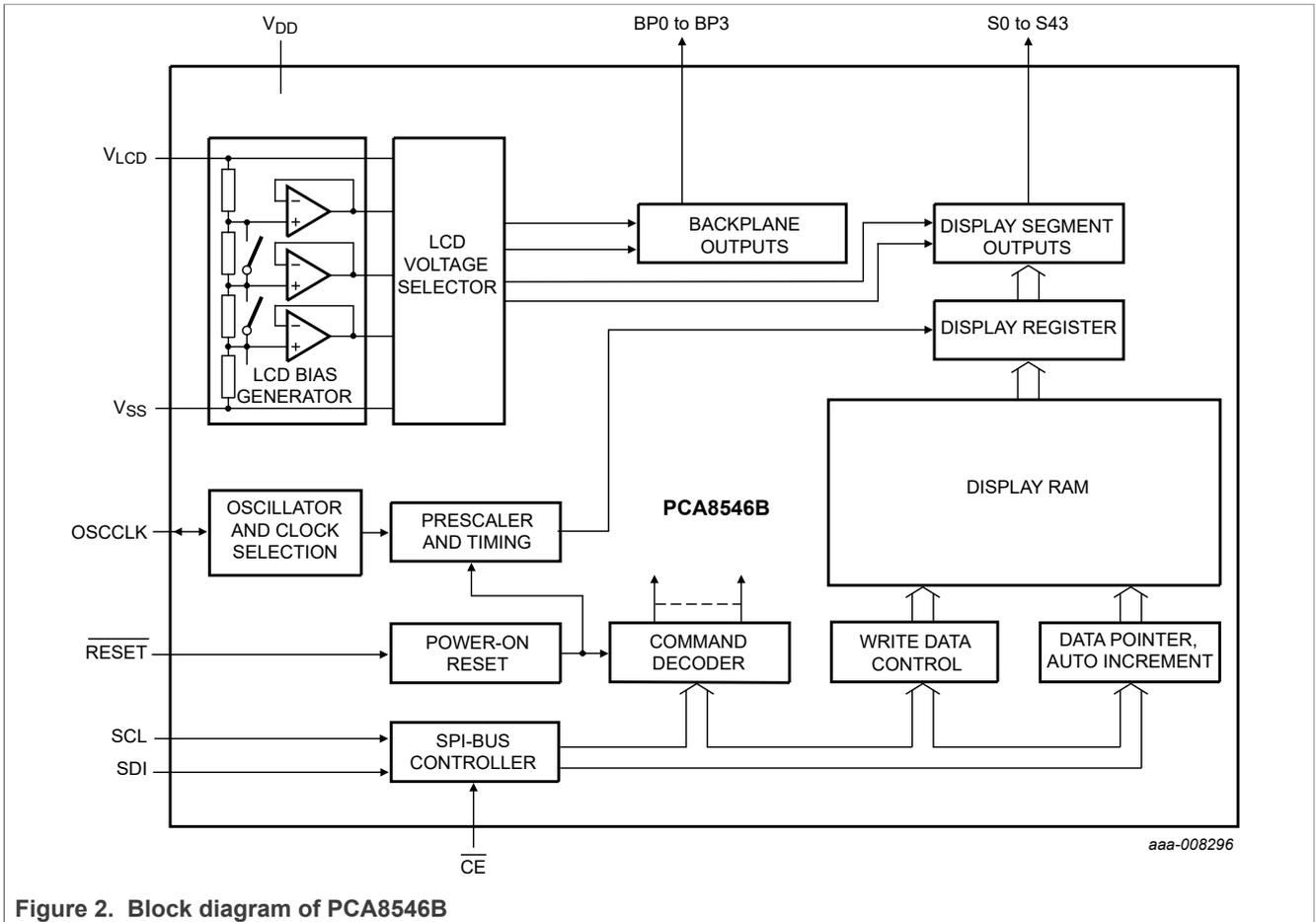
Figure 2. Block diagram of PCA8546B

# 6 Pinning information

## 6.1 Pinning

| S9 | 1 | | 56 | S8 |
| S10 | 2 | | 55 | S7 |
| S11 | 3 | | 54 | S6 |
| S12 | 4 | | 53 | S5 |
| S13 | 5 | | 52 | S4 |
| S14 | 6 | | 51 | S3 |
| S15 | 7 | | 50 | S2 |
| S16 | 8 | | 49 | S1 |
| S17 | 9 | | 48 | S0 |
| S18 | 10 | | 47 | $V_{LCD}$ |
| S19 | 11 | | 46 | OSCCLK |
| BP0/S32 | 12 | | 45 | $V_{DD}$ |
| BP1/S33 | 13 | | 44 | $V_{SS}$ |
| BP2/S34 | 14 | **PCA8546ATT** | 43 | $\overline{RESET}$ |
| BP3/S35 | 15 | | 42 | SDA |
| S43/S36 | 16 | | 41 | SCL |
| S42/S37 | 17 | | 40 | A0 |
| S41/S38 | 18 | | 39 | S39/BP0 |
| S40/S39 | 19 | | 38 | S38/BP1 |
| S20 | 20 | | 37 | S37/BP2 |
| S21 | 21 | | 36 | S36/BP3 |
| S22 | 22 | | 35 | S35/S43 |
| S23 | 23 | | 34 | S34/S42 |
| S24 | 24 | | 33 | S33/S41 |
| S25 | 25 | | 32 | S32/S40 |
| S26 | 26 | | 31 | S31 |
| S27 | 27 | | 30 | S30 |
| S28 | 28 | | 29 | S29 |

aaa-008297

Top view. For mechanical details, see Figure 39.

**Figure 3. Pin configuration for TSSOP56 (PCA8546ATT)**

| S9 | 1 | | 56 | S8 |
| S10 | 2 | | 55 | S7 |
| S11 | 3 | | 54 | S6 |
| S12 | 4 | | 53 | S5 |
| S13 | 5 | | 52 | S4 |
| S14 | 6 | | 51 | S3 |
| S15 | 7 | | 50 | S2 |
| S16 | 8 | | 49 | S1 |
| S17 | 9 | | 48 | S0 |
| S18 | 10 | | 47 | $V_{LCD}$ |
| S19 | 11 | | 46 | OSCCLK |
| BP0/S32 | 12 | | 45 | $V_{DD}$ |
| BP1/S33 | 13 | | 44 | $V_{SS}$ |
| BP2/S34 | 14 | **PCA8546BTT** | 43 | $\overline{RESET}$ |
| BP3/S35 | 15 | | 42 | SDI |
| S43/S36 | 16 | | 41 | SCL |
| S42/S37 | 17 | | 40 | $\overline{CE}$ |
| S41/S38 | 18 | | 39 | S39/BP0 |
| S40/S39 | 19 | | 38 | S38/BP1 |
| S20 | 20 | | 37 | S37/BP2 |
| S21 | 21 | | 36 | S36/BP3 |
| S22 | 22 | | 35 | S35/S43 |
| S23 | 23 | | 34 | S34/S42 |
| S24 | 24 | | 33 | S33/S41 |
| S25 | 25 | | 32 | S32/S40 |
| S26 | 26 | | 31 | S31 |
| S27 | 27 | | 30 | S30 |
| S28 | 28 | | 29 | S29 |

aaa-008298

Top view. For mechanical details, see Figure 39.

**Figure 4. Pin configuration for TSSOP56 (PCA8546BTT)**

PCA8546

**Product data sheet**

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

Rev. 2 — 29 September 2021

**5 / 60**

## 6.2 Pin description

**Table 3. Pin description of PCA8546ATT and PCA8546BTT**

*Input or input/output pins must always be at a defined level ($V_{SS}$ or $V_{DD}$) unless otherwise specified.*

| Pin | Symbol | Type | Description |
|---|---|---|---|
| 1 to 11 | S9 to S19 | output | LCD segment |
| 20 to 31 | S20 to S31 | output | LCD segment |
| 43 | RESET | input | active LOW reset input |
| 44 | $V_{SS}$ | supply | ground supply voltage |
| 45 | $V_{DD}$ | supply | supply voltage |
| 46 | OSCCLK | input/output | external clock input/internal oscillator output |
| 47 | $V_{LCD}$[1] | supply | LCD supply voltage |
| 48 to 56 | S0 to S8 | output | LCD segment |

**Pin layout depending on backplane swap configuration**[2]

| | BPS = 0[3] | BPS = 1 | | |
|---|---|---|---|---|
| 12 | BP0 | S32 | output | LCD backplane/LCD segment |
| 13 | BP1 | S33 | | |
| 14 | BP2 | S34 | | |
| 15 | BP3 | S35 | | |
| 16 | S43 | S36 | | |
| 17 | S42 | S37 | | |
| 18 | S41 | S38 | | |
| 19 | S40 | S39 | | |
| 32 | S32 | S40 | | |
| 33 | S33 | S41 | | |
| 34 | S34 | S42 | | |
| 35 | S35 | S43 | | |
| 36 | S36 | BP3 | | |
| 37 | S37 | BP2 | | |
| 38 | S38 | BP1 | | |
| 39 | S39 | BP0 | | |

**Pin layout depending on product and bus type**

| | PCA8546ATT | PCA8546BTT | | |
|---|---|---|---|---|
| 40 | A0 | | input | I²C-bus target address selection |
| | | CE | input | SPI-bus chip enable - active LOW |
| 41 | SCL | | input | I²C-bus serial clock |
| | | SCL | input | SPI-bus serial clock |

**Table 3. Pin description of PCA8546ATT and PCA8546BTT**...*continued*

*Input or input/output pins must always be at a defined level ($V_{SS}$ or $V_{DD}$) unless otherwise specified.*

| Pin | Symbol | | Type | Description |
|---|---|---|---|---|
| 42 | SDA | | input/output | I²C-bus serial data |
| | | SDI | input | SPI-bus data input |

[1] $V_{LCD}$ must be equal to or greater than $V_{DD}$.
[2] Effect of backplane swapping is illustrated in Figure 5.
[3] Bit BPS is explained in Section 7.1.3.

# 7 Functional description

The PCA8546 is a versatile peripheral device designed to interface any microcontroller to a wide variety of LCDs. It can directly drive any multiplexed LCD containing four backplanes and up to 44 segments.

## 7.1 Commands of PCA8546

The PCA8546 is controlled by 8 commands, which are defined in Table 4. Any other combinations of operation code bits that are not mentioned in this document may lead to undesired operation modes of PCA8546.

**Table 4. Commands of PCA8546**

| Command name | Register selection RS[1:0][1] | | Bits | | | | | | | | Reference |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| initialize | | | | | | | | | | | Section 7.1.1 |
|     initialize-MSB | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | |
|     initialize-LSB | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | |
| OTP-refresh | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | Section 7.1.2 |
| mode-settings | 0 | 0 | 0 | 1 | 0 | 1 | BPS | INV | PD | E | Section 7.1.3 |
| oscillator-control | 0 | 0 | 0 | 0 | 0 | 1 | 1 | EFR | COE | OSC | Section 7.1.4 |
| set-bias-mode | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | B[1:0] | | Section 7.1.5 |
| frame-frequency | 0 | 0 | 0 | 0 | 1 | FD[4:0] | | | | | Section 7.1.6 |
| load-data-pointer | 0 | 0 | 1 | 0 | DP[5:0] | | | | | | Section 7.1.7 |
| write-RAM-data | 0 | 1 | D[7:0] | | | | | | | | Section 7.1.8 |

[1] Information about control byte and register selection see Section 8.1.

### 7.1.1 Command: initialize

This command generates a chip-wide reset. It consists of two bytes which have to be sent both to the device.

**Table 5. Initialize - initialize command bit description**

| Bit | Symbol | Value | Description |
|---|---|---|---|
| **Initialize-MSB** | | | |

PCA8546

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

**Product data sheet** **Rev. 2 — 29 September 2021**

**7 / 60**

**Table 5. Initialize - initialize command bit description**...*continued*

| Bit | Symbol | Value | Description |
|---|---|---|---|
| 7 to 0 | - | 0001 0110 | fixed value |
| **Initialize-LSB** | | | |
| 7 to 0 | - | 0000 0011 | fixed value |

### 7.1.2 Command: OTP-refresh

During production of the device, each IC is calibrated to achieve the specified accuracy of the frame frequency. This calibration is performed on EPROM cells called One Time Programmable (OTP) cells. The device reads these cells every time the OTP-refresh command is sent. The OTP-refresh command has to be sent after a reset has been made and before the display is enabled.

This command will be completed after a maximum of 30 ms and requires either the internal or external clock to run. If the internal oscillator is not used, then a clock must be supplied to the OSCCLK pin. If the OTP-refresh instruction is sent and no clock is present, then the request is stored until a clock is available.

**Remark:** It is recommended not to enter power-down mode during the OTP refresh cycle.

**Table 6. OTP-refresh - OTP-refresh command bit description**

| Bit | Symbol | Value | Description |
|---|---|---|---|
| 7 to 0 | - | 1111 0000 | fixed value |

### 7.1.3 Command: mode-settings

**Table 7. Mode-settings - mode settings command bit description**

| Bit | Symbol | Value | Description |
|---|---|---|---|
| 7 to 4 | - | 0101 | fixed value |
| 3 | BPS | | **backplane swapping** |
| | | 0[1] | backplane configuration 0 |
| | | 1 | backplane configuration 1 |
| 2 | INV | | **set inversion mode** |
| | | 0[1][2] | Driving scheme A: LCD line inversion mode |
| | | 1 | Driving scheme B: LCD frame inversion mode |
| 1 | PD | | **set power mode** |
| | | 1 | power-down mode; backplane and segment outputs are connected to $V_{SS}$ and the internal oscillator is switched off |
| | | 0[1] | power-up mode |
| 0 | E | | **display switch** |
| | | 0[1] | display disabled; backplane and segment outputs are connected to $V_{SS}$ |
| | | 1 | display enabled |

[1]     Default value.
[2]     See Section 7.1.3.2.

### 7.1.3.1  Backplane swapping

Backplane swapping can be configured with the BPS bit (see Table 7). It moves the location of the backplane and the associated segment outputs from one side of the PCA8546 to the other. Backplane swapping is sometimes desirable to aid with the routing of PCBs that do not use multiple layers.

The BPS bit has to be set to the required value before enabling the display. Failure to do so does not damage the PCA8546 or the display, however unexpected display content may appear.
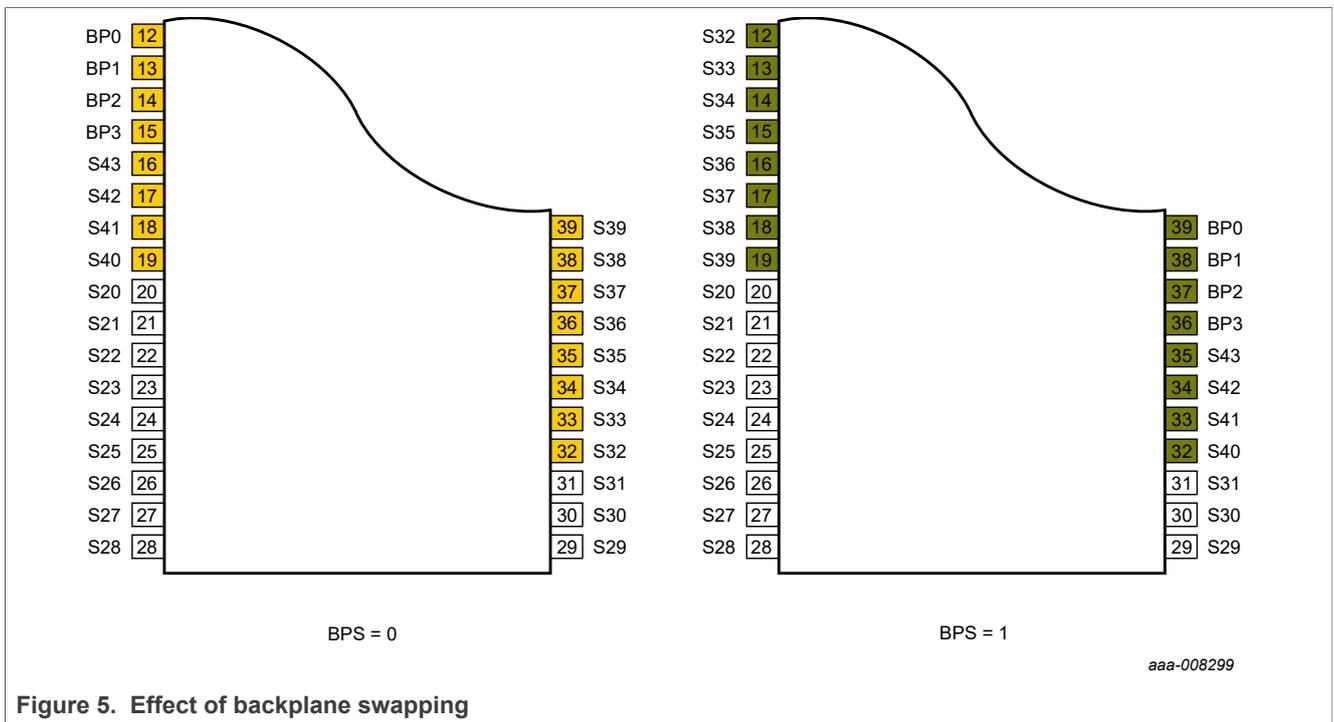


**Figure 5.  Effect of backplane swapping**

### 7.1.3.2  Line inversion (driving scheme A) and frame inversion (driving scheme B)

The DC offset of the voltage across the LCD is compensated over a certain period: line-wise in line inversion mode (driving scheme A) or frame-wise in frame inversion mode (driving scheme B). With the INV bit (see Table 7), the compensation mode can be switched.

In frame inversion mode, the DC value is compensated across two frames and not within one frame. Changing the inversion mode to frame inversion reduces the power consumption; therefore it is useful when power consumption is a key point in the application.

Frame inversion may not be suitable for all applications. The RMS voltage across a segment is better defined; however, since the switching frequency is reduced, there is possibility for flicker to occur.

The waveforms of Figure 14 shows the line inversion mode. Figure 15 shows the frame inversion mode.

#### 7.1.3.3 Power-down mode

The power-down bit (PD) allows the PCA8546 to be put in a minimum power configuration. To avoid display artifacts, enter power-down only after the display has been switched off by setting bit E to logic 0. During power-down, the internal oscillator is switched off.

**Table 8. Effect of the power-down bit (PD)**

| Effect on function | Mode settings | Effect of setting PD | |
|---|---|---|---|
| | | **0** | **1** |
| backplane output | E = 1 | normal function | $V_{SS}$ |
| segment output | E = 1 | normal function | $V_{SS}$ |
| internal oscillator | OSC = 0, COE = 1 | on | off |
| OSCCLK pin | OSC = 0, COE = 1 | output of internal oscillator frequency | $V_{DD}$ |
| OSCCLK pin | OSC = 1 | input clock | clock input, can be logic 0, logic 1, or left floating |

With the following sequence, the PCA8546 can be set to a state of minimum power consumption, called power-down mode.



*013aaa447*
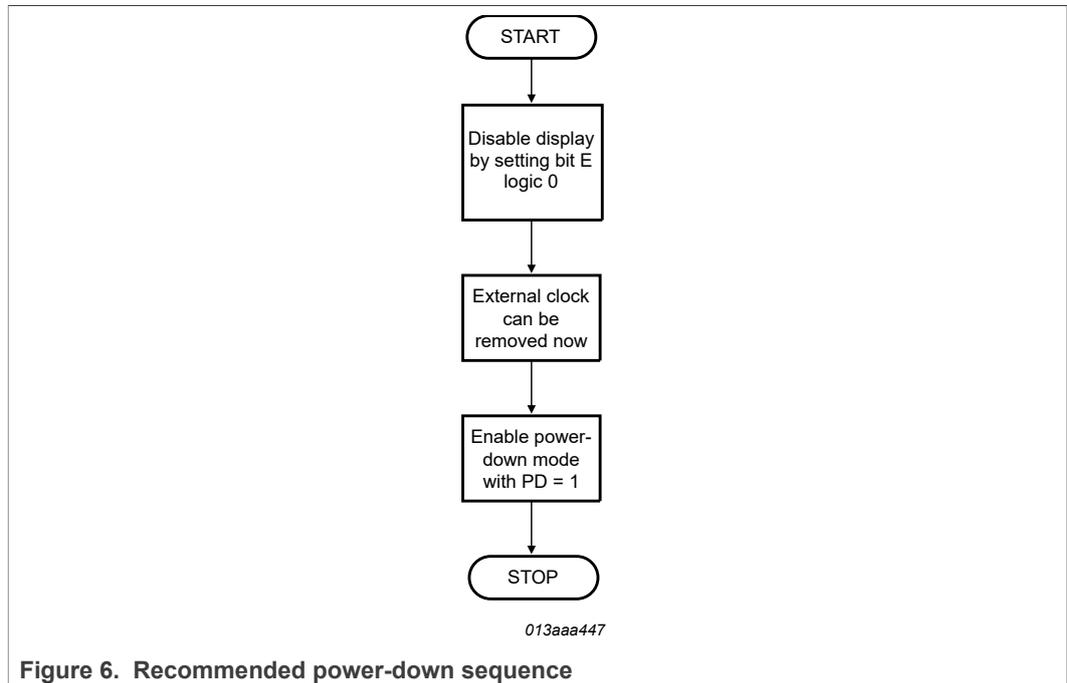
**Figure 6. Recommended power-down sequence**

**Remarks:**

- It is necessary to run the power-down sequence before removing the supplies. Depending on the application, care must be taken that no other signals are present at the chip input or output pins when removing the supplies (see Section 9). Otherwise it may cause unwanted display artifacts. If an uncontrolled removal of the supply happens, the PCA8546 does not get damaged.

- Static voltages across the liquid crystal display can build up when the external LCD supply voltage ($V_{LCD}$) is on while the IC supply voltage is off, or the other way around. This may cause unwanted display artifacts. To avoid such artifacts, $V_{LCD}$ and $V_{DD}$ must be applied or removed together.
- A clock signal must always be supplied to the device when the display is active. Removing the clock may freeze the LCD in a DC state, which is not suitable for the liquid crystal. First disable the display and afterwards remove the clock signal.

#### 7.1.3.4 Display enable

The display enable bit (E) is used to enable and disable the display. When the display is disabled, all LCD outputs go to $V_{SS}$. This function is implemented to ensure that no voltage can be induced on the LCD outputs as it may lead to unwanted displays of segments.

Recommended start-up sequences are found in Section 7.2.3

**Remark:** Display enable is not synchronized to an LCD frame boundary. Therefore using this function to flash a display for prolonged periods is not recommended due to the possible build-up of DC voltages on the display.

### 7.1.4 Command: oscillator-control

The oscillator-control command switches between internal and external oscillator and enables or disables the pin OSCCLK. It is also defines the external frequency.

**Table 9. Oscillator-control - oscillator control command bit description**

| Bit | Symbol | Value | Description |
|---|---|---|---|
| 7 to 3 | - | 0001 1 | fixed value |
| 2 | EFR | | **external clock frequency** applied on pin OSCCLK |
| | | 0[1] | 9.6 kHz |
| | | 1 | 230 kHz |
| 1 | COE | | **clock output enable for pin OSCCLK** |
| | | 0[1] | clock signal not available on pin OSCCLK; pin OSCCLK is in 3-state |
| | | 1 | clock signal available on pin OSCCLK |
| 0 | OSC | | **oscillator source** |
| | | 0[1] | internal oscillator running |
| | | 1 | external oscillator used; pin OSCCLK becomes an input; used in combination with EFR to determine input frequency |

[1] Default value.

The bits OSC, COE, and EFR control the source and frequency of the clock used to generate the LCD signals (see Figure 7). Valid combinations are shown in Table 10.

1. Can only be used with the internal oscillator (OSC = 0).
2. Can only be used with an external oscillator (OSC = 1).
3. Nominal value for divide factor q is 24; source clock is 230 kHz (see Section 7.1.6).

**Figure 7. Oscillator selection**
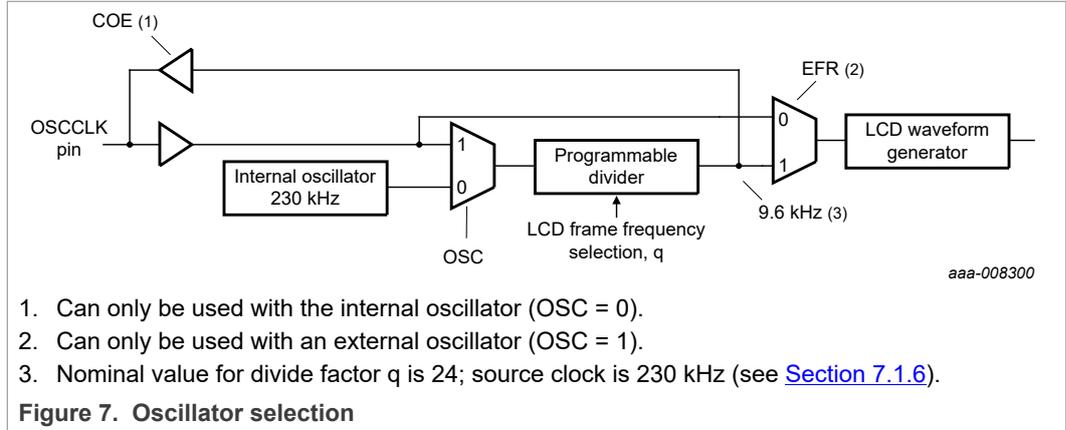
**Table 10. Valid combinations of bits OSC, EFR, and COE**

| OSC | COE | EFR | OSCCLK pin | Clock source |
|---|---|---|---|---|
| 0 | 0 | not used | inactive; may be left floating | internal oscillator used |
| 0 | 1 | not used | output of internal oscillator frequency (prescaler) | internal oscillator used |
| 1 | not used | 0 | 9.6 kHz input | OSCCLK pin |
| 1 | not used | 1 | 230 kHz input | OSCCLK pin |

**Table 11. Typical use of bits OSC, EFR, and COE**

| Usage | OSC | COE | EFR |
|---|---|---|---|
| LCD with internal oscillator | 0 | 0 | not used |
| LCD with external oscillator (230 kHz) | 1 | not used | 1 |
| LCD with external oscillator (9.6 kHz) | 1 | not used | 0 |

#### 7.1.4.1 Oscillator

The system is designed to operate from a 9.6 kHz or a 230 kHz clock. This clock can be sourced internally or externally. The internal logic and LCD drive signals of the PCA8546 are timed either by the internal oscillator or from the clock externally supplied.

Internal clock

When the internal oscillator is used, all LCD signals are generated from it. The oscillator runs at nominal 230 kHz. The relationship between this frequency and the LCD frame frequency is detailed in Section 7.1.6. Control over the internal oscillator is made with the OSC bit (see Section 7.1.4).

It is possible to make the internal oscillator signal available on pin OSCCLK by using the oscillator-control command (see Table 9) and configuring the clock output enable (COE) bit. If not required, the pin OSCCLK should be left open or connected to $V_{SS}$. At power-on the signal at pin OSCCLK is disabled and pin OSCCLK is in 3-state.

Clock output is only valid when using the internal oscillator. The signal appears on the OSCCLK pin.

An intermediate clock frequency is available at the OSCCLK pin. The duty cycle of this clock varies with the chosen divide ratio.

**Table 12. OSCCLK pin state depending on configuration**

| PD | OSC | COE | EFR | OSCCLK pin[1] |
|---|---|---|---|---|
| power-down | n.a. | off | n.a. | 3-state[2] |
| power-down | n.a. | on | n.a. | $V_{DD}$ |
| power-up | internal oscillator | off | n.a. | 3-state |
| | | on | n.a. | 9.6 kHz output[3] |
| | external oscillator | n.a. | 9.6 kHz | 9.6 kHz input |
| | | | 230 kHz | 230 kHz input |

[1] When $\overline{RESET}$ is active, the pin OSCCLK is in 3-state.
[2] In this state, an external clock may be applied, but it is not a requirement.
[3] 9.6 kHz is the nominal frequency with q = 24, see Table 13.

External clock

In applications where an external clock must be applied to the PCA8546, bit OSC (see Table 9) has to be set logic 1. In this case pin OSCCLK becomes an input.

The OSCCLK signal must switch between the $V_{SS}$ and the $V_{DD}$ voltage supplied to the chip.

The EFR bit determines the external clock frequency (230 kHz or 9.6 kHz). The clock frequency ($f_{clk(ext)}$) in turn determines the LCD frame frequency, see Table 13.

**Remark:** If an external clock is used, then this clock signal must always be supplied to the device when the display is on. Removing the clock may freeze the LCD in a DC state which damages the LCD material.

### 7.1.4.2 Timing and frame frequency

The timing of the PCA8546 organizes the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. The timing also generates the LCD frame frequency which it derives as an integer division of the clock frequency (see Table 13). The frame frequency is a fixed division of the internal clock or of the frequency applied to pin OSCCLK when an external clock is used.

**Table 13. LCD frame frequencies**

| Frame frequency | Typical external frequency (Hz) | Nominal frame frequency (Hz) | EFR bit | Value of q[1] |
|---|---|---|---|---|
| $f_{fr(LCD)} = \dfrac{f_{clk(ext)}}{48}$ | 9 600 | 200 | 0 | - |
| $f_{fr(LCD)} = \dfrac{f_{clk(ext)}}{48q}$ | 230 000 | 200 | 1 | 24 |

[1] Other values of the frame frequency prescaler see Table 16.

When the internal clock is used, or an external clock with EFR = 1, the LCD frame frequency can be programmed by software in steps of approximately 10 Hz in the range of 60 Hz to 300 Hz (see Table 16). Furthermore the internal oscillator is factory calibrated, see Table 31.

### 7.1.5  Command: set-bias-mode

The set-bias-mode command allows setting the bias level.

**Table 14.  Set-bias-mode - set bias mode command bit description**

| Bit | Symbol | Value | Description |
| --- | --- | --- | --- |
| 7 to 2 | - | 0000 01 | fixed value |
| 1 to 0 | B[1:0] | 00[1]. 01 | $\frac{1}{4}$ bias |
| | | 11 | $\frac{1}{3}$ bias |
| | | 10 | $\frac{1}{2}$ bias |

[1]  Default value.

### 7.1.6  Command: frame-frequency

With the frame-frequency command, the frame frequency for the display can be configured. The clock frequency determines the frame frequency.

**Table 15.  Frame-frequency - frame frequency and output clock frequency command bit description**

| Bit | Symbol | Value | Description |
| --- | --- | --- | --- |
| 7 to 5 | - | 001 | fixed value |
| 4 to 0 | FD[4:0] | see Table 16 | frequency prescaler |

When using an **external clock** it can be either a 230 kHz or a 9.6 kHz clock signal. The EFR bit (see Table 9) has to be set according to the external clock frequency.

When EFR is set to 9.6 kHz, then the LCD frame frequency is calculated with Equation 1:

$$f_{fr(LCD)} = \frac{f_{clk(ext)}}{48} \quad (1)$$

When EFR is set to 230 kHz, then the LCD frame frequency is calculated with Equation 2:

$$f_{fr(LCD)} = \frac{f_{clk(ext)}}{48q} \quad (2)$$

where q is the frequency divide factor (see Table 16).

**Remark:** $f_{clk(ext)}$ is the external input clock frequency to pin OSCCLK.

When the **internal oscillator** is used, the intermediate frequency may be output on the OSCCLK pin. Its frequency is given in Table 16.

**Table 16.  Frame frequency prescaler values for 230 kHz clock operation**

| FD[4:0] | Nominal LCD frame frequency (Hz)[1] | Divide factor, q | Intermediate clock frequency (Hz) |
| --- | --- | --- | --- |
| 0 0000 | 59.9 | 80 | 2 875 |

**Table 16. Frame frequency prescaler values for 230 kHz clock operation**...*continued*

| FD[4:0] | Nominal LCD frame frequency (Hz)[1] | Divide factor, q | Intermediate clock frequency (Hz) |
|---|---|---|---|
| 0 0001 | 70.5 | 68 | 3 382 |
| 0 0010 | 79.9 | 60 | 3 833 |
| 0 0011 | 90.4 | 53 | 4 340 |
| 0 0100 | 99.8 | 48 | 4 792 |
| 0 0101 | 108.9 | 44 | 5 227 |
| 0 0110 | 119.8 | 40 | 5 750 |
| 0 0111 | 129.5 | 37 | 6 216 |
| 0 1000 | 140.9 | 34 | 6 765 |
| 0 1001 | 149.7 | 32 | 7 188 |
| 0 1010 | 159.7 | 30 | 7 667 |
| 0 1011 | 171.1 | 28 | 8 214 |
| 0 1100 | 177.5 | 27 | 8 519 |
| 0 1101 | 191.7 | 25 | 9 200 |
| 0 1110[2] | 199.7 | 24 | 9 583 |
| 0 1111 | 208.3 | 23 | 10 000 |
| 1 0000 | 217.8 | 22 | 10 455 |
| 1 0001 | 228.3 | 21 | 10 952 |
| 1 0010 | 239.6 | 20 | 11 500 |
| 1 0011 | 252.2 | 19 | 12 105 |
| 1 0100 | 266.2 | 18 | 12 778 |
| 1 0101 | 281.9 | 17 | 13 529 |
| 1 0110 | 299.5 | 16 | 14 375 |
| 1 0111 to 1 1111 | not used | | |

[1] Nominal frame frequency calculated for the default clock frequency of 230 kHz.
[2] Default value.

### 7.1.7 Command: load-data-pointer

The load-data-pointer command defines the start address of the display RAM, see Table 17. The data pointer is auto incremented after each RAM write.

**Table 17. Load-data-pointer - load data pointer command bit description**

| Bit | Symbol | Value | Description |
|---|---|---|---|
| 7 to 6 | - | 10 | fixed value |
| 5 to 0 | DP[5:0] | 00 0000[1] to 10 1011 | 6-bit binary value of 0 to 43 |

[1] Default value.

**Remark:** Data pointer values outside of the valid range are ignored and no RAM content is transferred until a valid data pointer value is set.

Filling of the display RAM is described in Section 7.9.

### 7.1.8 Command: write-RAM-data

This command initiates the transfer of data to the display RAM. Data is written into the address defined by the load-data-pointer command. RAM filling is described in Section 7.9.

**Table 18. Write-RAM-data - write RAM data command bit description**
*For this command to be effective bit RS[1:0] of the control byte has to be set logic 01, see Table 22on page 29.*

| Bit | Symbol | Value | Description |
|---|---|---|---|
| 7 to 0 | D[7:0] | 0000 0000 to 1111 1111 | writing data byte-wise to RAM |

## 7.2 Start-up and shut-down

### 7.2.1 Reset and Power-On Reset (POR)

After power-on the PCA8546 has to be initialized by sending the two bytes of the initialize command (see Section 7.1.1 and Table 5).

After a reset and the initialization the starting conditions of the PCA8546 are as follows:

1. The display is disabled.
2. All backplane and segment outputs are set to $V_{SS}$.
3. The data pointers are cleared (set logic 0).
4. RAM data is not initialized. Its content can be considered to be random.
5. The internal oscillator is running; no clock signal is available on pin OSCCLK; pin OSCCLK is in 3-state.

The state after a reset and the initialization is shown in Table 19.

**Table 19. Starting conditions**

| Associated command | Bits | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| mode-settings | - | - | - | - | BPS = 0 | INV = 0 | PD = 0 | E = 0 |
| oscillator-control | - | - | - | - | - | EFR = 0 | COE = 0 | OSC = 0 |
| set-bias-mode | - | - | - | - | - | - | B[1:0] = 00 | |
| frame-frequency | - | - | - | FD[4:0] = 0 1110 | | | | |
| load-data-pointer | - | - | DP[5:0] = 00 0000 | | | | | |

After Power-On Reset (POR) and the initialize command and before enabling the display, the RAM content should be brought to a defined state by writing meaningful content (for example, a graphic) otherwise unwanted display artifacts may appear on the display.

### 7.2.2 RESET pin function

The $\overline{\text{RESET}}$ pin sets the PCA8546 in a defined mode. The RAM content remains unchanged. After the reset signal is removed, the initialize command (see Section 7.1.1 and Table 5) has to be sent to the PCA8546. See Section 7.2.1 for details.

### 7.2.3 Recommended start-up sequences

This chapter describes how to proceed with the initialization of the chip in different application modes.

In general, the sequence should always be:

1. Power-on or reset the device,
2. send the initialize command,
3. set the display and functional modes,
4. fill the display memory and then
5. turn on the display.



*aaa-008313*
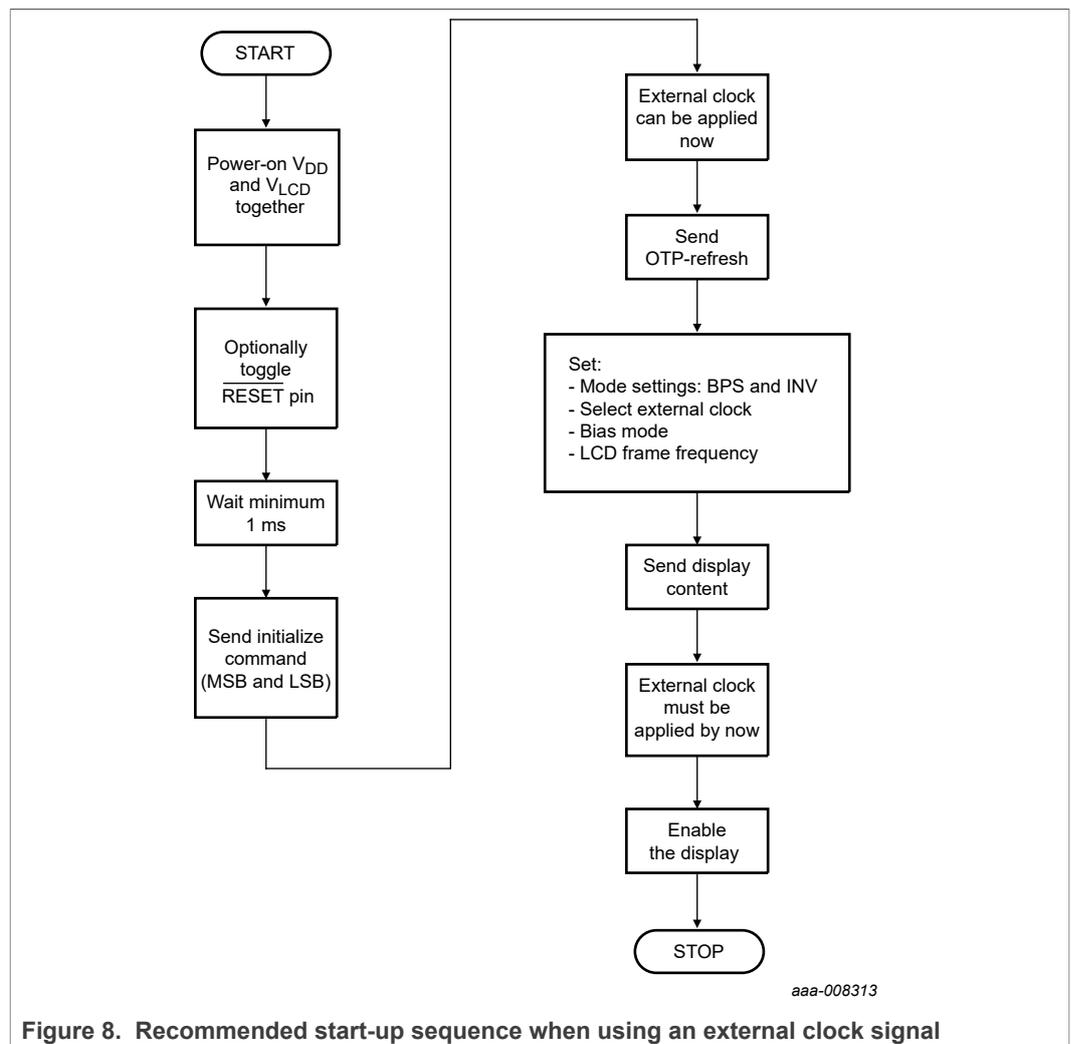
**Figure 8. Recommended start-up sequence when using an external clock signal**

PCA8546

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

**Product data sheet** **Rev. 2 — 29 September 2021**

**17 / 60**

**Figure 9. Recommended start-up sequence when using the internal oscillator**
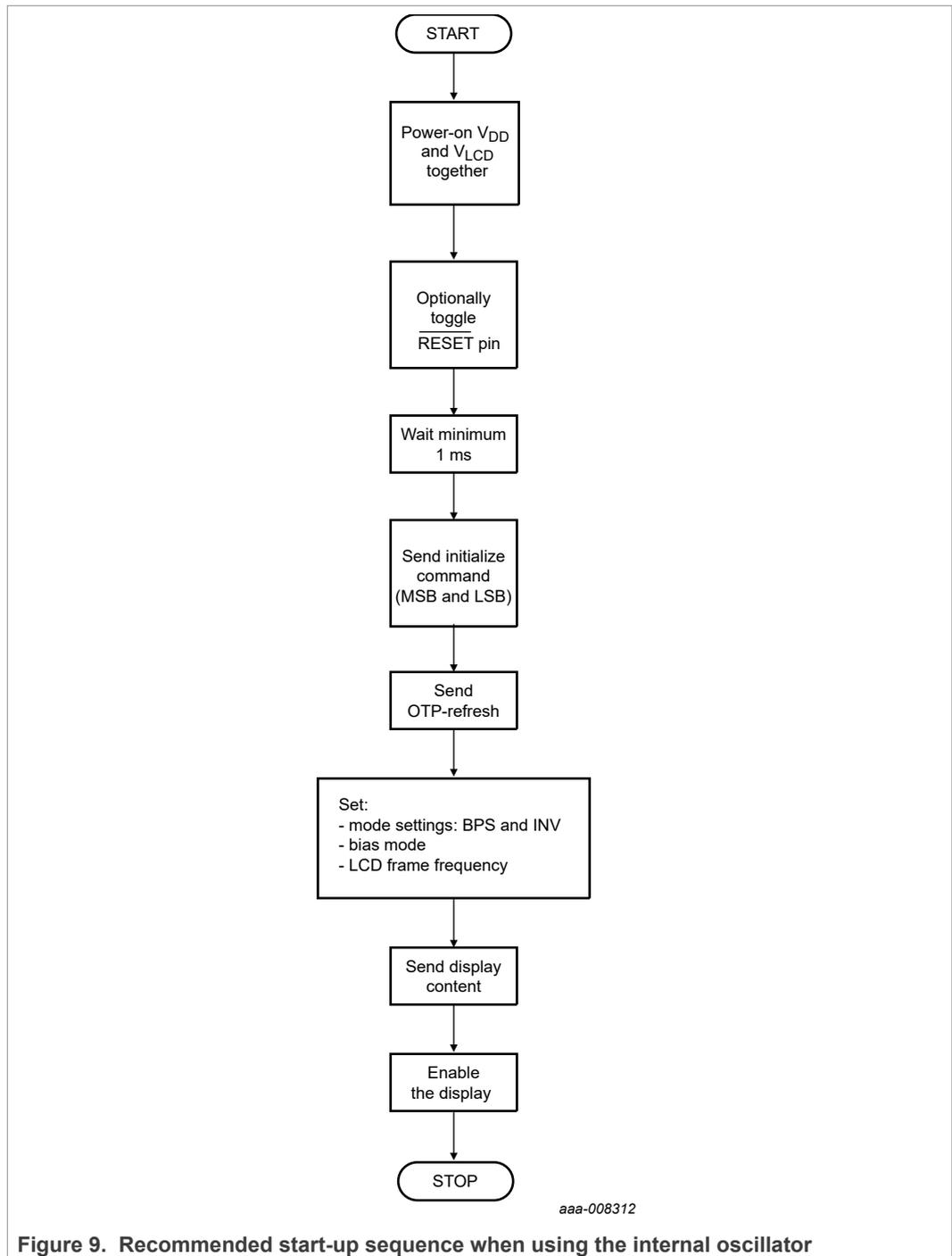
## 7.3 Possible display configurations

The PCA8546 is a versatile peripheral device designed to interface between any microcontroller to a wide variety of LCD segment or dot matrix displays (see Figure 10). It can drive multiplexed LCD with 4 backplanes and up to 44 segments.

PCA8546

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

**Product data sheet** **Rev. 2 — 29 September 2021**

**18 / 60**
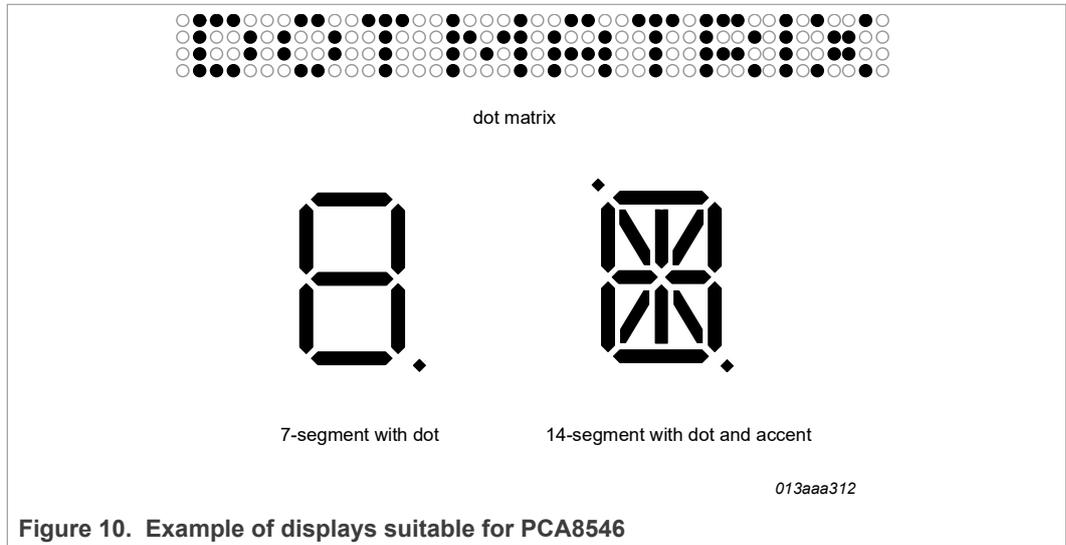
**Figure 10. Example of displays suitable for PCA8546**

**Table 20. Display configuration**

| Number of | | | Digits/Characters | | Dot matrix/ Elements |
|---|---|---|---|---|---|
| **Backplanes** | **Segments** | **Icons** | **7 segment**[1] | **14 segment**[2] | |
| 4 | 44 | 176 | 22 | 11 | 176 |

[1]    7 segment display has 8 elements including the decimal point.
[2]    14 segment display has 16 elements including decimal point and accent dot.

The display configuration in Table 20 can be implemented in the typical systems shown in Figure 11 and Figure 12.



**Figure 11. Typical system configuration for the I²C-bus**

**Product data sheet**                     **Rev. 2 — 29 September 2021**

**Figure 12. Typical system configuration for the SPI-bus**
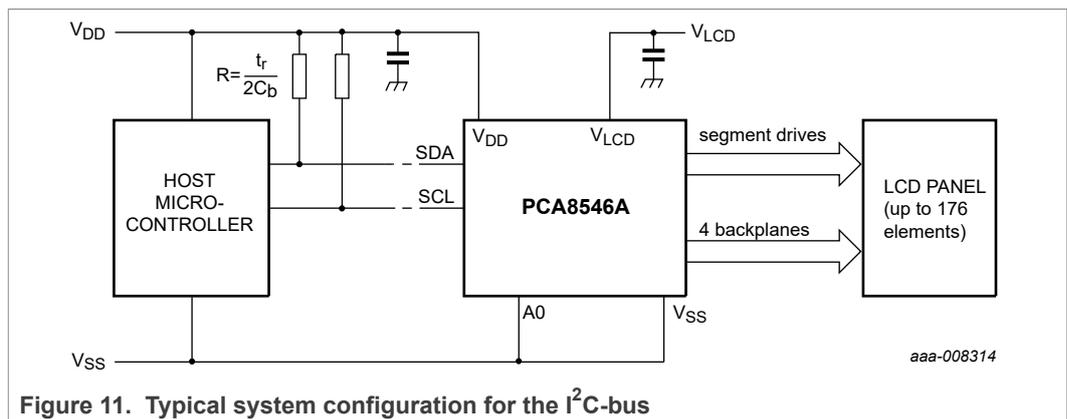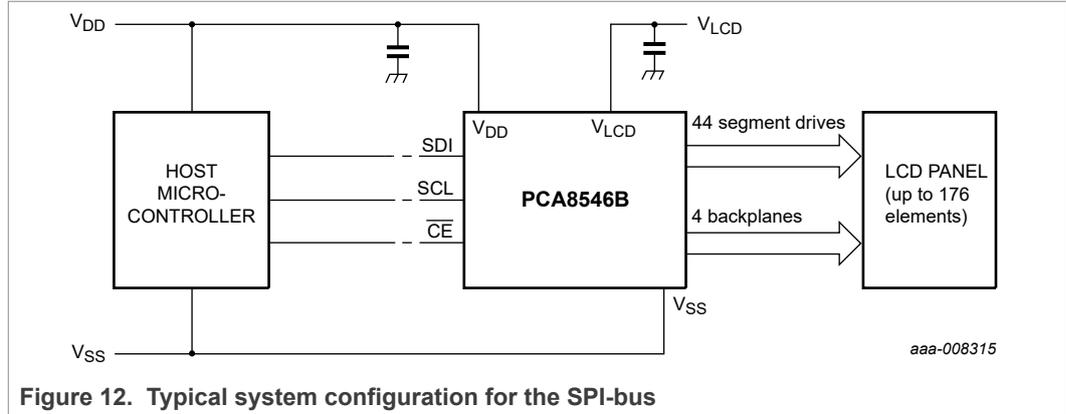
The host microcontroller maintains the two line I$^2$C-bus or a three line SPI-bus communication channel with the PCA8546. The appropriate biasing voltages for the multiplexed LCD waveforms are generated internally. The only other connections required to complete the system are the power supplies ($V_{DD}$, $V_{SS}$, $V_{LCD}$) and the LCD panel selected for the application.

The minimum recommended values for external capacitors on $V_{DD}$ and $V_{LCD}$ are 100 nF respectively. Decoupling of $V_{LCD}$ helps to reduce display artifacts. The decoupling capacitors should be placed close to the IC with short connections to the respective supply pin and $V_{SS}$.

## 7.4 LCD voltage selector

The LCD voltage selector coordinates the multiplexing of the LCD in accordance with the selected LCD drive configuration. The operation of the voltage selector is controlled by the set-bias-mode command (see Table 14).

Fractional LCD biasing voltages are obtained from an internal voltage divider. The biasing configurations, the biasing characteristics as functions of $V_{LCD}$ and the resulting discrimination ratios (D), are given in Table 21.

Discrimination is a term which is defined as the ratio of the on and off RMS voltage across a segment. It can be thought of as a measurement of contrast.

**Table 21. Preferred LCD drive modes: summary of characteristics**

| LCD multiplex drive mode | Number of: | | LCD bias configuration | $\dfrac{V_{off(RMS)}}{V_{LCD}}$ | $\dfrac{V_{on(RMS)}}{V_{LCD}}$ | $D = \dfrac{V_{on(RMS)}}{V_{off(RMS)}}$ [1] | $V_{LCD}$[2] |
|---|---|---|---|---|---|---|---|
| | **Backplanes** | **Levels** | | | | | |
| 1:4 [3] | 4 | 3 | $\frac{1}{2}$ | 0.433 | 0.661 | 1.527 | 2.309$V_{off(RMS)}$ |
| 1:4 | 4 | 4 | $\frac{1}{3}$ | 0.333 | 0.577 | 1.732 | 3.0$V_{off(RMS)}$ |
| 1:4 [3] | 4 | 5 | $\frac{1}{4}$ | 0.331 | 0.545 | 1.646 | 3.024$V_{off(RMS)}$ |

[1] Determined from Equation 5.
[2] Determined from Equation 4.
[3] In these examples, the discrimination factor and hence the contrast ratios are smaller. The advantage of these LCD drive modes is a reduction of the LCD voltage $V_{LCD}$.

A practical value for $V_{LCD}$ is determined by equating $V_{off(RMS)}$ with a defined LCD threshold voltage ($V_{th(off)}$), typically when the LCD exhibits approximately 10 % contrast.

Bias is calculated by $\frac{1}{1+a}$, where the values for a are

a = 1 for $\frac{1}{2}$ bias
a = 2 for $\frac{1}{3}$ bias
a = 3 for $\frac{1}{4}$ bias

The RMS on-state voltage ($V_{on(RMS)}$) for the LCD is calculated with Equation 3

$$V_{on(RMS)} = \frac{V_{LCD}}{\sqrt{n \times (1+a)^2}} \sqrt{a^2 + 2a + n} \quad (3)$$

where $V_{LCD}$ is the resultant voltage at the LCD segment and where the value for n is

n = 4 for 1:4 multiplex drive

The RMS off-state voltage ($V_{off(RMS)}$) for the LCD is calculated with Equation 4:

$$V_{off(RMS)} = \frac{V_{LCD}}{\sqrt{n \times (1+a)^2}} \sqrt{a^2 - 2a + n} \quad (4)$$

Discrimination is the ratio of $V_{on(RMS)}$ to $V_{off(RMS)}$ and is determined from Equation 5:

$$D = \frac{V_{on(RMS)}}{V_{off(RMS)}} = \sqrt{\frac{a^2 + 2a + n}{a^2 - 2a + n}} \quad (5)$$

$V_{LCD}$ is sometimes referred to as the LCD operating voltage.

### 7.4.1 Electro-optical performance

Suitable values for $V_{on(RMS)}$ and $V_{off(RMS)}$ are dependent on the LCD liquid used. The RMS voltage, at which a pixel gets switched on or off, determine the transmissibility of the pixel.

For any given liquid, there are two threshold values defined. One point is at 10 % relative transmission (at $V_{th(off)}$) and the other at 90 % relative transmission (at $V_{th(on)}$), see Figure 13. For a good contrast performance, the following rules should be followed:

$$V_{on(RMS)} \geq V_{th(on)} \quad (6)$$

$$V_{off(RMS)} \leq V_{th(off)} \quad (7)$$

$V_{on(RMS)}$ and $V_{off(RMS)}$ are properties of the display driver and are affected by the selection of a, n (see Equation 3 to Equation 5) and the $V_{LCD}$ voltage.

$V_{th(off)}$ and $V_{th(on)}$ are properties of the LCD liquid and can be provided by the module manufacturer. $V_{th(off)}$ is sometimes named $V_{th}$. $V_{th(on)}$ is sometimes named saturation voltage $V_{sat}$.

It is important to match the module properties to those of the driver in order to achieve optimum performance.

013aaa494

**Figure 13. Electro-optical characteristic: relative transmission curve of the liquid**
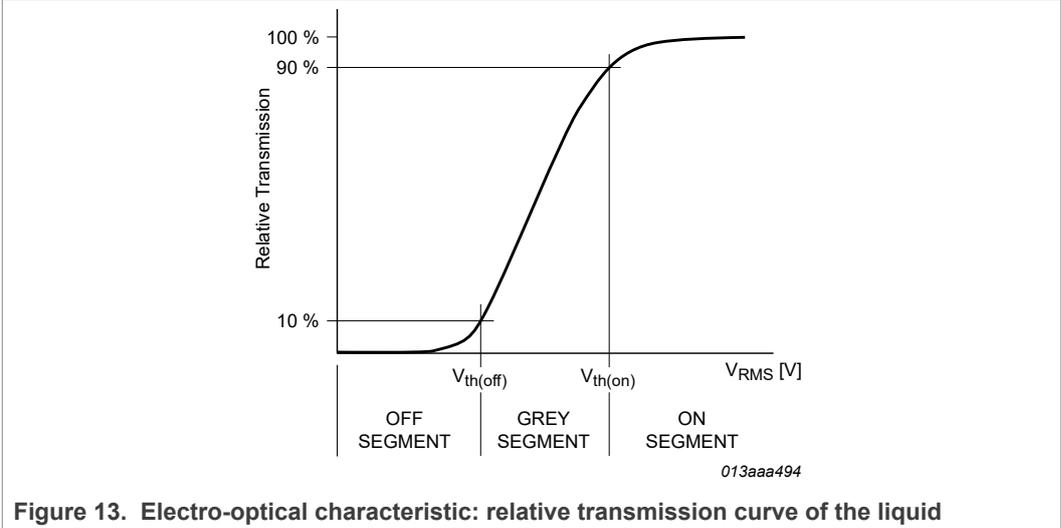
## 7.5 LCD drive mode waveforms

### 7.5.1 $\frac{1}{3}$ bias and line inversion



$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$. $V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.
$V_{on(RMS)}(t) = 0.577V_{LCD}$. $V_{off(RMS)}(t) = 0.333V_{LCD}$.

**Figure 14. Waveforms for the 1:4 multiplex drive mode with $\frac{1}{3}$ bias and line inversion**

PCA8546

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

**Product data sheet**

**Rev. 2 — 29 September 2021**

**23 / 60**

### 7.5.2 $\frac{1}{3}$ bias and frame inversion



(a) Waveforms at driver

(b) Resultant waveforms at LCD segment

aaa-008201

$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$. $V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

$V_{on(RMS)}(t) = 0.577 V_{LCD}$. $V_{off(RMS)}(t) = 0.333 V_{LCD}$.

**Figure 15. Waveforms for 1:4 multiplex drive mode with $\frac{1}{3}$ bias and frame inversion**

## 7.6 Display register

The display register holds the display data while the corresponding multiplex signals are generated.

## 7.7 Backplane outputs

The LCD drive section includes four backplane outputs: BP0 to BP3 which must be connected directly to the LCD.

### 7.8 Segment outputs

The LCD drive section includes up to 44 segment outputs (S0 to S43) which must be connected directly to the LCD. The segment output signals are generated based on the data resident in the display register. When less segment outputs are required, the unused segment outputs must be left open-circuit.

### 7.9 Display RAM

The display RAM stores the LCD data. The RAM size is 44 × 4 bit.



The display RAM bitmap shows the direct relationship between the display RAM column and the segment outputs and between the bits in a RAM row and the backplane outputs.

**Figure 16. Display RAM bitmap**
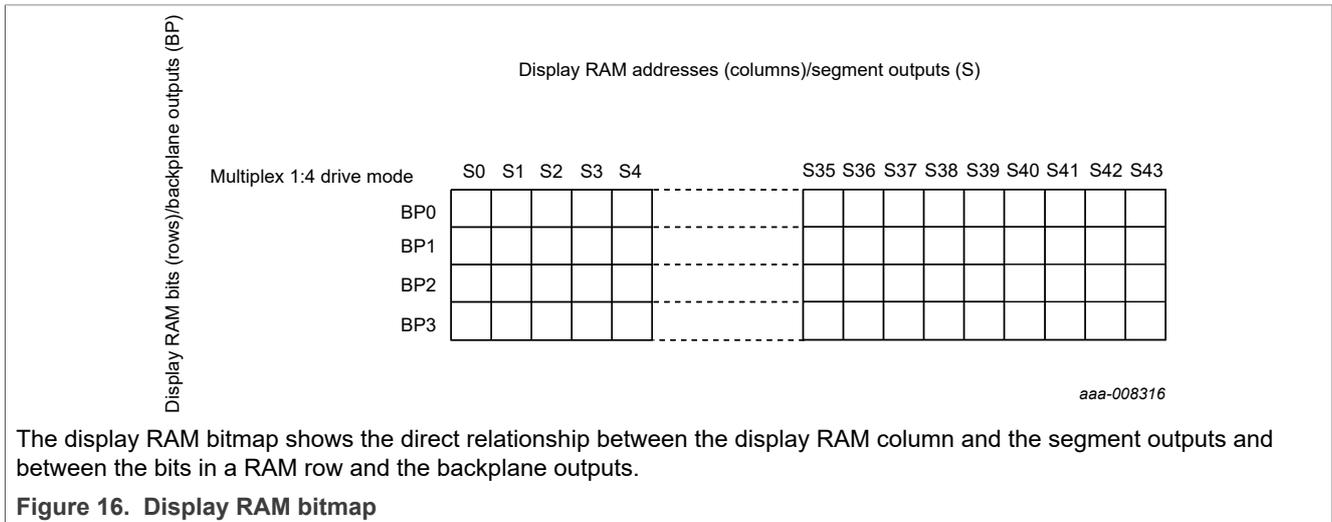
Logic 1 in the RAM bit map indicates the on-state ($V_{on(RMS)}$) of the corresponding LCD element; similarly, logic 0 indicates the off-state ($V_{off(RMS)}$). For more information on $V_{on(RMS)}$ and $V_{off(RMS)}$, see Section 7.4.

There is a one-to-one correspondence between

• the bits in the RAM bitmap and the LCD elements,
• the RAM columns and the segment outputs,
• the RAM rows and the backplane outputs.

The display RAM bit map, Figure 16, shows row 0 to row 3 and column 0 to column 43. Row 0 to row 3 correspond with the backplane outputs BP0 to BP3. Column 0 to column 43 correspond with the segment outputs S0 to S43. In multiplexed LCD applications, the data of each row of the display RAM is time-multiplexed with the corresponding backplane (row 0 with BP0, row 1 with BP1, and so on).

#### 7.9.1 Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the data pointer by the load-data-pointer command (see Table 17).

Following this command, an arriving data byte is stored starting at the display RAM address indicated by the data pointer.

The data pointer is automatically incremented. That is, after each byte is stored, the contents of the data pointer are incremented by two.

When the address counter reaches the end of the RAM, it stops incrementing after the last byte is transmitted. Redundant bits of the last byte and subsequent bytes transmitted are discarded until the pointer is reset. To send new RAM data, the data pointer must be reset.

If an I$^2$C-bus or SPI-bus data access is terminated early, then the state of the data pointer is unknown. The data pointer must then be rewritten before further RAM accesses.

### 7.9.2 RAM filling

The RAM is organized in four rows and 44 columns. The eight transmitted data bits are placed in two successive display RAM columns of four rows (see Figure 17). In order to fill the whole four RAM rows, 22 bytes need to be sent to the PCA8546. After the last byte sent, the data pointer must be reset before the next RAM content update. Additional data bytes sent and any data bits that spill over the RAM are discarded.
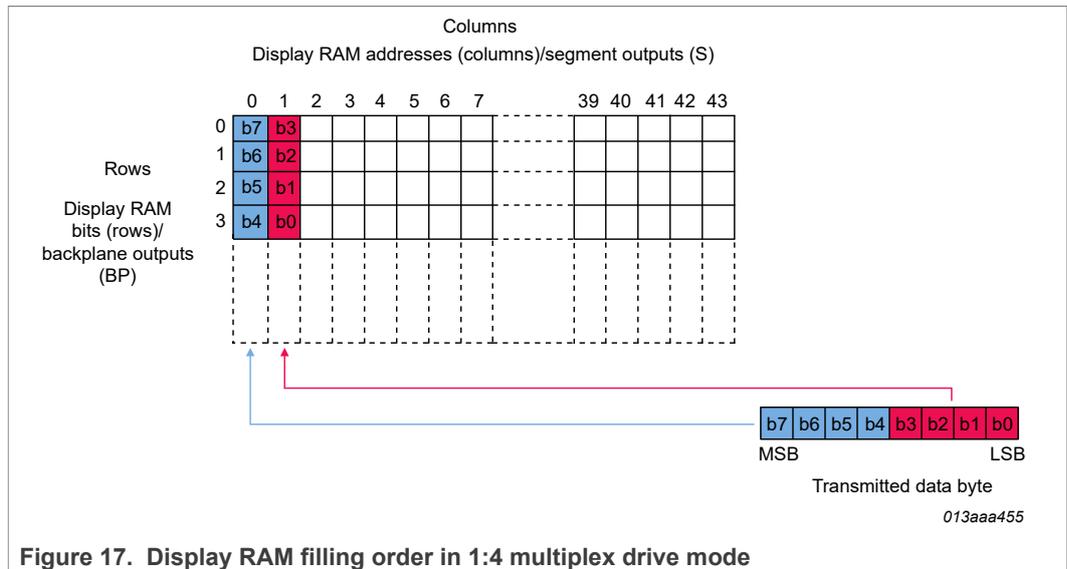


**Figure 17. Display RAM filling order in 1:4 multiplex drive mode**

Depending on the start address of the data pointer, there is the possibility for a boundary condition. This occurs when more data bits are sent than fit into the remaining RAM. The additional data bits are discarded. See Figure 18.

**Product data sheet**
Rev. 2 — 29 September 2021

**Figure 18.  Boundary condition in 1:4 multiplex drive mode**
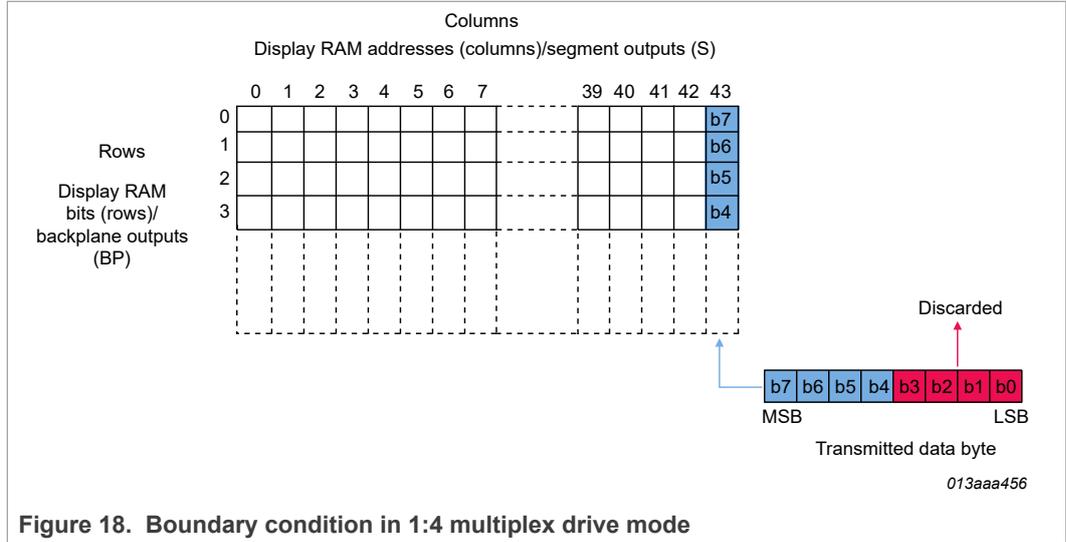
# 8    Bus interfaces

## 8.1  Control byte and register selection

After initiating the communication over the bus and sending the target address ($I^2$C-bus, see Section 8.2) or subaddress (SPI-bus, see Section 8.3), a control byte follows. The purpose of this byte is to indicate both, the content for the following data bytes (RAM, or command) and to indicate that more control bytes will follow.

Typical sequences could be:

• target address/subaddress - control byte - command byte - command byte - command byte - end
• target address/subaddress - control byte - RAM byte - RAM byte - RAM byte - end
• target address/subaddress - control byte - command byte - control byte - RAM byte - end

In this way, it is possible to send a mixture of RAM and command data in one access or alternatively, to send just one type of data in one access.

**Table 22.  Control byte description**

| Bit | Symbol | Value | Description |
|---|---|---|---|
| 7 | CO | | **continue bit** |
| | | 0 | last control byte |
| | | 1 | control bytes continue |
| 6 to 5 | RS[1:0] | | **register selection** |
| | | 00 | command register |
| | | 01 | RAM data |
| | | 10, 11 | unused |
| 4 to 0 | - | - | unused |
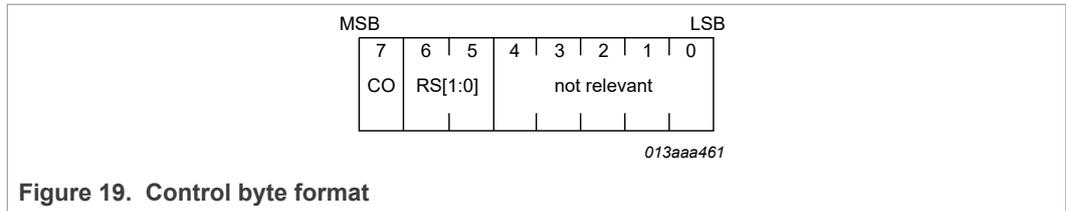
**Figure 19. Control byte format**

## 8.2 I$^2$C-bus interface

The I$^2$C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a Serial DAta line (SDA) and a Serial CLock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

### 8.2.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time is interpreted as a control signal (see Figure 20).
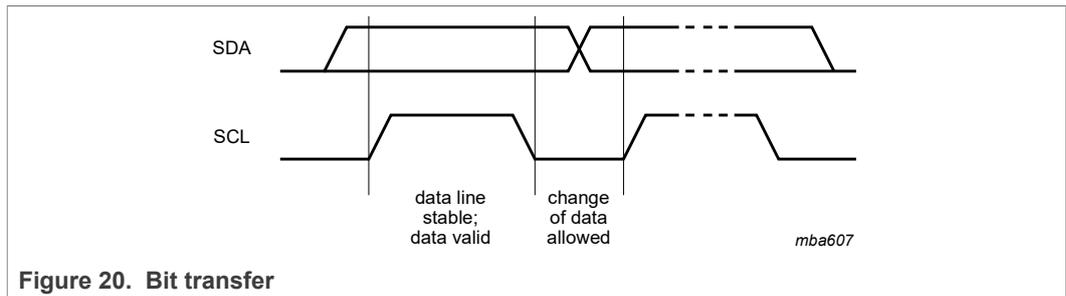


**Figure 20. Bit transfer**

### 8.2.2 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy.

A HIGH-to-LOW change of the data line, while the clock is HIGH, is defined as the START condition (S).

A LOW-to-HIGH change of the data line, while the clock is HIGH, is defined as the STOP condition (P).

The START and STOP conditions are shown in Figure 21.
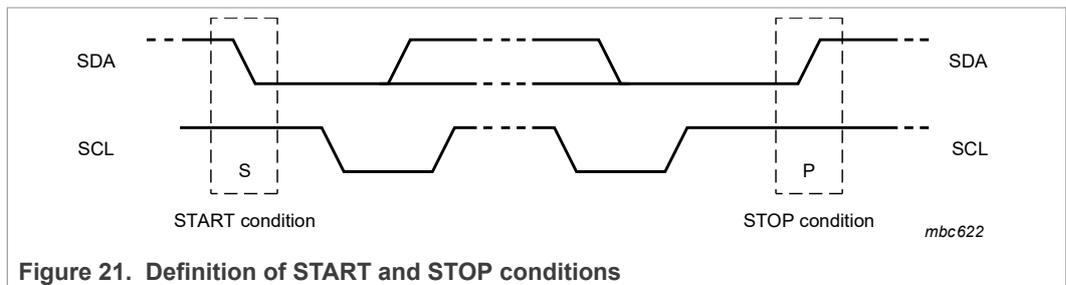


**Figure 21. Definition of START and STOP conditions**

### 8.2.3 System configuration

A device generating a message is a transmitter, a device receiving a message is the receiver. The device that controls the message is the controller and the devices which are controlled by the controller are the targets. The system configuration is shown in Figure 22.
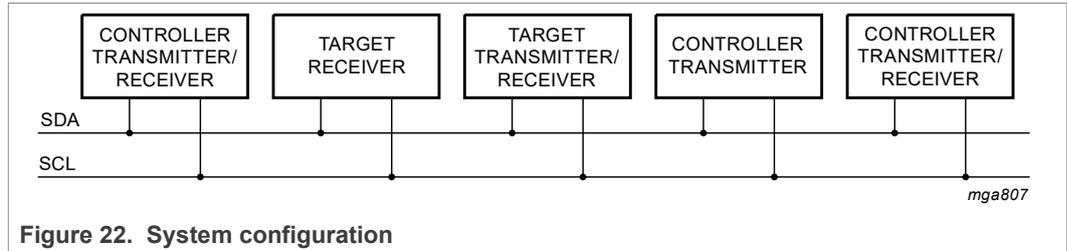


**Figure 22. System configuration**

### 8.2.4 Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of 8 bits is followed by an acknowledge cycle.

- A target receiver which is addressed must generate an acknowledge after the reception of each byte.
- Also a controller receiver must generate an acknowledge after the reception of each byte that has been clocked out of the target transmitter.
- The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be considered).
- A controller receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the target. In this event, the transmitter must leave the data line HIGH to enable the controller to generate a STOP condition.

Acknowledgement on the I$^2$C-bus is shown in Figure 23.
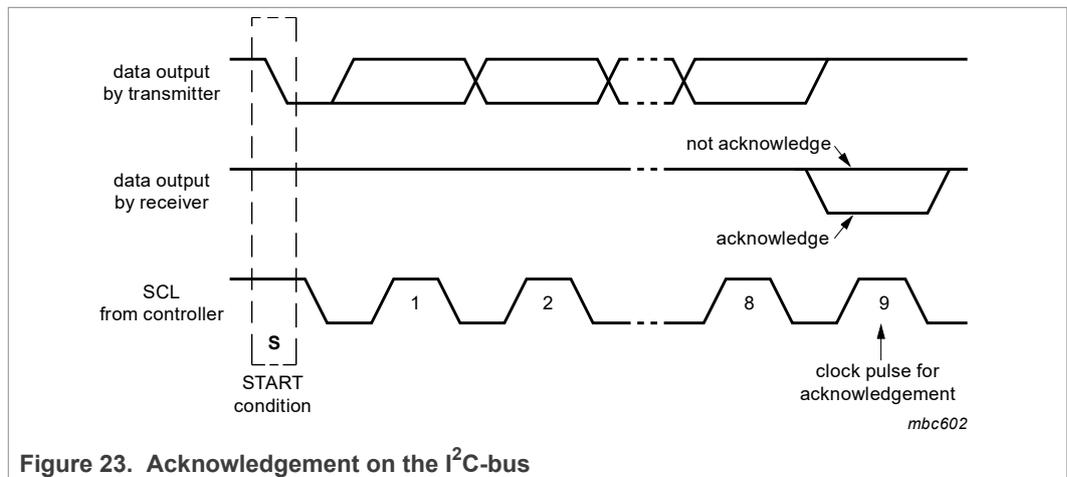


**Figure 23. Acknowledgement on the I$^2$C-bus**

### 8.2.5 I$^2$C-bus controller

The PCA8546 acts as an I$^2$C-bus target receiver. It does not initiate I$^2$C-bus transfers or transmit data to an I$^2$C-bus controlller receiver. Device selection depends on the I$^2$C-bus target address.

### 8.2.6 Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

### 8.2.7 I$^2$C-bus target address

Device selection depends on the I$^2$C-bus target address. Two different I$^2$C-bus target addresses can be used to address the PCA8546 (see Table 23).

**Table 23. I$^2$C target address byte**

| | target address | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Bit** | **7** | **6** | **5** | **4** | **3** | **2** | **1** | **0** |
| | **MSB** | | | | | | | **LSB** |
| | 0 | 1 | 1 | 1 | 0 | 0 | A0 | R/$\overline{\text{W}}$ |

The least significant bit of the target address byte is bit R/$\overline{\text{W}}$ (see Table 24).

**Table 24. R/$\overline{\text{W}}$-bit description**

| R/$\overline{\text{W}}$ | Description |
|---|---|
| 0 | write data |
| 1 | read data |

Bit 1 of the target address is defined by connecting the input A0 to either $V_{SS}$ (logic 0) or $V_{DD}$ (logic 1). Therefore, two instances of PCA8546 can be distinguished on the same I$^2$C-bus.

### 8.2.8 I$^2$C-bus protocol

The I$^2$C-bus protocol is shown in Figure 24. The sequence is initiated with a START condition (S) from the I$^2$C-bus controller which is followed by one of the two PCA8546 target addresses available. All PCA8546 with the corresponding A0 level acknowledge in parallel to the target address. But any PCA8546 with the alternative A0 level ignore the whole I$^2$C-bus transfer.

After acknowledgement, a control byte follows (see Section 8.1).

The display bytes are stored in the display RAM at the address specified by the RAM data pointer.

The acknowledgement after each byte is made only by the addressed PCA8546. After the last data byte, the I$^2$C-bus controller issues a STOP condition (P). Alternatively a START may be issued to RESTART an I$^2$C-bus access.

**Figure 24. I$^2$C-bus protocol write mode**

#### 8.2.8.1 Status read out

Status read out for I$^2$C-bus operation only. This command initiates the read-out of a fixed value plus the target address bit A0 from the PCA8546. The read-out function allows the I$^2$C controller to confirm the existence of the device on the I$^2$C-bus.

**Table 25. Status read out value**

| Bit | Symbol | Value | Description |
|---|---|---|---|
| 7 to 1 | - | 0101 010 | fixed value |
| 0 | A0 | 0 | read back value is 0101 0100 |
| | | 1 | read back value is 0101 0101 |

If a readout is made, the R/$\overline{W}$ bit must be logic 1 and then the next data byte following is provided by the PCA8546 as shown in Figure 25.



1. From PCA8546.

**Figure 25. I$^2$C-bus protocol read mode**

In the unlikely case that the chip has entered the internal test mode, detection of this state is possible by using the modified status read-out detailed in Table 26. The read out value is modified to indicate that the chip has entered an internal test mode.

**Table 26. Modified status read out value**

| Bit | Symbol | Value | Description |
|---|---|---|---|
| 7 to 1 | - | 1111 000 | fixed value |
| 0 | A0 | 0 | read back value is 1111 0000 |
| | | 1 | read back value is 1111 0001 |

EMC detection

The PCA8546 is ruggedized against EMC susceptibility; however it is not possible to cover all cases. To detect if a severe EMC event has occurred, it is possible to check the responsiveness of the device by reading its register.

## 8.3 SPI-bus interface

Data transfer to the device is made via a 3 line SPI-bus (see Table 27). There is no output data line. The SPI-bus is initialized whenever the chip enable line pin $\overline{CE}$ is inactive.

**Table 27. Serial interface**

| Symbol | Function | Description |
|---|---|---|
| $\overline{CE}$ | chip enable input[1]; active LOW | when HIGH, the interface is reset |
| SCL | serial clock input | input may be higher than $V_{DD}$ |
| SDI | serial data input | input may be higher than $V_{DD}$; input data is sampled on the rising edge of SCL |

[1] The chip enable must not be wired permanently LOW.

### 8.3.1 Data transmission

The chip enable signal is used to identify the transmitted data. Each data transfer is a byte with the Most Significant Bit (MSB) sent first.

The transmission is controlled by the active LOW chip enable signal $\overline{CE}$. The first byte transmitted is the subaddress byte.
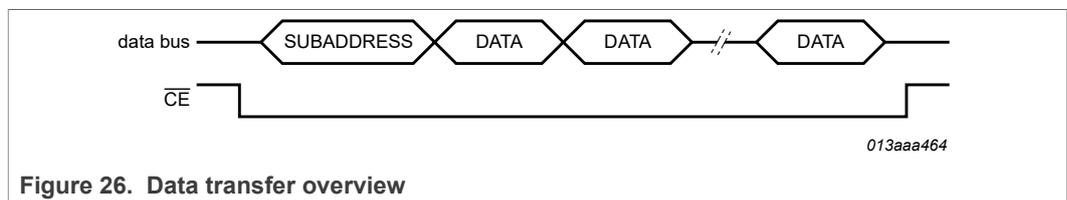


**Figure 26. Data transfer overview**

The subaddress byte opens the communication with a read/write bit and a subaddress. The subaddress is used to identify multiple devices on one SPI-bus.

**Table 28. Subaddress byte definition**

| Bit | Symbol | Value | Description |
|---|---|---|---|
| 7 | R/$\overline{W}$ | | **data read or write selection** |
| | | 0 | write data |
| | | 1 | read data |

**Table 28. Subaddress byte definition**...*continued*

| Bit | Symbol | Value | Description |
|-----|--------|-------|-------------|
| 6 to 5 | SA[1:0] | 01 | **subaddress**; other codes cause the device to ignore data transfer |
| 4 to 0 | - | | unused |

After the subaddress byte, a control byte follows (see Section 8.1).



Data transfers are terminated by de-asserting $\overline{CE}$ (set $\overline{CE}$ to logic 1).

**Figure 27. SPI-bus write example**



In this example, the bias system is set to $\frac{1}{3}$. The transfer is terminated by $\overline{CE}$ returning to logic 1. After the last bit is transmitted, the state of the SDI line is not important.

**Figure 28. SPI-bus example**

PCA8546

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

**Product data sheet** **Rev. 2 — 29 September 2021**

33 / 60

## 9   Internal circuitry



**Figure 29. Device protection diagram for PCA8546A**
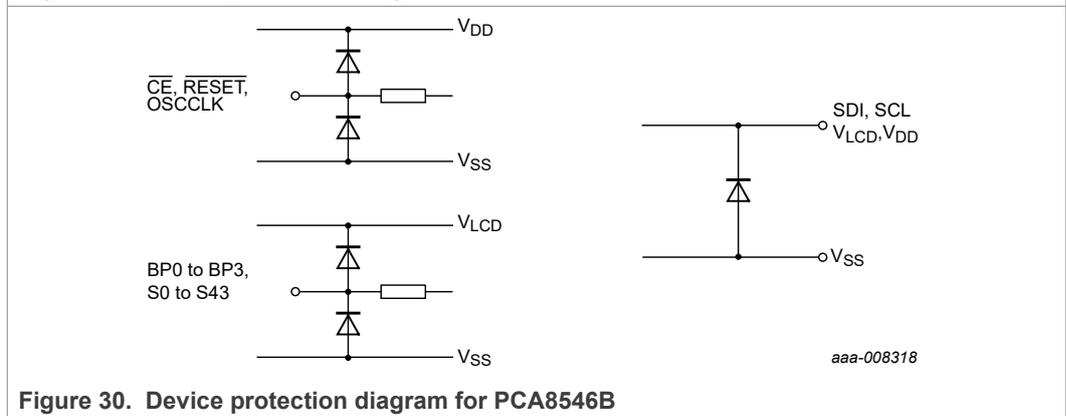


**Figure 30. Device protection diagram for PCA8546B**

## 10  Safety notes

| CAUTION |
|---|
| This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices. Such precautions are described in the *ANSI/ESD S20.20, IEC/ST 61340-5, JESD625-A* or equivalent standards. |

| CAUTION |
|---|
| Static voltages across the liquid crystal display can build up when the LCD supply voltage ($V_{LCD}$) is on while the IC supply voltage ($V_{DD}$) is off, or vice versa. This may cause unwanted display artifacts. To avoid such artifacts, $V_{LCD}$ and $V_{DD}$ must be applied or removed together. |

## 11 Limiting values

**Table 29. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | supply voltage | | | -0.5 | +6.5 | V |
| $I_{DD}$ | supply current | | | -50 | +50 | mA |
| $V_{LCD}$ | LCD supply voltage | | | -0.5 | +10 | V |
| $I_{DD(LCD)}$ | LCD supply current | | | -50 | +50 | mA |
| $V_I$ | input voltage | PCA8546ATT | | | | |
| | | on pins SDA, OSCCLK, SCL, A0, $\overline{RESET}$ | | -0.5 | +6.5 | V |
| | | PCA8546BTT | | | | |
| | | on pins $\overline{CE}$, OSCCLK, SCL, SDI, $\overline{RESET}$ | | -0.5 | +6.5 | V |
| $I_I$ | input current | | | -10 | +10 | mA |
| $V_O$ | output voltage | on pins S0 to S43, BP0 to BP3 | | -0.5 | +10 | V |
| | | on pin SDA | | -0.5 | +6.5 | V |
| $I_O$ | output current | | | -10 | +10 | mA |
| $I_{SS}$ | ground supply current | | | -50 | +50 | mA |
| $P_{tot}$ | total power dissipation | | | - | 400 | mW |
| P/out | power dissipation per output | | | - | 100 | mW |
| $V_{ESD}$ | electrostatic discharge voltage | HBM | [1] | - | ±3 500 | V |
| | | CDM | [2] | - | ±1 250 | V |
| $I_{lu}$ | latch-up current | | [3] | - | 200 | mA |
| $T_{stg}$ | storage temperature | | [4] | -65 | +150 | °C |
| $T_{amb}$ | ambient temperature | operating device | | -40 | +95 | °C |

[1] Pass level; Human Body Model (HBM), according to [1].
[2] Pass level; Charge Device Model (CDM), according to [2].
[3] Pass level; latch-up testing according to [3] at maximum ambient temperature ($T_{amb(max)}$).
[4] According to the store and transport requirements (see [4]) the devices have to be stored at a temperature of +8 °C to +45 °C and a humidity of 25 % to 75 %.

## 12 Static characteristics

**Table 30. Static characteristics**

*$V_{DD}$ = 1.8 V to 5.5 V; $V_{SS}$ = 0 V; $V_{LCD}$ = 2.5 V to 9 V; $T_{amb}$ = -40 °C to +95 °C; unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Supplies** | | | | | | |
| $V_{DD}$ | supply voltage | | 1.8 | - | 5.5 | V |

**Table 30. Static characteristics**...*continued*

$V_{DD}$ = 1.8 V to 5.5 V; $V_{SS}$ = 0 V; $V_{LCD}$ = 2.5 V to 9 V; $T_{amb}$ = -40 °C to +95 °C; unless otherwise specified.

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{LCD}$ | LCD supply voltage | $V_{LCD} \geq V_{DD}$ | | 2.5 | - | 9 | V |
| $I_{DD(pd)}$ | power-down mode supply current | | [1] | - | 0.5 | 2 | µA |
| $I_{DD}$ | supply current | see Figure 31 | | | | | |
| | | external 9.6 kHz clock | [2] | - | 10 | 25 | µA |
| | | internal oscillator | [2] | - | 30 | 60 | µA |
| $I_{DD(LCD)}$ | LCD supply current | power-down, see Figure 32 | [1][3] | - | 7 | 15 | µA |
| | | display active, see Figure 33 | [4] | - | 55 | 140 | µA |
| **Logic** | | | | | | | |
| $V_I$ | input voltage | | | $V_{SS}$ - 0.5 | - | $V_{DD}$ + 0.5 | V |
| $V_{IL}$ | LOW-level input voltage | on pins OSCCLK, A0 and $\overline{RESET}$ | | - | - | $0.3V_{DD}$ | V |
| $V_{IH}$ | HIGH-level input voltage | on pins OSCCLK, A0 and $\overline{RESET}$ | | $0.7V_{DD}$ | - | - | V |
| $V_O$ | output voltage | | | -0.5 | - | $V_{DD}$ + 0.5 | V |
| $V_{OH}$ | HIGH-level output voltage | driving load of 50 µA on pins OSCCLK | | $0.8V_{DD}$ | - | - | V |
| $V_{OL}$ | LOW-level output voltage | driving load of 50 µA on pins OSCCLK | | - | - | $0.2V_{DD}$ | V |
| $I_{OH}$ | HIGH-level output current | output source current; $V_{OH} = V_{DD}$ - 0.4 V | | | | | |
| | | on pin OSCCLK | | | | | |
| | | $V_{DD}$ = 1.8 V | | 0.7 | 1.6 | - | mA |
| | | $V_{DD} \geq 3.3$ V | | 1.5 | 4.0 | - | mA |
| $I_{OL}$ | LOW-level output current | output sink current; $V_{OL}$ = 0.4 V | | | | | |
| | | on pin OSCCLK | | | | | |
| | | $V_{DD}$ = 1.8 V | | 3 | 4 | - | mA |
| | | $V_{DD} \geq 3.3$ V | | 5 | 10 | - | mA |
| $I_L$ | leakage current | $V_i = V_{DD}$ or $V_{SS}$; on pin OSCCLK | | -1 | - | +1 | µA |
| **I²C-bus**[5] | | | | | | | |
| On pins SCL and SDA | | | | | | | |
| $V_I$ | input voltage | | | $V_{SS}$ - 0.5 | - | 5.5 | V |
| $V_{IL}$ | LOW-level input voltage | | | - | - | $0.3V_{DD}$ | V |
| $V_{IH}$ | HIGH-level input voltage | | | $0.7V_{DD}$ | - | - | V |
| $V_O$ | output voltage | | | -0.5 | - | +5.5 | V |

PCA8546

**Product data sheet** **Rev. 2 — 29 September 2021**

**36 / 60**

**Table 30. Static characteristics**...*continued*

$V_{DD}$ = 1.8 V to 5.5 V; $V_{SS}$ = 0 V; $V_{LCD}$ = 2.5 V to 9 V; $T_{amb}$ = -40 °C to +95 °C; unless otherwise specified.

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $I_L$ | leakage current | $V_I$ = $V_{DD}$ or $V_{SS}$ | | -1 | - | +1 | μA |
| On pin SDA | | | | | | | |
| $I_{OL}$ | LOW-level output current | output sink current | | | | | |
| | | $V_{DD}$ = 1.8 V | | 3 | 5.5 | - | mA |
| | | $V_{DD}$ = 3.3 V | | 5 | 9 | - | mA |
| SPI-bus | | | | | | | |
| $V_I$ | input voltage | on pin SCL | | $V_{SS}$ - 0.5 | - | 5.5 | V |
| | | on pins $\overline{CE}$ and SDI | | $V_{SS}$ - 0.5 | - | $V_{DD}$ + 0.5 | V |
| On pins SCL, $\overline{CE}$ and SDI | | | | | | | |
| $V_{IL}$ | LOW-level input voltage | | | - | - | $0.3V_{DD}$ | V |
| $V_{IH}$ | HIGH-level input voltage | | | $0.7V_{DD}$ | - | - | V |
| $I_L$ | leakage current | $V_I$ = $V_{DD}$ or $V_{SS}$ | | -1 | - | +1 | μA |
| LCD outputs | | | | | | | |
| $\Delta V_O$ | output voltage variation | on pins BP0 to BP3 | [6] | - | 2.5 | +10 | mV |
| | | on pins S0 to S43 | [7] | - | 2.5 | +10 | mV |
| $R_O$ | output resistance | $V_{LCD}$ = 7 V; on pins BP0 to BP3 | [8] | - | 0.9 | 5.0 | kΩ |
| | | $V_{LCD}$ = 7 V; on pins S0 to S43 | [8] | - | 1.5 | 6.0 | kΩ |

[1]  Power-down mode is enabled; I²C-bus or SPI-bus inactive.
[2]  ¹⁄₄ bias; display enabled; LCD outputs are open circuit; RAM is all written with logic 1; inputs at $V_{SS}$ or $V_{DD}$; default display prescale factor; I²C-bus or SPI-bus inactive.
[3]  Strongly linked to $V_{LCD}$ voltage. See Figure 32.
[4]  ¹⁄₄ bias; display enabled; LCD outputs are open circuit; RAM is all written with logic 1; default display prescale factor.
[5]  The I²C-bus interface of PCA8546 is 5 V tolerant.
[6]  Variation between any two backplanes on a given voltage level; static measured.
[7]  Variation between any two segments on a given voltage level; static measured.
[8]  Outputs measured one at a time.

$\frac{1}{4}$ bias; internal oscillator; display enabled; LCD outputs are open circuit; RAM is all written with logic 1; inputs at $V_{SS}$ or $V_{DD}$; default display prescale factor; $I^2C$-bus or SPI-bus inactive. Typical is defined at $V_{DD}$ = 3.3 V, 25 °C.

**Figure 31. Typical $I_{DD}$ with respect to temperature**



Power-down mode is enabled; $I^2C$-bus or SPI-bus inactive. Typical is defined at 25 °C.

**Figure 32. Typical $I_{DD(LCD)}$ in power-down mode with respect to temperature**

$\frac{1}{4}$ bias; display enabled; LCD outputs are open circuit; RAM is all written with logic 1; default display prescale factor. Typical is defined at 25 °C.

**Figure 33. Typical $I_{DD(LCD)}$ when display is active with respect to temperature**

# 13 Dynamic characteristics

**Table 31. Dynamic characteristics**

*$V_{DD}$ = 1.8 V to 5.5 V; $V_{SS}$ = 0 V; $V_{LCD}$ = 2.5 V to 9 V; $T_{amb}$ = -40 °C to +95 °C; unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $f_{clk}$ | clock frequency | output on pin OSCCLK; $V_{DD}$ = 3.3 V | [1] | 7 800 | 9 600 | 11 040 | Hz |
| $f_{clk(ext)}$ | external clock frequency | EFR = 0 | | - | - | 250 000 | Hz |
| $t_{(RESET\_N)}$ | RESET_N pulse width | LOW time | | 400 | - | - | ns |
| **External clock source used on pin OSCCLK** | | | | | | | |
| $t_{clk(H)}$ | clock HIGH time | | | 33 | - | - | µs |
| $t_{clk(L)}$ | clock LOW time | | | 33 | - | - | µs |

[1]    Frequency present on OSCCLK with default display frequency division factor.

1. -40 °C.
2. 25 °C.
3. 85 °C.

**Figure 34. Typical clock frequency with respect to V$_{DD}$ and temperature**



External clock source used on pin OSCCLK.

**Figure 35. Driver timing waveforms**



**Figure 36. RESET timing**
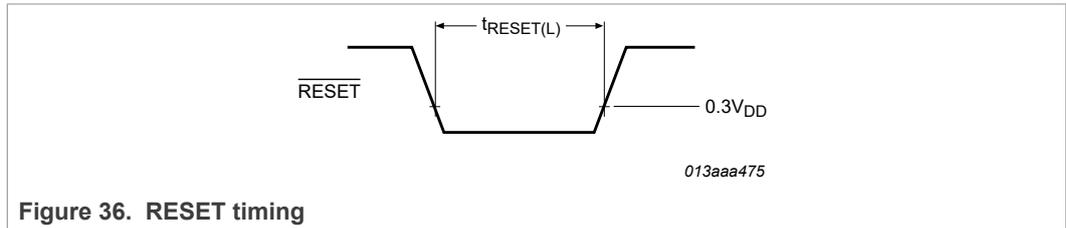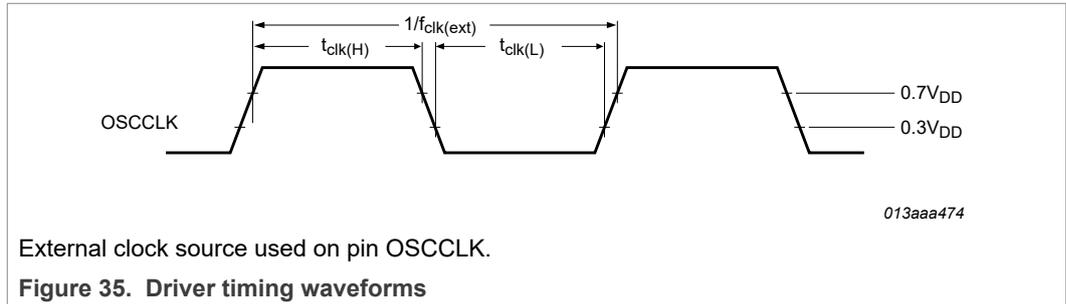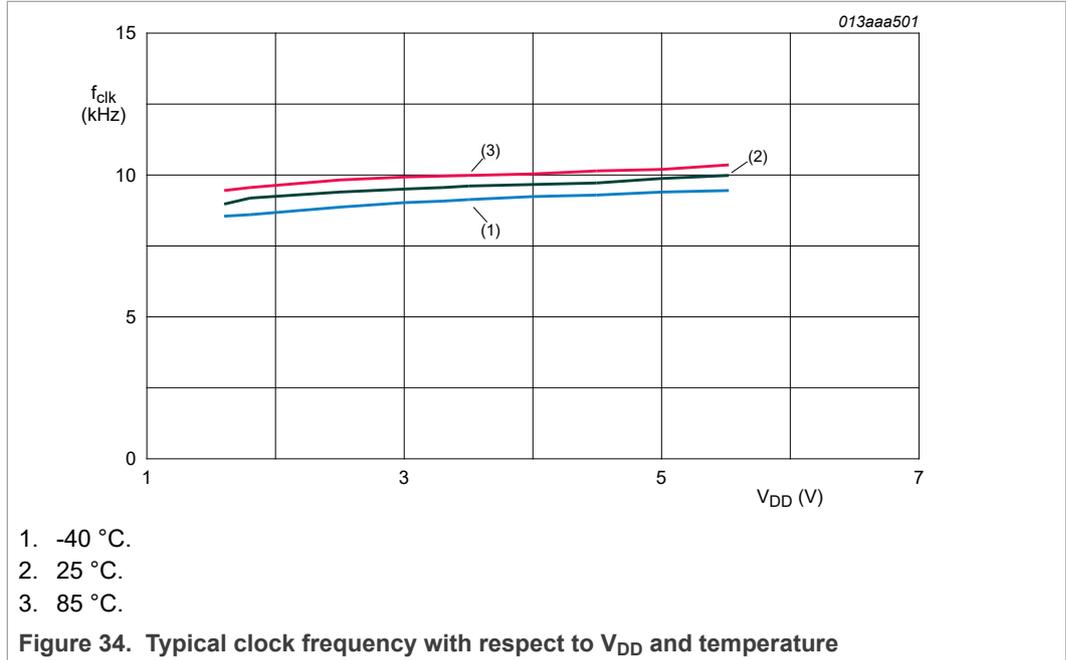
**Table 32. Timing characteristics: I$^2$C-bus**

*V$_{DD}$ = 1.8 V to 5.5 V; V$_{SS}$ = 0 V; T$_{amb}$ = -40 °C to +95 °C; unless otherwise specified. All timing values are valid within the operating supply voltage and temperature range and referenced to V$_{IL}$ and V$_{IH}$ with an input voltage swing of V$_{SS}$ to V$_{DD}$. Timing waveforms see* <u>Figure 37</u>*.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Pin SCL** | | | | | | | |
| f$_{SCL}$ | SCL clock frequency | | [1] | - | - | 400 | kHz |

PCA8546

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

**Product data sheet**

**Rev. 2 — 29 September 2021**

**40 / 60**

**Table 32. Timing characteristics: I²C-bus**...*continued*

*$V_{DD}$ = 1.8 V to 5.5 V; $V_{SS}$ = 0 V; $T_{amb}$ = -40 °C to +95 °C; unless otherwise specified. All timing values are valid within the operating supply voltage and temperature range and referenced to $V_{IL}$ and $V_{IH}$ with an input voltage swing of $V_{SS}$ to $V_{DD}$. Timing waveforms see* Figure 37.

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $t_{LOW}$ | LOW period of the SCL clock | | | 1.3 | - | - | µs |
| $t_{HIGH}$ | HIGH period of the SCL clock | | | 0.6 | - | - | µs |
| **Pin SDA** | | | | | | | |
| $t_{SU;DAT}$ | data set-up time | | | 100 | - | - | ns |
| $t_{HD;DAT}$ | data hold time | | | 0 | - | - | ns |
| **Pins SCL and SDA** | | | | | | | |
| $t_{BUF}$ | bus free time between a STOP and START condition | | | 1.3 | - | - | µs |
| $t_{SU;STO}$ | set-up time for STOP condition | | | 0.6 | - | - | µs |
| $t_{HD;STA}$ | hold time (repeated) START condition | | | 0.6 | - | - | µs |
| $t_{SU;STA}$ | set-up time for a repeated START condition | | | 0.6 | - | - | µs |
| $t_r$ | rise time of both SDA and SCL signals | $f_{SCL}$ = 400 kHz | | - | - | 0.3 | µs |
| | | $f_{SCL}$ = 100 kHz | | - | - | 1.0 | µs |
| $t_f$ | fall time of both SDA and SCL signals | | | - | - | 0.3 | µs |
| $t_{VD;ACK}$ | data valid acknowledge time | | [2] | 0.6 | - | - | µs |
| $t_{VD;DAT}$ | data valid time | | [3] | 0.6 | - | - | µs |
| $C_b$ | capacitive load for each bus line | | | - | - | 400 | pF |
| $t_{SP}$ | pulse width of spikes that must be suppressed by the input filter | | [4] | - | - | 50 | ns |

[1] The minimum SCL clock frequency is limited by the bus time-out feature, which resets the serial bus interface if either the SDA or SCL is held LOW for a minimum of 25 ms. The bus time-out feature must be disabled for DC operation.

[2] $t_{VD;ACK}$ = time for acknowledgement signal from SCL LOW to SDA output LOW.

[3] $t_{VD;DAT}$ = minimum time for valid SDA output following SCL LOW.

[4] Input filters on the SDA and SCL inputs suppress noise spikes of less than 50 ns.
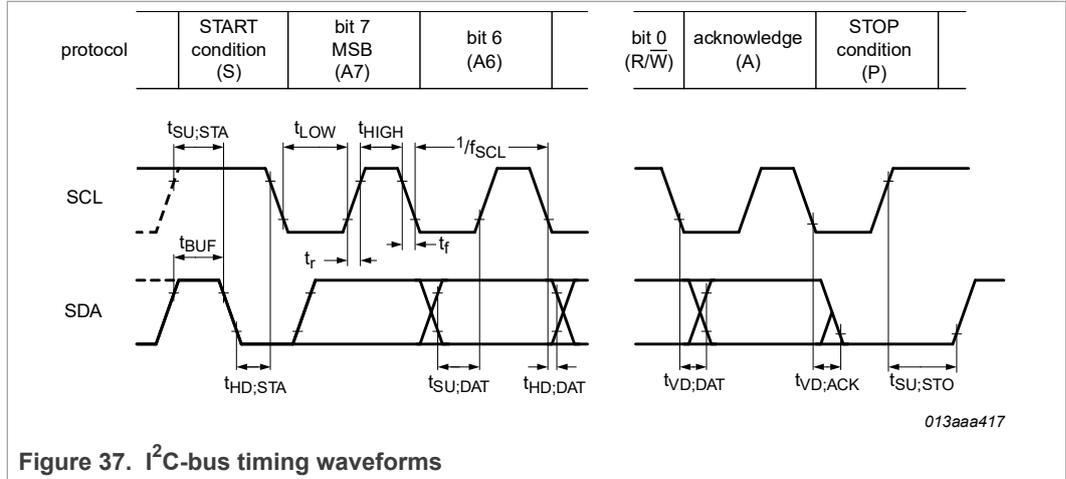
**Figure 37.** I$^2$C-bus timing waveforms

**Table 33.** Timing characteristics: SPI-bus

$V_{DD}$ = 1.8 V to 5.5 V; $V_{SS}$ = 0 V; $T_{amb}$ = -40 °C to +95 °C. All timing values are valid within the operating supply voltage and temperature range and referenced to $V_{IL}$ and $V_{IH}$ with an input voltage swing of $V_{SS}$ to $V_{DD}$. Timing waveforms see Figure 38.

| Symbol | Parameter | Conditions | $V_{DD}$ < 2.7 V | | $V_{DD} \geq$ 2.7 V | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| $f_{clk(SCL)}$ | SCL clock frequency | | - | 2 | - | 5 | MHz |
| $t_{SCL}$ | SCL time | | 500 | - | 200 | - | ns |
| $t_{clk(H)}$ | clock HIGH time | | 200 | - | 80 | - | ns |
| $t_{clk(L)}$ | clock LOW time | | 200 | - | 80 | - | ns |
| $t_r$ | rise time | for SCL signal | - | 100 | - | 100 | ns |
| $t_f$ | fall time | for SCL signal | - | 100 | - | 100 | ns |
| $t_{su(CE\_N)}$ | CE_N set-up time | | 150 | - | 80 | - | ns |
| $t_{h(CE\_N)}$ | CE_N hold time | | 0 | - | 0 | - | ns |
| $t_{rec(CE\_N)}$ | CE_N recovery time | | 100 | - | 100 | - | ns |
| $t_{su}$ | set-up time | set-up time for SDI data | 10 | - | 5 | - | ns |
| $t_h$ | hold time | hold time for SDI data | 25 | - | 10 | - | ns |

PCA8546

**Product data sheet** **Rev. 2 — 29 September 2021**

**42 / 60**
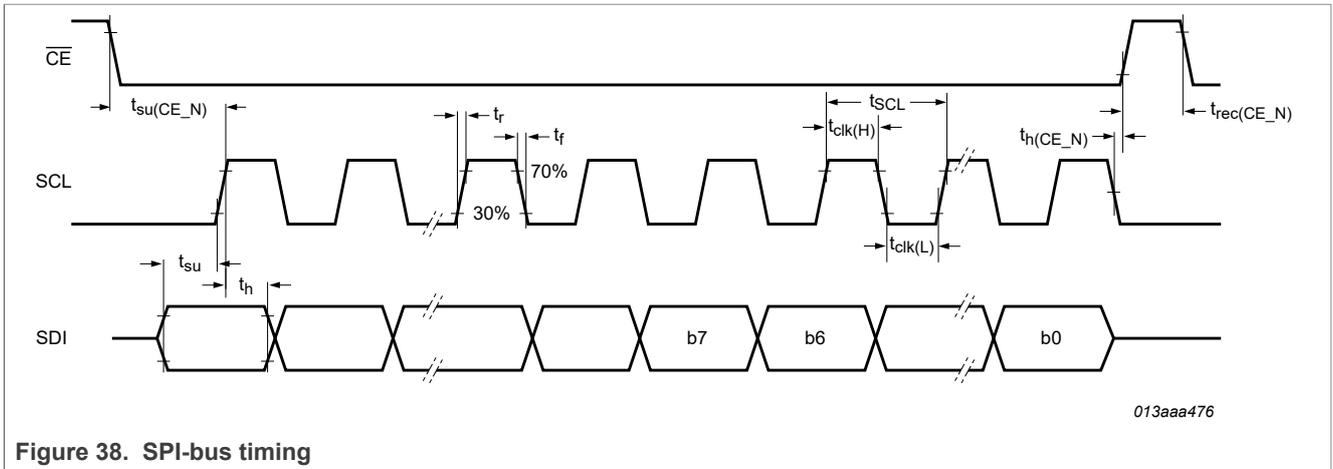
**Figure 38. SPI-bus timing**

## 14 Package outline

**TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm**

**SOT364-1**
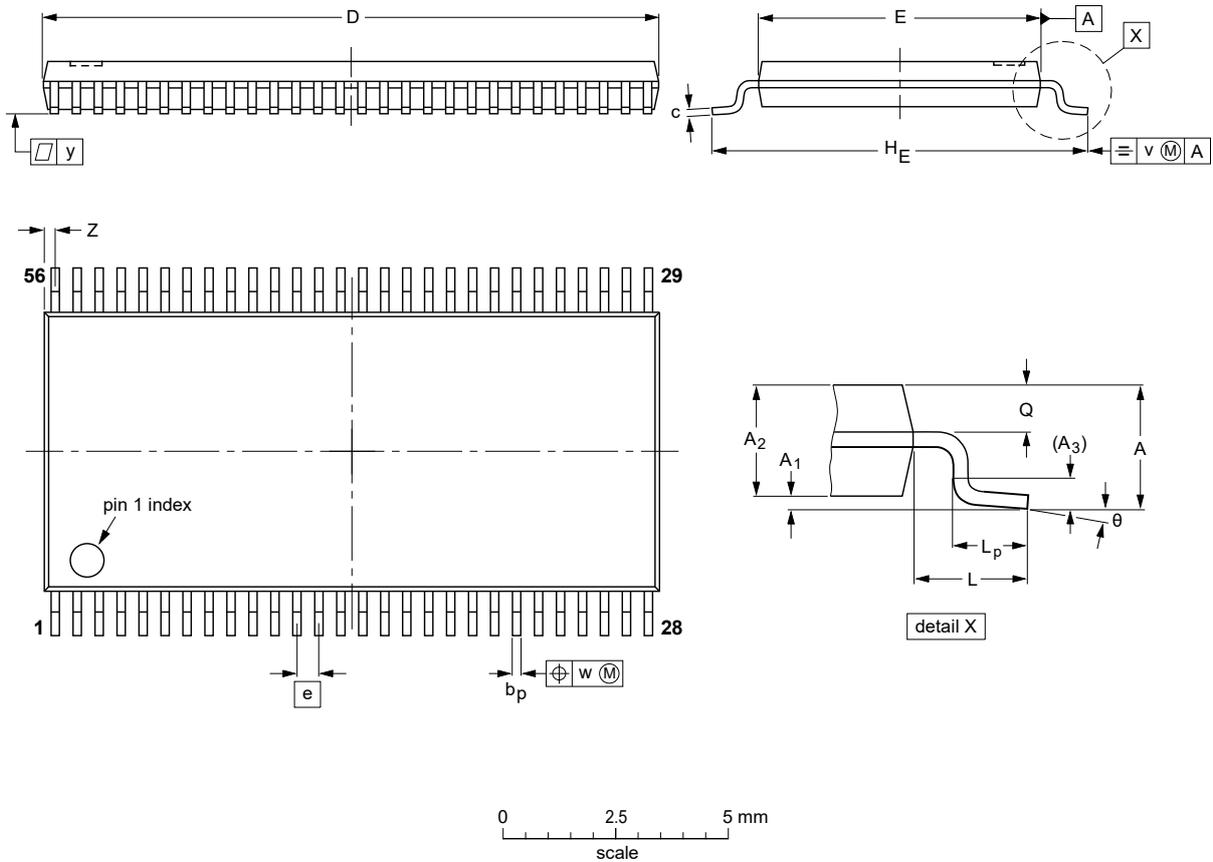


**DIMENSIONS (mm are the original dimensions).**

| UNIT | A max. | A₁ | A₂ | A₃ | b_p | c | D(1) | E(2) | e | H_E | L | L_p | Q | v | w | y | Z | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.2 | 0.15 0.05 | 1.05 0.85 | 0.25 | 0.28 0.17 | 0.2 0.1 | 14.1 13.9 | 6.2 6.0 | 0.5 | 8.3 7.9 | 1 | 0.8 0.4 | 0.50 0.35 | 0.25 | 0.08 | 0.1 | 0.5 0.1 | 8° 0° |

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT364-1 | | MO-153 | | | | 99-12-27 03-02-19 |

**Figure 39. Package outline SOT364-1 (TSSOP56)**

PCA8546

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

**Product data sheet**

**Rev. 2 — 29 September 2021**

**44 / 60**

## 15 Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling Metal-Oxide Semiconductor (MOS) devices ensure that all normal precautions are taken as described in *JESD625-A*, *IEC 61340-5* or equivalent standards.

## 16 Packing information

### 16.1 Tape and reel information



**Figure 40. Tape and reel details for PCA8546ATT and PCA8546BTT**
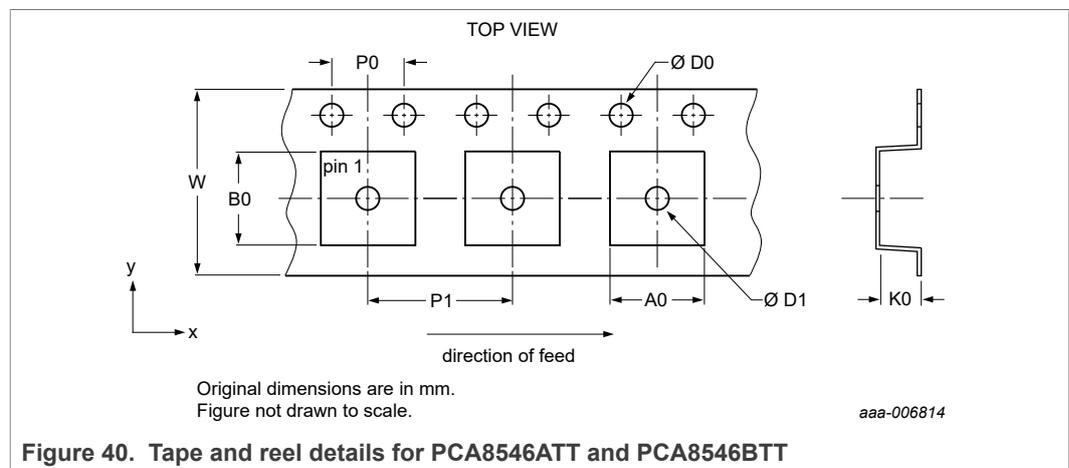
**Table 34. Carrier tape dimensions of PCA8546ATT and PCA8546BTT**

| Symbol | Description | Value | Unit |
|---|---|---|---|
| **Compartments** | | | |
| A0 | pocket width in x direction | 8.65 to 8.9 | mm |
| B0 | pocket width in y direction | 14.4 to 15.8 | mm |
| K0 | pocket depth | 1.5 to 1.8 | mm |
| P1 | pocket hole pitch | 12 | mm |
| D1 | pocket hole diameter | 1.5 to 2.05 | mm |
| **Overall dimensions** | | | |
| W | tape width | 24 | mm |
| D0 | sprocket hole diameter | 1.5 to 1.55 | mm |
| P0 | sprocket hole pitch | 4 | mm |

## 17 Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

PCA8546

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

**Product data sheet**

**Rev. 2 — 29 September 2021**

**45 / 60**

## 17.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

## 17.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

• Through-hole components
• Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

• Board specifications, including the board finish, solder masks and vias
• Package footprints, including solder thieves and orientation
• The moisture sensitivity level of the packages
• Package placement
• Inspection and repair
• Lead-free soldering versus SnPb soldering

## 17.3 Wave soldering

Key characteristics in wave soldering are:

• Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
• Solder bath specifications, including temperature and impurities

## 17.4 Reflow soldering

Key characteristics in reflow soldering are:

• Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 41) than a SnPb process, thus reducing the process window
• Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board

- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 35 and Table 36

**Table 35. SnPb eutectic process (from J-STD-020D)**

| Package thickness (mm) | Package reflow temperature (°C) | |
|---|---|---|
| | Volume (mm³) | |
| | < 350 | ≥ 350 |
| < 2.5 | 235 | 220 |
| ≥ 2.5 | 220 | 220 |

**Table 36. Lead-free process (from J-STD-020D)**

| Package thickness (mm) | Package reflow temperature (°C) | | |
|---|---|---|---|
| | Volume (mm³) | | |
| | < 350 | 350 to 2000 | > 2000 |
| < 1.6 | 260 | 260 | 260 |
| 1.6 to 2.5 | 260 | 250 | 245 |
| > 2.5 | 250 | 245 | 245 |

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 41.



MSL: Moisture Sensitivity Level
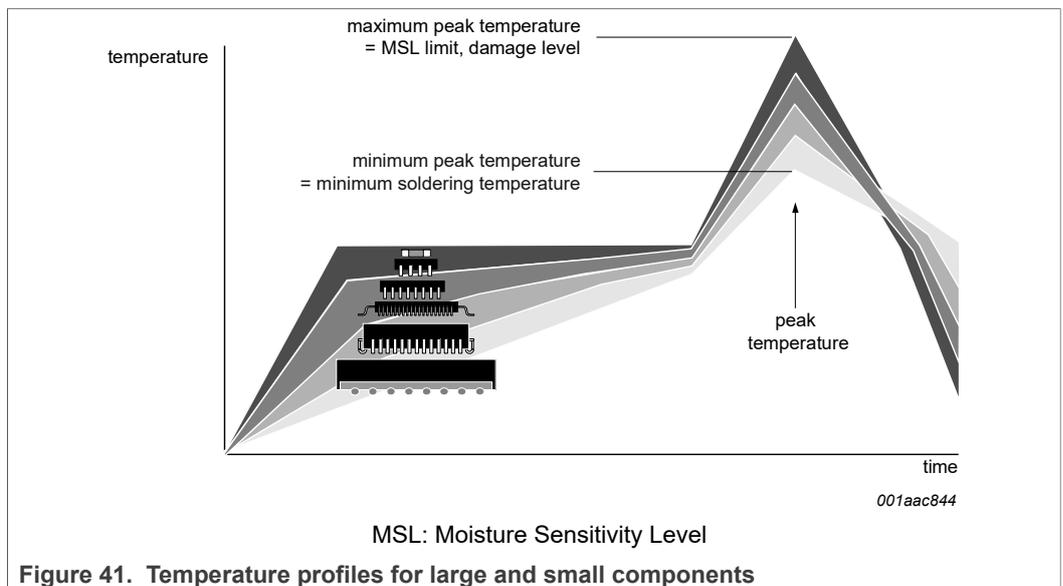
**Figure 41. Temperature profiles for large and small components**

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

PCA8546

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

**Product data sheet**

**Rev. 2 — 29 September 2021**

**48 / 60**

## 18 Footprint information for reflow soldering

**Footprint information for reflow soldering of TSSOP56 package** **SOT364-1**



Generic footprint pattern
Refer to the package outline drawing for actual layout

🔲 solder land

- - - - occupied area

DIMENSIONS in mm

| P1 | P2 | Ay | By | C | D1 | D2 | Gx | Gy | Hx | Hy |
|---|---|---|---|---|---|---|---|---|---|---|
| 0.500 | 0.560 | 8.900 | 6.100 | 1.400 | 0.280 | 0.400 | 14.270 | 7.000 | 16.600 | 9.150 |
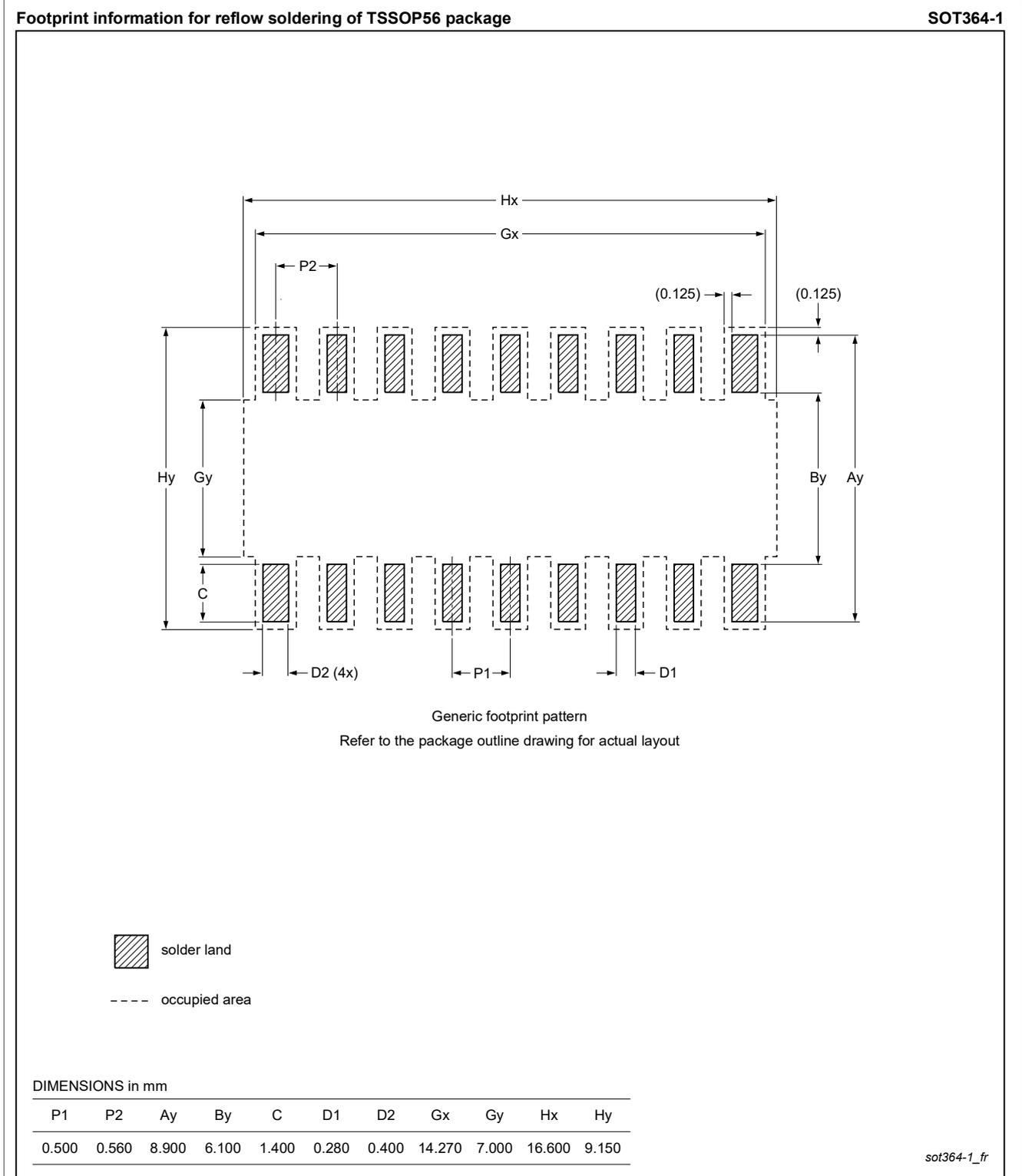
*sot364-1_fr*

**Figure 42. Footprint information for reflow soldering of SOT364-1 (TSSOP56) package**

# 19 Appendix

## 19.1 LCD segment driver selection

Table 37. Selection of LCD segment drivers

| Type name | Number of elements at MUX | | | | | | | V_DD (V) | V_LCD (V) | f_fr (Hz) | V_LCD (V) charge pump | V_LCD (V) temperature compensat. | T_amb (°C) | Interface | Package | AEC-Q100 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1:1 | 1:2 | 1:3 | 1:4 | 1:6 | 1:8 | 1:9 | | | | | | | | | |
| PCA8561AHN[1] | 18 | 36 | 54 | 72 | - | - | - | 1.8 to 5.5 | 1.8 to 5.5 | 32 to 256[2] | N | N | -40 to 105 | I²C | HVQFN32 | Y |
| PCA8561BHN[1] | 18 | 36 | 54 | 72 | - | - | - | 1.8 to 5.5 | 1.8 to 5.5 | 32 to 256[2] | N | N | -40 to 105 | SPI | HVQFN32 | Y |
| PCF8566TS | 24 | 48 | 72 | 96 | - | - | - | 2.5 to 6 | 2.5 to 6 | 69 | N | N | -40 to 85 | I²C | VSO40 | N |
| PCF85162T | 32 | 64 | 96 | 128 | - | - | - | 1.8 to 5.5 | 2.5 to 6.5 | 82 | N | N | -40 to 85 | I²C | TSSOP48 | N |
| PCA85162T | 32 | 64 | 96 | 128 | - | - | - | 1.8 to 5.5 | 2.5 to 8 | 110 | N | N | -40 to 95 | I²C | TSSOP48 | Y |
| PCA85262ATT | 32 | 64 | 96 | 128 | - | - | - | 1.8 to 5.5 | 2.5 to 8 | 200 | N | N | -40 to 105 | I²C | TSSOP48 | Y |
| PCF8551ATT[1] | 36 | 72 | 108 | 144 | - | - | - | 1.8 to 5.5 | 1.8 to 5.5 | 32 to 128[2] | N | N | -40 to 85 | I²C | TSSOP48 | N |
| PCF8551BTT[1] | 36 | 72 | 108 | 144 | - | - | - | 1.8 to 5.5 | 1.8 to 5.5 | 32 to 128[2] | N | N | -40 to 85 | SPI | TSSOP48 | N |
| PCA8551ATT[1] | 36 | 72 | 108 | 144 | - | - | - | 1.8 to 5.5 | 1.8 to 5.5 | 32 to 256[2] | N | N | -40 to 105 | I²C | TSSOP48 | Y |
| PCA8551BTT[1] | 36 | 72 | 108 | 144 | - | - | - | 1.8 to 5.5 | 1.8 to 5.5 | 32 to 256[2] | N | N | -40 to 105 | SPI | TSSOP48 | Y |
| PCF85176T | 40 | 80 | 120 | 160 | - | - | - | 1.8 to 5.5 | 2.5 to 6.5 | 82 | N | N | -40 to 85 | I²C | TSSOP56 | N |
| PCA85176T | 40 | 80 | 120 | 160 | - | - | - | 1.8 to 5.5 | 2.5 to 8 | 110 | N | N | -40 to 95 | I²C | TSSOP56 | Y |
| PCA85276ATT | 40 | 80 | 120 | 160 | - | - | - | 1.8 to 5.5 | 2.5 to 8 | 200 | N | N | -40 to 105 | I²C | TSSOP56 | Y |
| PCF85176H | 40 | 80 | 120 | 160 | - | - | - | 1.8 to 5.5 | 2.5 to 6.5 | 82 | N | N | -40 to 85 | I²C | TQFP64 | N |
| PCA85176H | 40 | 80 | 120 | 160 | - | - | - | 1.8 to 5.5 | 2.5 to 8 | 82 | N | N | -40 to 95 | I²C | TQFP64 | Y |
| PCF8553ATT[1] | 40 | 80 | 120 | 160 | - | - | - | 1.8 to 5.5 | 1.8 to 5.5 | 32 to 128[2] | N | N | -40 to 85 | I²C | TSSOP56 | N |
| PCF8553BTT[1] | 40 | 80 | 120 | 160 | - | - | - | 1.8 to 5.5 | 1.8 to 5.5 | 32 to 128[2] | N | N | -40 to 85 | SPI | TSSOP56 | N |
| PCA8553ATT[1] | 40 | 80 | 120 | 160 | - | - | - | 1.8 to 5.5 | 1.8 to 5.5 | 32 to 256[2] | N | N | -40 to 105 | I²C | TSSOP56 | Y |
| PCA8553BTT[1] | 40 | 80 | 120 | 160 | - | - | - | 1.8 to 5.5 | 1.8 to 5.5 | 32 to 256[2] | N | N | -40 to 105 | SPI | TSSOP56 | Y |
| PCA8546ATT[1] | - | - | - | 176 | - | - | - | 1.8 to 5.5 | 2.5 to 9 | 60 to 300[2] | N | N | -40 to 95 | I²C | TSSOP56 | Y |
| PCA8546BTT[1] | - | - | - | 176 | - | - | - | 1.8 to 5.5 | 2.5 to 9 | 60 to 300[2] | N | N | -40 to 95 | SPI | TSSOP56 | Y |
| PCA8547AHT[1] | 44 | 88 | - | 176 | - | - | - | 1.8 to 5.5 | 2.5 to 9 | 60 to 300[2] | Y | Y[3] | -40 to 95 | I²C | TQFP64 | Y |
| PCA8547BHT[1] | 44 | 88 | - | 176 | - | - | - | 1.8 to 5.5 | 2.5 to 9 | 60 to 300[2] | Y | Y[3] | -40 to 95 | SPI | TQFP64 | Y |
| PCF85134HL | 60 | 120 | 180 | 240 | - | - | - | 1.8 to 5.5 | 2.5 to 6.5 | 82 | N | N | -40 to 85 | I²C | LQFP80 | N |

PCA8546

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2021. All rights reserved.

**Product data sheet** **Rev. 2 — 29 September 2021**

**51 / 60**

Table 37. Selection of LCD segment drivers...*continued*

| Type name | Number of elements at MUX | | | | | | | V_DD (V) | V_LCD (V) | f_fr (Hz) | V_LCD (V) charge pump | V_LCD (V) temperature compensat. | T_amb (°C) | Interface | Package | AEC-Q100 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1:1 | 1:2 | 1:3 | 1:4 | 1:6 | 1:8 | 1:9 | | | | | | | | | |
| PCA85134H | 60 | 120 | 180 | 240 | - | - | - | 1.8 to 5.5 | 2.5 to 8 | 82 | N | N | -40 to 95 | I$^2$C | LQFP80 | Y |
| PCA8543AHL | 60 | 120 | - | 240 | - | - | - | 2.5 to 5.5 | 2.5 to 9 | 60 to 300[2] | Y | Y | -40 to 105 | I$^2$C | LQFP80 | Y |
| PCF8545ATT[1] | - | - | - | 176 | 252 | 320 | - | 1.8 to 5.5 | 2.5 to 5.5 | 60 to 300[2] | N | N | -40 to 85 | I$^2$C | TSSOP56 | N |
| PCF8545BTT[1] | - | - | - | 176 | 252 | 320 | - | 1.8 to 5.5 | 2.5 to 5.5 | 60 to 300[2] | N | N | -40 to 85 | SPI | TSSOP56 | N |
| PCF8536AT[4] | - | - | - | 176 | 252 | 320 | - | 1.8 to 5.5 | 2.5 to 9 | 60 to 300[2] | N | N | -40 to 85 | I$^2$C | TSSOP56 | N |
| PCF8536BT[4] | - | - | - | 176 | 252 | 320 | - | 1.8 to 5.5 | 2.5 to 9 | 60 to 300[2] | N | N | -40 to 85 | SPI | TSSOP56 | N |
| PCA8536AT[4] | - | - | - | 176 | 252 | 320 | - | 1.8 to 5.5 | 2.5 to 9 | 60 to 300[2] | N | N | -40 to 95 | I$^2$C | TSSOP56 | Y |
| PCA8536BT[4] | - | - | - | 176 | 252 | 320 | - | 1.8 to 5.5 | 2.5 to 9 | 60 to 300[2] | N | N | -40 to 95 | SPI | TSSOP56 | Y |
| PCF8537AH | 44 | 88 | - | 176 | 276 | 352 | - | 1.8 to 5.5 | 2.5 to 9 | 60 to 300[2] | Y | Y[3] | -40 to 85 | I$^2$C | TQFP64 | N |
| PCF8537BH | 44 | 88 | - | 176 | 276 | 352 | - | 1.8 to 5.5 | 2.5 to 9 | 60 to 300[2] | Y | Y[3] | -40 to 85 | SPI | TQFP64 | N |
| PCA8537AH | 44 | 88 | - | 176 | 276 | 352 | - | 1.8 to 5.5 | 2.5 to 9 | 60 to 300[2] | Y | Y[3] | -40 to 95 | I$^2$C | TQFP64 | Y |
| PCA8537BH | 44 | 88 | - | 176 | 276 | 352 | - | 1.8 to 5.5 | 2.5 to 9 | 60 to 300[2] | Y | Y[3] | -40 to 95 | SPI | TQFP64 | Y |
| PCA9620H | 60 | 120 | - | 240 | 320 | 480 | - | 2.5 to 5.5 | 2.5 to 9 | 60 to 300[2] | Y | Y[3] | -40 to 105 | I$^2$C | LQFP80 | Y |
| PCA9620U | 60 | 120 | - | 240 | 320 | 480 | - | 2.5 to 5.5 | 2.5 to 9 | 60 to 300[2] | Y | Y[3] | -40 to 105 | I$^2$C | bare die | Y |
| PCF8552DUG[1] | 36 | 72 | 108 | 144 | - | - | - | 1.8 to 5.5 | 1.8 to 5.5 | 32 to 128[2] | N | N | -40 to 85 | I$^2$C, SPI | bare die | N |
| PCA8552DUG[1] | 36 | 72 | 108 | 144 | - | - | - | 1.8 to 5.5 | 1.8 to 5.5 | 32 to 256[2] | N | N | -40 to 105 | I$^2$C, SPI | bare die | Y |
| PCF8576DU | 40 | 80 | 120 | 160 | - | - | - | 1.8 to 5.5 | 2.5 to 6.5 | 77 | N | N | -40 to 85 | I$^2$C | bare die | N |
| PCF8576EUG | 40 | 80 | 120 | 160 | - | - | - | 1.8 to 5.5 | 2.5 to 6.5 | 77 | N | N | -40 to 85 | I$^2$C | bare die | N |
| PCA8576FUG[1] | 40 | 80 | 120 | 160 | - | - | - | 1.8 to 5.5 | 2.5 to 8 | 200 | N | N | -40 to 105 | I$^2$C | bare die | Y |
| PCF85133U | 80 | 160 | 240 | 320 | - | - | - | 1.8 to 5.5 | 2.5 to 6.5 | 82, 110[5] | N | N | -40 to 85 | I$^2$C | bare die | N |
| PCA85133U | 80 | 160 | 240 | 320 | - | - | - | 1.8 to 5.5 | 2.5 to 8 | 82, 110[5] | N | N | -40 to 95 | I$^2$C | bare die | Y |
| PCA85233U | 80 | 160 | 240 | 320 | - | - | - | 1.8 to 5.5 | 2.5 to 8 | 150, 220[5] | N | N | -40 to 105 | I$^2$C | bare die | Y |
| PCA8530DUG[1] | 102 | 204 | - | 408 | - | - | - | 2.5 to 5.5 | 4 to 12 | 45 to 300[2] | Y | Y[3] | -40 to 105 | I$^2$C, SPI | bare die | Y |
| PCF85132U | 160 | 320 | 480 | 640 | - | - | - | 1.8 to 5.5 | 1.8 to 8 | 60 to 90[2] | N | N | -40 to 85 | I$^2$C | bare die | N |

**Table 37. Selection of LCD segment drivers**...*continued*

| Type name | Number of elements at MUX | | | | | | | V_DD (V) | V_LCD (V) | f_fr (Hz) | V_LCD (V) charge pump | V_LCD (V) temperature compensat. | T_amb (°C) | Interface | Package | AEC-Q100 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 1:1 | 1:2 | 1:3 | 1:4 | 1:6 | 1:8 | 1:9 | | | | | | | | | |
| PCA85132U | 160 | 320 | 480 | 640 | - | - | - | 1.8 to 5.5 | 1.8 to 8 | 60 to 90[2] | N | N | -40 to 95 | I²C | bare die | Y |
| PCA85232U | 160 | 320 | 480 | 640 | - | - | - | 1.8 to 5.5 | 1.8 to 8 | 117 to 176[2] | N | N | -40 to 95 | I²C | bare die | Y |
| PCF8538UG[1] | 102 | 204 | - | 408 | 612 | 816 | 918 | 2.5 to 5.5 | 4 to 12 | 45 to 300[2] | Y | Y[3] | -40 to 85 | I²C, SPI[5] | bare die | N |
| PCA8538UG | 102 | 204 | - | 408 | 612 | 816 | 918 | 2.5 to 5.5 | 4 to 12 | 45 to 300[2] | Y | Y[3] | -40 to 105 | I²C, SPI[5] | bare die | Y |

[1]  In development.
[2]  Can be selected by command.
[3]  Extra feature: Temperature sensor.
[4]  Extra feature: 6 PWM channels.
[5]  Can be selected by pin configuration.

## 20 Abbreviations

**Table 38. Abbreviations**

| Acronym | Description |
|---------|-------------|
| CDM | Charged-Device Model |
| CMOS | Complementary Metal-Oxide Semiconductor |
| DC | Direct Current |
| EMC | ElectroMagnetic Compatibility |
| EPROM | Erasable Programmable Read-Only Memory |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| $I^2C$ | Inter-Integrated Circuit bus |
| IC | Integrated Circuit |
| LCD | Liquid Crystal Display |
| LSB | Least Significant Bit |
| MSB | Most Significant Bit |
| MSL | Moisture Sensitivity Level |
| MUX | Multiplexer |
| OTP | One Time Programmable |
| PCB | Printed-Circuit Board |
| POR | Power-On Reset |
| RC | Resistance-Capacitance |
| RAM | Random Access Memory |
| RGB | Red Green Blue |
| RMS | Root Mean Square |
| SCL | Serial CLock line |
| SDA | Serial DAta line |
| SPI | Serial Peripheral Interface |

## 21 References

[1] JESD22-A114 Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)

[2] JESD22-C101 Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components

[3] JESD78 IC Latch-Up Test

[4] UM10569 Store and transport requirements

PCA8546
All information provided in this document is subject to legal disclaimers.
© NXP B.V. 2021. All rights reserved.

**Product data sheet**
Rev. 2 — 29 September 2021

**54 / 60**

## 22 Revision history

**Table 39. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| PCA8546 v.2 | 20210929 | Product data sheet | PCN202102010F01 | PCA8546 v.1 |
| Modifications: | • Updated Ordering information. See Change notice column.<br>• Removed Marking information (formerly Section 5).<br>• The terms "master" and "slave" changed to "controller" and "target" to comply with NXP inclusive language policy. | | | |
| PCA8546 v.1 | 20131113 | Product data sheet | - | - |

## 23  Legal information

### 23.1  Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1]  Please consult the most recently issued document before initiating or completing a design.

[2]  The term 'short data sheet' is explained in section "Definitions".

[3]  The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

### 23.2  Definitions

**Draft** — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

**Short data sheet** — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

**Product specification** — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

### 23.3  Disclaimers

**Limited warranty and liability** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors. In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory. Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without

notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification. Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products. NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

**Limiting values** — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

**Terms and conditions of commercial sale** — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

**No offer to sell or license** — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Suitability for use in automotive applications** — This NXP product has been qualified for use in automotive applications. If this product is used by customer in the development of, or for incorporation into, products or services (a) used in safety critical applications or (b) in which failure could lead to death, personal injury, or severe physical or environmental damage (such products and services hereinafter referred to as "Critical Applications"),

PCA8546

Product data sheet

All information provided in this document is subject to legal disclaimers.

Rev. 2 — 29 September 2021

© NXP B.V. 2021. All rights reserved.

56 / 60

then customer makes the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, safety, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP. As such, customer assumes all risk related to use of any products in Critical Applications and NXP and its suppliers shall not be liable for any such use by customer. Accordingly, customer will indemnify and hold NXP harmless from any claims, liabilities, damages and associated costs and expenses (including attorneys' fees) that NXP may incur related to customer's incorporation of any product in a Critical Application.

**Export control** — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

**Translations** — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

## 23.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

**I²C-bus** — logo is a trademark of NXP B.V.

**NXP** — wordmark and logo are trademarks of NXP B.V.

PCA8546

**Product data sheet**

**Rev. 2 — 29 September 2021**

**57 / 60**

## Tables

## Figures

# Contents

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.