<b>PCN Number:</b> 2019120		912050	5000 <b>PCN Date:</b>					Dec. 9, 2019					
Title: Datasheet for DRV884			8847	7									
Customer Contact: PCN Ma			Manag	lanager					e	vices			
Cha	inge Type:										•		
	Assembly Site				Design					Wafer	<sup>-</sup> Bump Site		
	Assembly Process			🛛 Data Sheet					Wafer Bump Material				
	Assembly Materials			Part number change						Wafer Bump Process			
	Mechanical Specification			Test Site					Wafer Fab Site				
	Packing/Shipping/Labeling			Test Process						- Fab Material	S		
										Wafer	- Fab Process		
Notification Details													
Description of Change:													
	Texas Instruments Incorporated is announcing an information only notification.												
The product datasheet(s) is being updated as summarized below. The following change history provides further details.													
Ine	rollowing change i	listory	provid	les	rurther de	talis.							
	Trues												
TEXAS INSTRUMENTS DRV8847													
	SLVSE65B – JULY 2018 – REVISED SEPTEMBER 2019												
Ch	nanges from Revision A	(July 2	018) to E	ovie	ion B							Page	
	-		-										
•	<ul> <li>Changed the Low On-State Resistance to be the indicated value when VM &gt; 5 V</li></ul>												
•	Changed nFAULT pin type to OD/I												
•	Changed VM description to indicate 0.1-uF capacitor should be ceramic												
•	Changed digital pin voltage (IN1, IN2, IN3, IN4, TRQ, nSLEEP, nFAULT, SCL, SDA) maximum voltage from 5.5 V												
	to 5.75 V												
	Changed the Phase node pin voltage specification's name to Continuous phase node pin voltage												
	Added for ISEN12, ISEN34 specification a footnote stating transients of +- 1V for less than 25 ns are acceptable												
•	and thermal limits must be observed												
•		Changed V(ESD) specification's value to 4000 V											
•	Changed the V <sub>IL</sub> specification to be two specifications based on test conditions VM < 7 V and VM >= 7 V7												
•	Changed the I <sub>IH</sub> specification's minimum value to 18 uA for test condition IN1, IN2, IN3, IN4, TRQ, VIN = 5 V and to 10 uA for test condition nSLEEP, V <sub>IN</sub> = minimum (VM, 5 V)												
•	Added to I <sub>OCP</sub> specification a minimum value									8			
•	Changed pin naming of Block Diagram for DRV8847S figure												
•	Deleted ceramic from C <sub>VM1</sub>										17		
•	Changed the relay or so												
•	Added sentence to clari	fy nFAU	LT pin be	ehavi	or when oper	n load is detec	ted					36	
•	Added sentence to clarify nFAULT pin behavior during power-up												
•	Added an Open Load Implementation section												
•	Added a Layout Recom	mendati	on of 16-	Pin C	QFN Package	for Double La	iyer Boa	rd fi	gui	e		62	
	datasheet number	· will b	e chan	ging									
De	vice Family				Chang	e From:				Chang	е То:		
DR	DRV8847				SLVSE65A				SLVSE65B				
		revia	wed at	the	datachor	t links pro	habiv						
These changes may be reviewed at the datasheet links provided.													
http://www.ti.com/product/DRV8847													
-													
	son for Change:												
To accurately reflect device characteristics.													

Anticipated impact on Fit, Form, Function, Quality or Reliability (positive / negative): No anticipated impact. This is a specification change announcement only. There are no changes to the actual device.

 It of the actual device.

 Changes to product identification resulting from this PCN:

 None.
 Product Affected:

 DRV8847PWPR
 DRV8847PWR
 DRV8847RTER

 DRV8847SPWR
 DRV8847SPWR
 DRV8847RTER

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