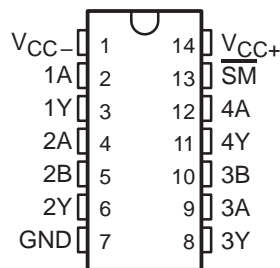


# SN75C198 QUADRUPLE LOW-POWER LINE DRIVERS

SLLS051C – JULY 1990 – REVISED MARCH 1997

- Meets ANSI EIA/TIA-232-E and ITU Recommendation V.28
- Very Low Supply Current
- Sleep Mode:  
3-State Outputs in High-Impedance State  
Ultra-Low Supply Current . . . 17  $\mu$ A Typ
- Improved Functional Replacement for:  
SN75188,  
Motorola MC1488,  
National Semiconductor DS14C88, and  
DS1488
- CMOS- and TTL-Compatible Data Inputs
- On-Chip Slew-Rate Limit . . . 30 V/ $\mu$ s
- Output Current Limit . . . 10 mA Typ
- Wide Supply Voltage Range . . .  $\pm$ 4.5 V to  $\pm$ 15 V

D OR N PACKAGE  
(TOP VIEW)



NOT RECOMMENDED FOR NEW DESIGNS

## description

The SN75C198 is a monolithic low-power BI-MOS device containing four low-power line drivers designed to interface data terminal equipment (DTE) with data circuit-terminating equipment (DCE) in conformance with the specifications of ANSI EIA/TIA-232-E. The drivers of the SN75C198 are similar to those of the SN75C188 quadruple driver. The drivers have a controlled-output slew rate that is limited to a maximum of 30 V/ $\mu$ s. This feature eliminates the need for external components.

The sleep-mode input,  $\overline{SM}$ , can switch the outputs to high impedance, which avoids the transmission of corrupted data during power-up and allows significant system power savings during data-off periods.

The SN75C198 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS			OUTPUT Y
$\overline{SM}$	A	B	
H	H	H	L
H	L	X	H
H	X	L	H
L	X	X	Z

H = high level, L = low level,  
X = irrelevant, Z = high impedance



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

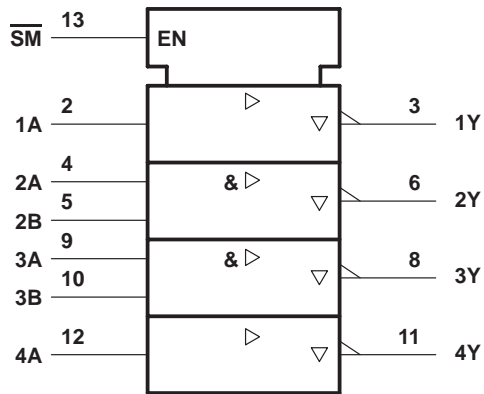
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 1997, Texas Instruments Incorporated

# SN75C198 QUADRUPLE LOW-POWER LINE DRIVERS

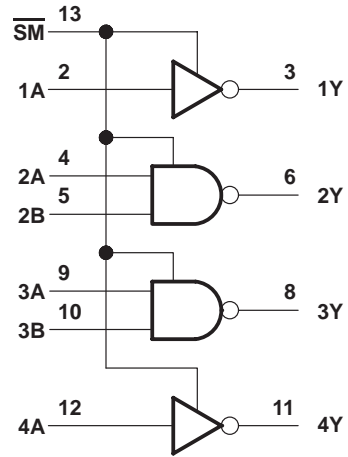
SLLS051C – JULY 1990 – REVISED MARCH 1997

## logic symbol†

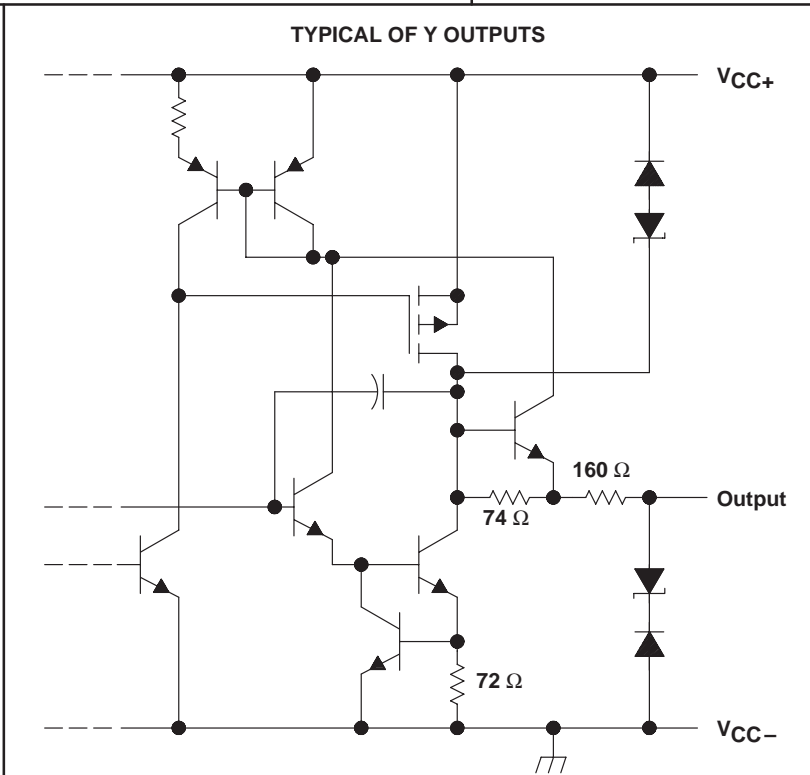
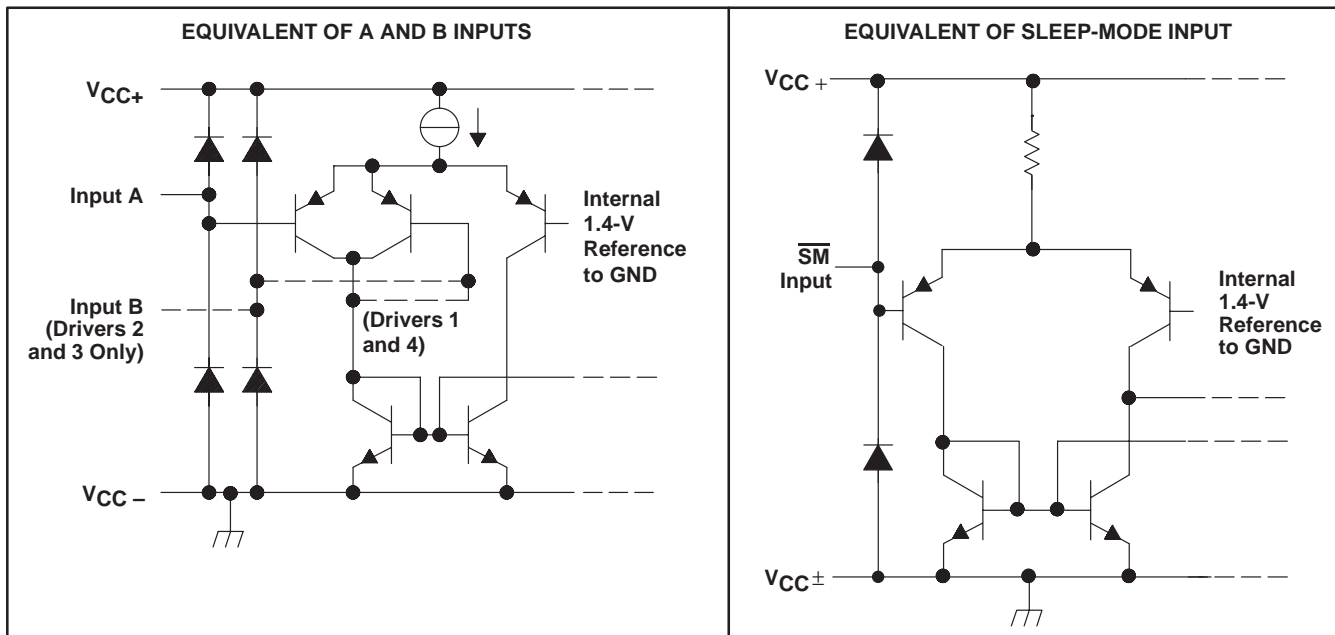


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



schematics of inputs and outputs



All resistor values shown are nominal.

# SN75C198 QUADRUPLE LOW-POWER LINE DRIVERS

SLLS051C – JULY 1990 – REVISED MARCH 1997

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, $V_{CC+}$ (see Note 1)	15 V
Supply voltage, $V_{CC-}$	-15 V
Input voltage range, $V_I$	-15 V to 15 V
Output voltage range, $V_O$	$V_{CC-} - 6\text{ V}$ to $V_{CC+} + 6\text{ V}$
Continuous total power dissipation	See Dissipation Rating Table
Operating free-air temperature range, $T_A$ : SN75C198	0°C to 70°C
Storage temperature range, $T_{stg}$	-65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltages are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING
D	950 mW	7.6 mW/°C	608 mW
N	1150 mW	9.2 mW/°C	730 mW

## recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, $V_{CC+}$	4.5	12	15	V
Supply voltage, $V_{CC-}$	-4.5	-12	-15	V
Input voltage, $V_I$ (see Figure 2)	$V_{CC-} + 2$		$V_{CC+}$	V
High-level input voltage, $V_{IH}$	2			V
Low-level input voltage, $V_{IL}$	A and B inputs		0.8	V
	SM input		0.6	
Operating free-air temperature, $T_A$	0		70	°C



# SN75C198 QUADRUPLE LOW-POWER LINE DRIVERS

SLLS051C – JULY 1990 – REVISED MARCH 1997

**electrical characteristics over recommended operating free-air temperature range,  $V_{CC\pm} = \pm 12$  V,  $\overline{SM}$  at 2 V (unless otherwise noted)**

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V <sub>OH</sub>	High-level output voltage	V <sub>IH</sub> = 0.8 V, R <sub>L</sub> = 3 kΩ	V <sub>CC±</sub> = ±5 V	4			V
			V <sub>CC±</sub> = ±12 V	10			
V <sub>OL</sub>	Low-level output voltage (see Note 2)	V <sub>IH</sub> = 2 V, R <sub>L</sub> = 3 kΩ	V <sub>CC±</sub> = ±5 V			-4	V
			V <sub>CC±</sub> = ±12 V			-10	
I <sub>IH</sub>	High-level input current	V <sub>I</sub> = 5 V				10	μA
I <sub>IL</sub>	Low-level input current	V <sub>I</sub> = 0 V				-10	μA
I <sub>OZ</sub>	High-impedance-state output current	$\overline{SM}$ at 0.6 V	V <sub>O</sub> = 12 V, V <sub>CC±</sub> = ±12 V			100	μA
			V <sub>O</sub> = -12 V, V <sub>CC±</sub> = ±12 V			-100	
I <sub>OS(H)</sub>	High-level short-circuit output current‡	V <sub>I</sub> = 0.8 V, V <sub>O</sub> = 0 or V <sub>CC-</sub>		-4.5	-10	-19.5	mA
I <sub>OS(L)</sub>	Low-level short-circuit output current‡	V <sub>I</sub> = 2 V, V <sub>O</sub> = 0 or V <sub>CC+</sub>		4.5	10	19.5	mA
r <sub>o</sub>	Output resistance	V <sub>CC±</sub> = 0, V <sub>O</sub> = -2 V to 2 V		300			Ω
I <sub>CC+</sub>	Supply current from V <sub>CC+</sub>	A and B inputs at 0.8 V or 2 V, No load	V <sub>CC±</sub> = ±5 V		90	160	μA
			V <sub>CC±</sub> = ±12 V		95	160	
		A and B inputs at 0.8 V or 2 V, R <sub>L</sub> = 3 kΩ, $\overline{SM}$ at 0.6 V	V <sub>CC±</sub> = ±5 V		40		
			V <sub>CC±</sub> = ±12 V		40		
I <sub>CC-</sub>	Supply current from V <sub>CC-</sub>	A and B inputs at 0.8 V or 2 V, No load	V <sub>CC±</sub> = ±5 V		-90	-160	μA
			V <sub>CC±</sub> = ±12 V		-95	-160	
		A and B inputs at 0.8 V or 2 V, R <sub>L</sub> = 3 kΩ, $\overline{SM}$ at 0.6 V	V <sub>CC±</sub> = ±5 V		-40		
			V <sub>CC±</sub> = ±12 V		-40		

† All typical values are at T<sub>A</sub> = 25°C.

‡ Not more than one output should be shorted at a time.

NOTE 2: The algebraic convention, where the more positive (less negative) limit is designated as maximum, is used in this data sheet for logic levels only, e.g., if -10 V is a maximum, the typical value is a more negative voltage.

**switching characteristics over recommended operating free-air temperature range,  $V_{CC\pm} = \pm 12$  V (unless otherwise noted)**

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
t <sub>PLH</sub>	Propagation delay time, low- to high-level output§	R <sub>L</sub> = 3 kΩ to 7 kΩ, C <sub>L</sub> = 15 pF, See Figure 1				3	μs
t <sub>PHL</sub>	Propagation delay time, high- to low-level output§					3.5	μs
t <sub>TLH</sub>	Transition time, low- to high-level output¶			0.53	1	3.2	μs
t <sub>THL</sub>	Transition time, high- to low-level output¶			0.53	1	3.2	μs
t <sub>TLH</sub>	Transition time, low- to high-level output#	R <sub>L</sub> = 3 kΩ to 7 kΩ, C <sub>L</sub> = 2500 pF, See Figure 2			1.5		μs
t <sub>THL</sub>	Transition time, high- to low-level output#				1.5		μs
t <sub>PZH</sub>	Output enable time to high level	R <sub>L</sub> = 3 kΩ to 7 kΩ, C <sub>L</sub> = 15 pF, See Figure 3				50	μs
t <sub>PHZ</sub>	Output disable time from high level					10	μs
t <sub>PZL</sub>	Output enable time to low level	R <sub>L</sub> = 3 kΩ to 7 kΩ, C <sub>L</sub> = 15 pF, See Figure 4				15	μs
t <sub>PLZ</sub>	Output disable time from low level					10	μs
SR	Output slew rate#	R <sub>L</sub> = 3 kΩ to 7 kΩ, C <sub>L</sub> = 15 pF	6	15	30		V/μs

† All typical values are at T<sub>A</sub> = 25°C.

§ t<sub>PHL</sub> and t<sub>PLH</sub> include the additional time due to on-chip slew rate and are measured at the 50% points.

¶ Measured between 10% and 90% points of output waveform

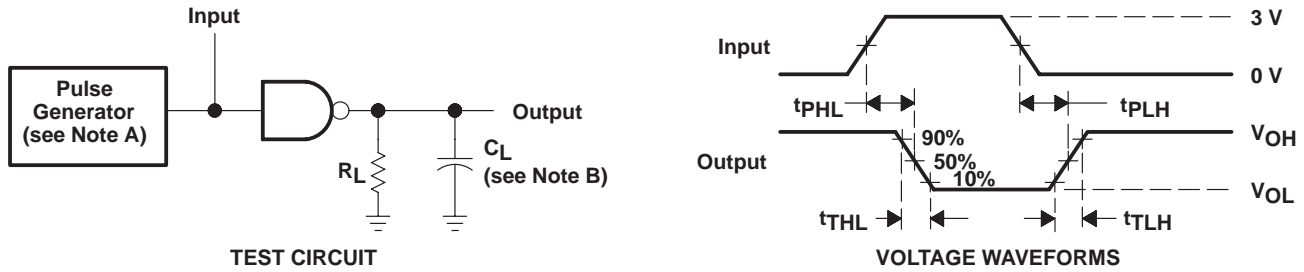
# Measured between 3-V and -3-V points of output waveform



# SN75C198 QUADRUPLE LOW-POWER LINE DRIVERS

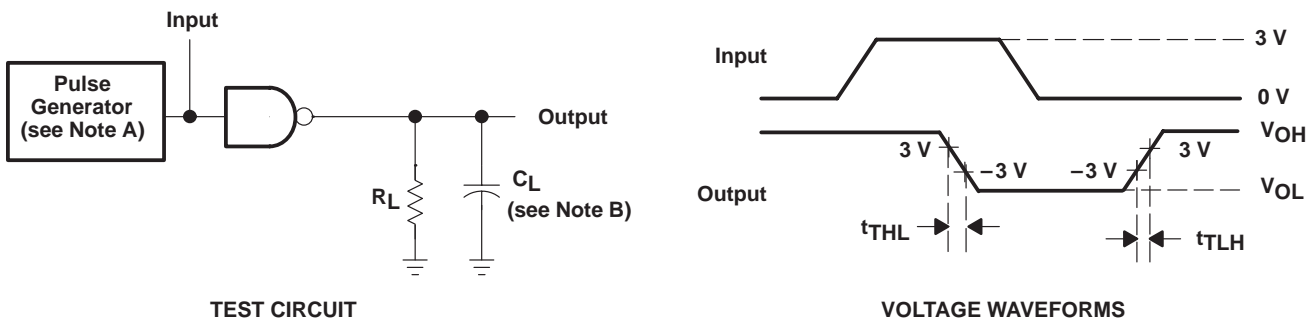
SLLS051C – JULY 1990 – REVISED MARCH 1997

## PARAMETER MEASUREMENT INFORMATION



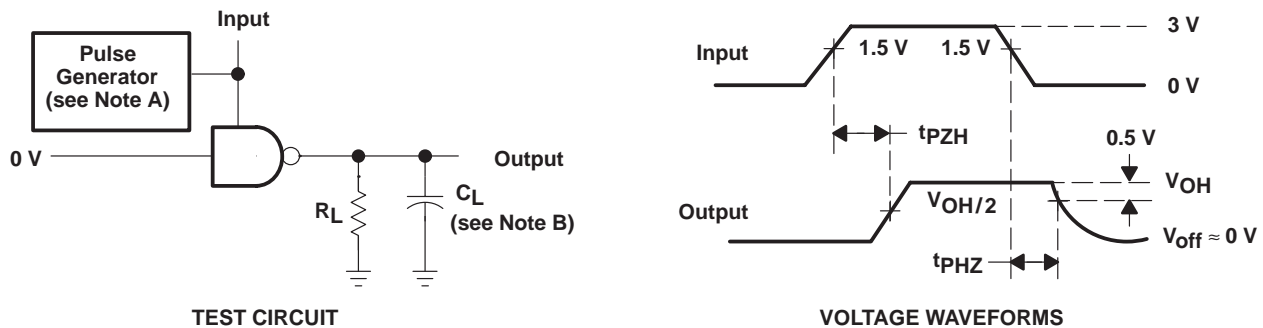
NOTES: A. The pulse generator has the following characteristics:  $t_w = 25 \mu s$ , PRR = 20 kHz,  $Z_O = 50 \Omega$ ,  $t_r = t_f \leq 50$  ns.  
B.  $C_L$  includes probe and jig capacitance.

**Figure 1. Test Circuit and Voltage Waveforms, Propagation and Transition Times**



NOTES: A. The pulse generator has the following characteristics:  $t_w = 25 \mu s$ , PRR = 20 kHz,  $Z_O = 50 \Omega$ ,  $t_r = t_f \leq 50$  ns.  
B.  $C_L$  includes probe and jig capacitance.

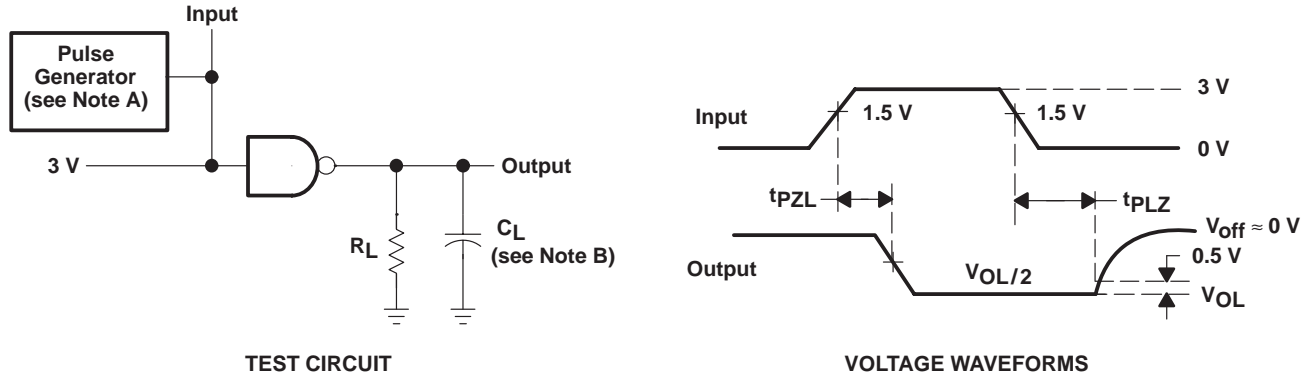
**Figure 2. Test Circuit and Voltage Waveforms, Transition Times**



NOTES: A. The pulse generator has the following characteristics:  $t_w = 25 \mu s$ , PRR = 20 kHz,  $Z_O = 50 \Omega$ ,  $t_r = t_f \leq 50$  ns.  
B.  $C_L$  includes probe and jig capacitance.

**Figure 3. Driver Test Circuit and Voltage Waveforms**

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. The pulse generator has the following characteristics:  $t_W = 25 \mu s$ ,  $PRR = 20 \text{ kHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = t_f \leq 50 \text{ ns}$ .  
 B.  $C_L$  includes probe and jig capacitance.

Figure 4. Driver Test Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

VOLTAGE TRANSFER CHARACTERISTICS

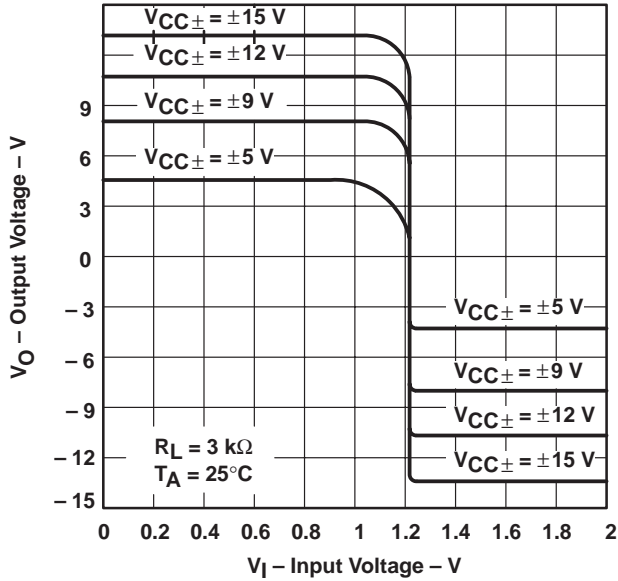


Figure 5

OUTPUT CURRENT vs OUTPUT VOLTAGE

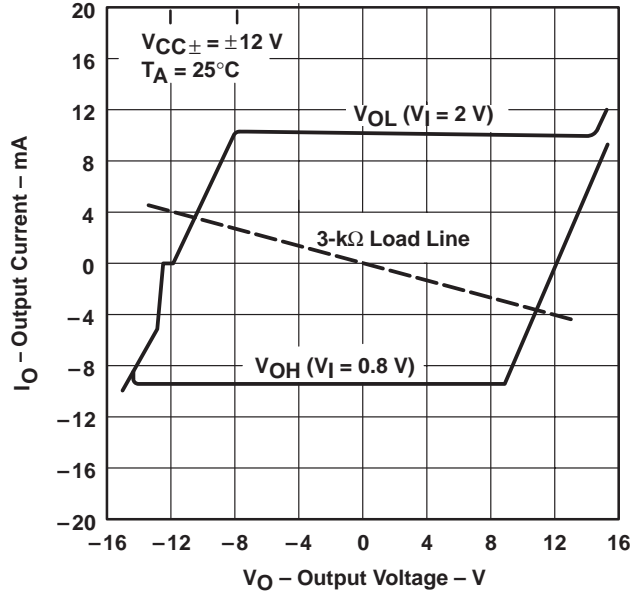


Figure 6

SHORT-CIRCUIT OUTPUT CURRENT vs FREE-AIR TEMPERATURE

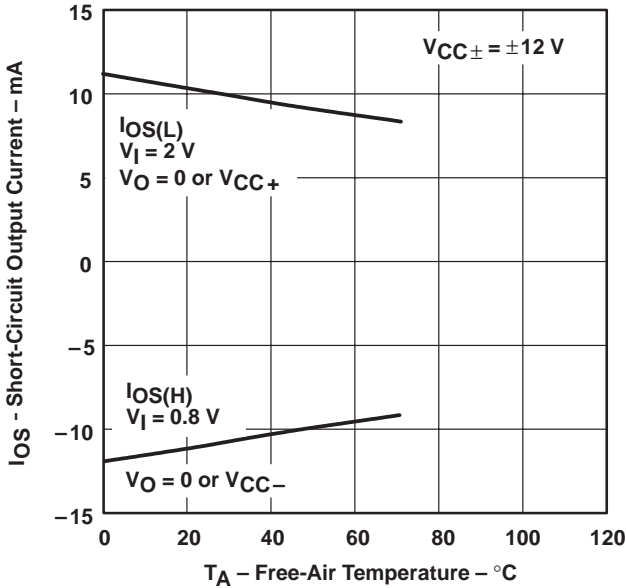


Figure 7

OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

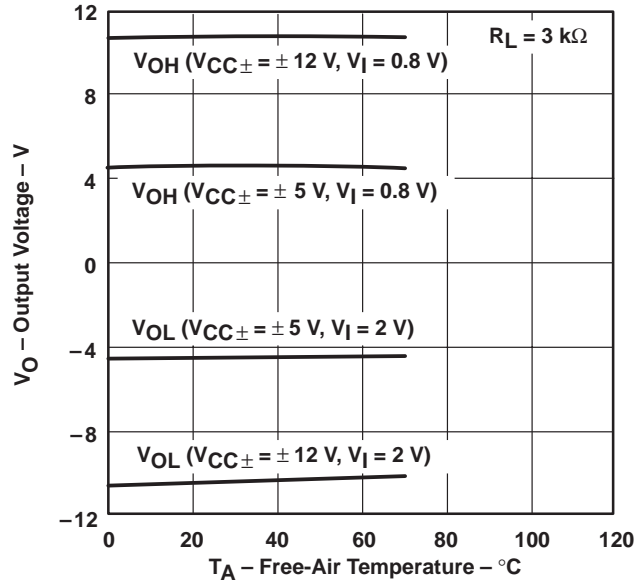
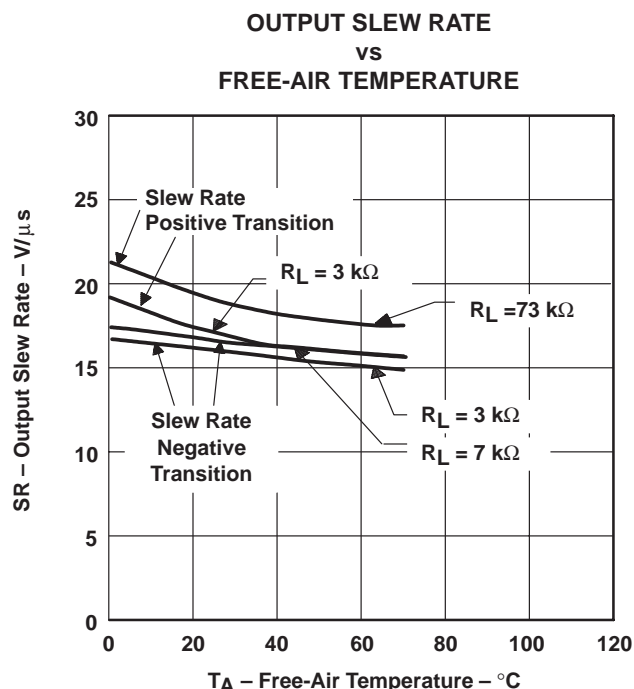
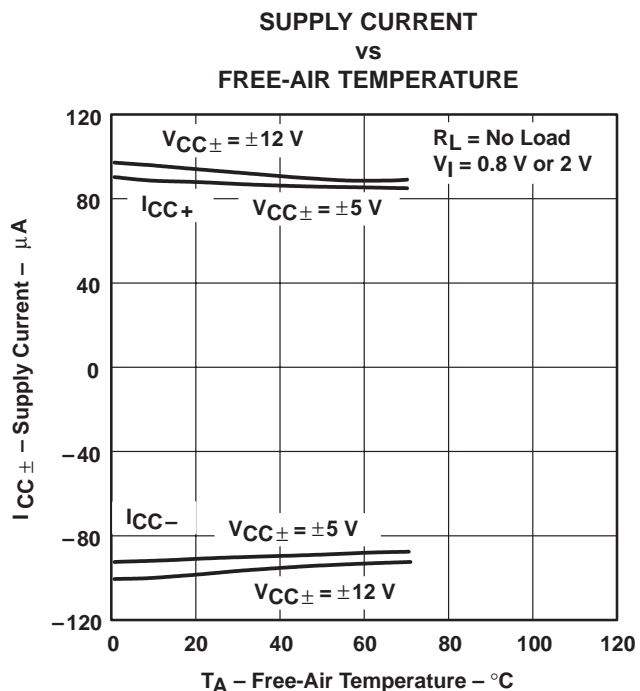
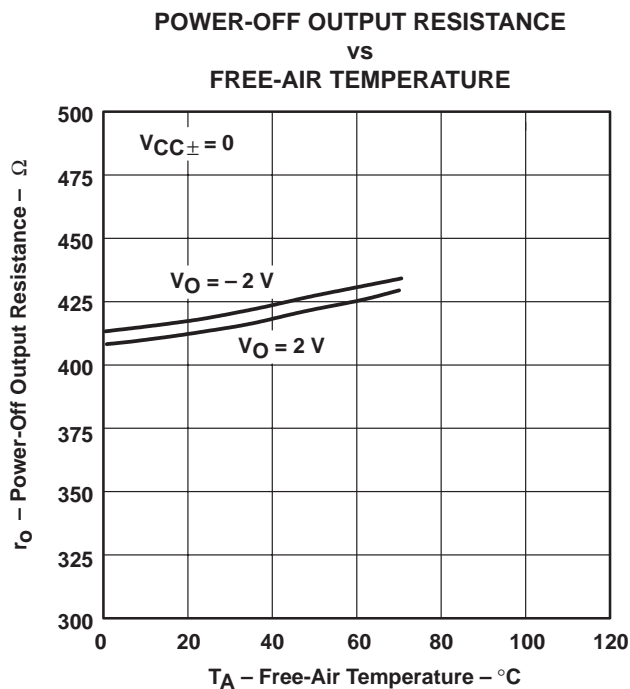
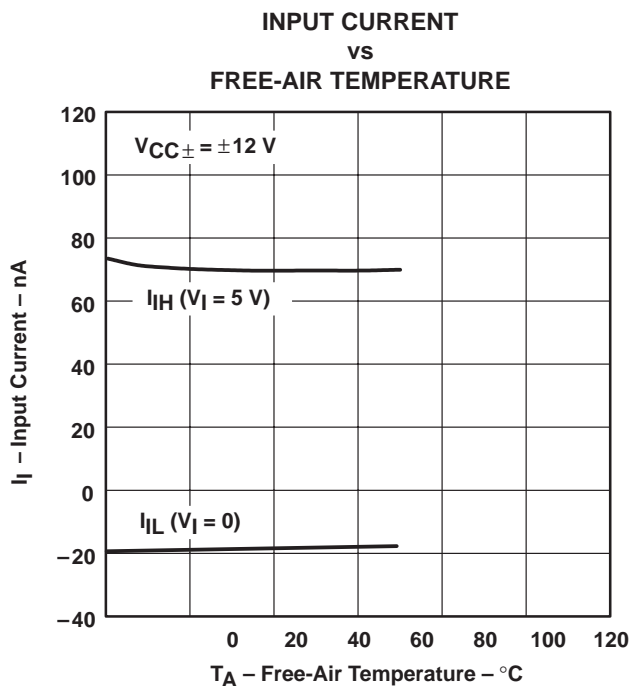


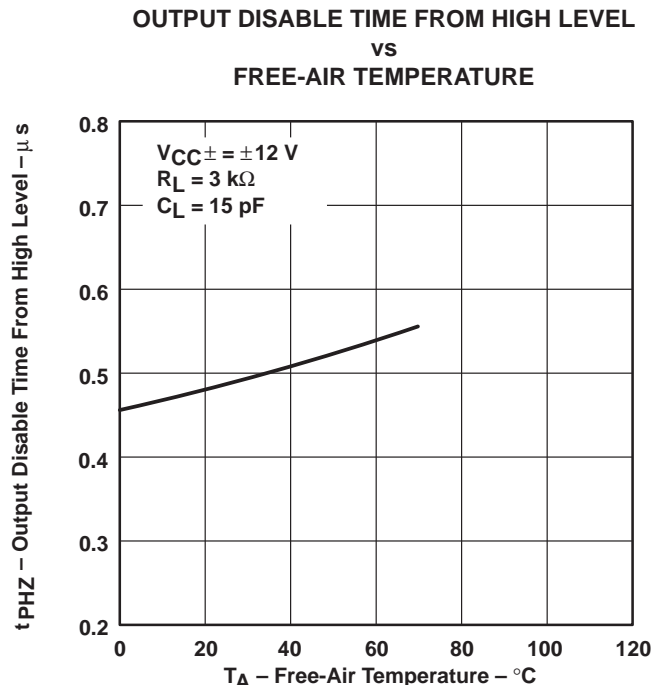
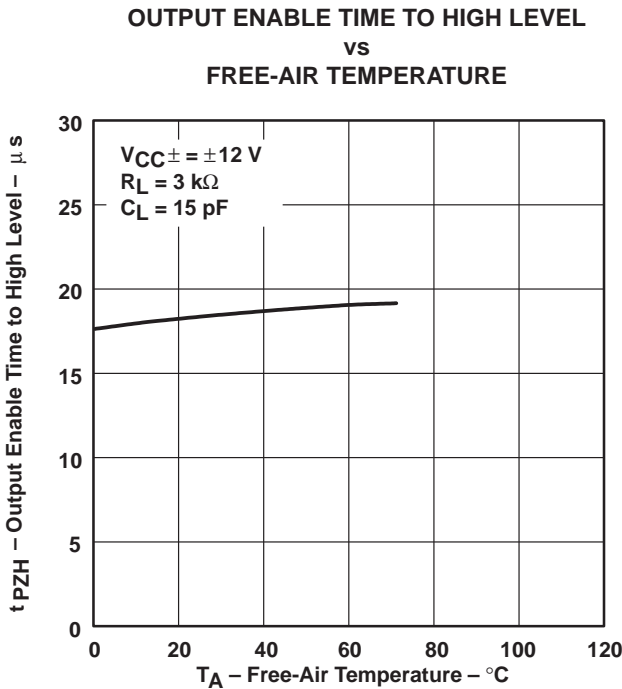
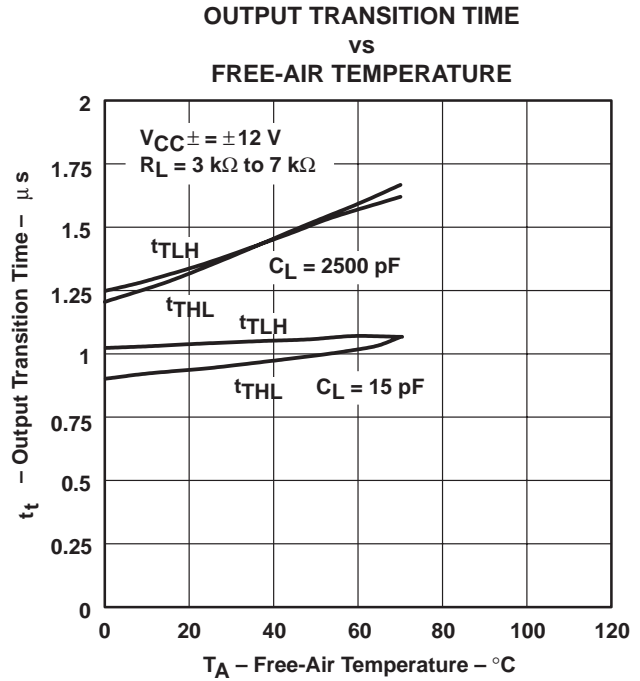
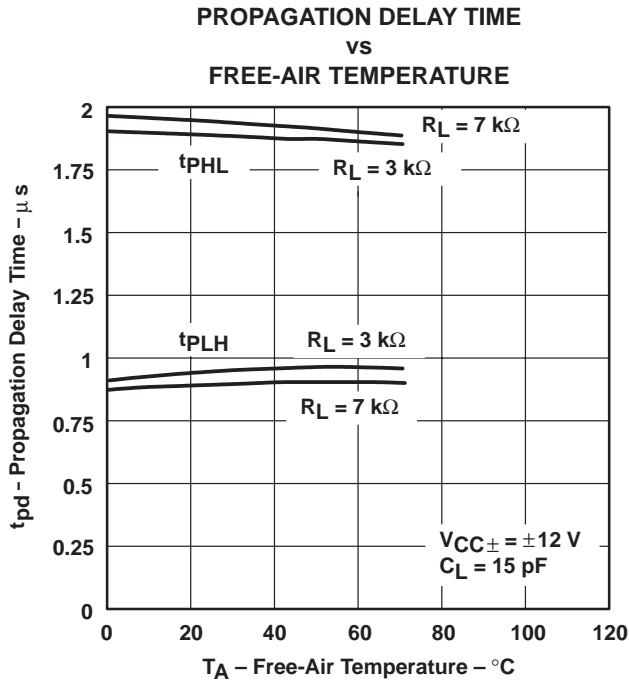
Figure 8



TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS

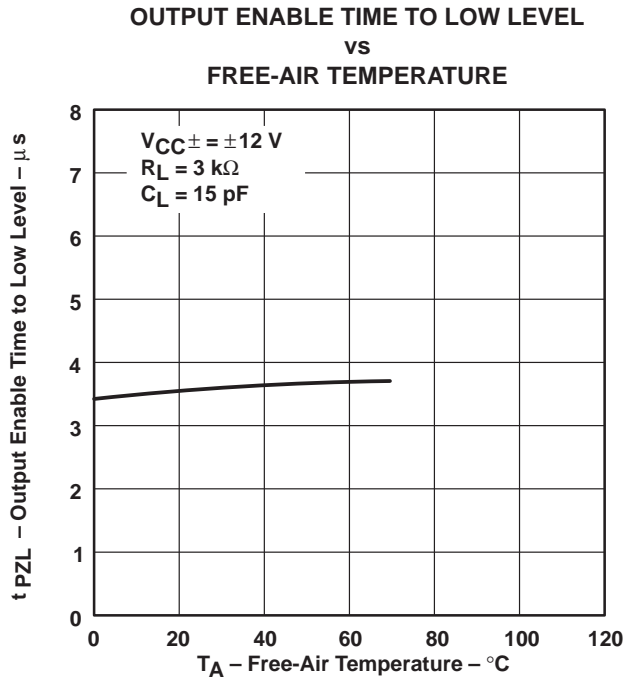


Figure 17

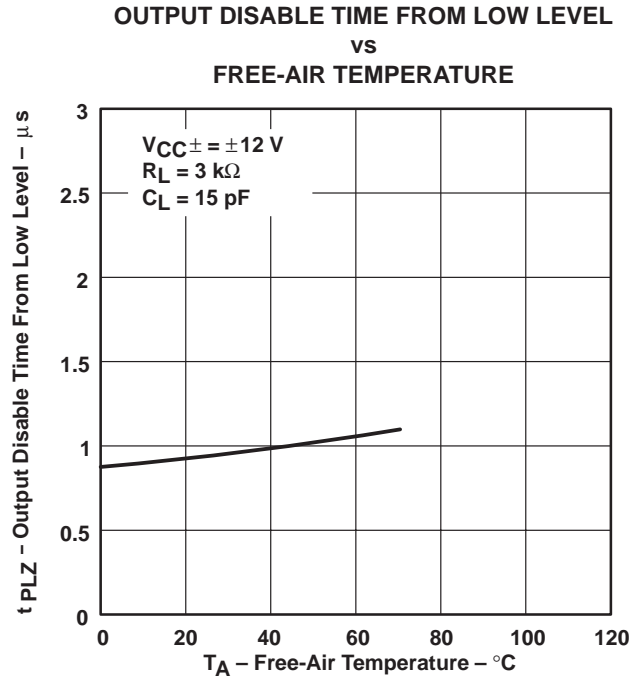


Figure 18

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75C198D	NRND	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75C198	
SN75C198N	NRND	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN75C198N	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN75C198D	D	SOIC	14	50	506.6	8	3940	4.32
SN75C198N	N	PDIP	14	25	506	13.97	11230	4.32

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040047-5/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



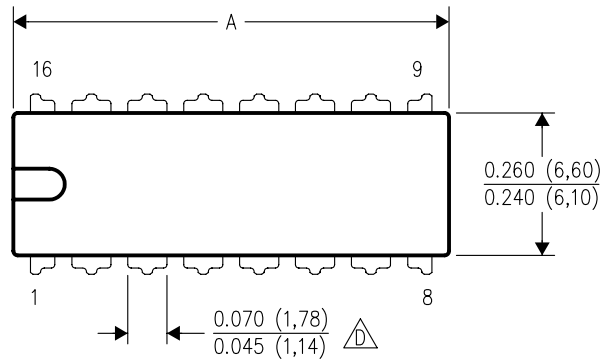
4211283-3/E 08/12

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

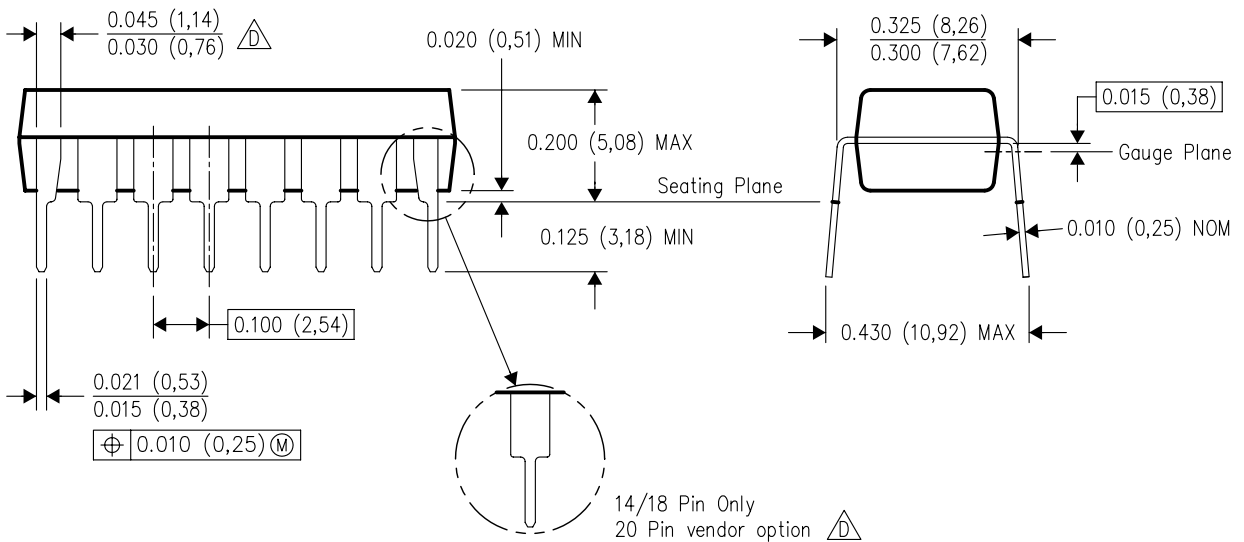
N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



DIM	PINS **			
	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - $\triangle D$  The 20 pin end lead shoulder width is a vendor option, either half or full width.



## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2023, Texas Instruments Incorporated