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N-Channel UltraFET Power MOSFET
55 V, 20 A, 26 mΩ

These N-Channel power MOSFETs are manufactured using the innovative UltraFET process. This advanced process technology achieves the lowest possible on-resistance per silicon area, resulting in outstanding performance. This device is capable of withstanding high energy in the avalanche mode and the diode exhibits very low reverse recovery time and stored charge. It was designed for use in applications where power efficiency is important, such as switching regulators, switching converters, motor drivers, relay drivers, low-voltage bus switches, and power management in portable and battery-operated products.

Formerly developmental type TA75329.

Features

- 20A, 55V

- Simulation Models
  - Temperature Compensated PSPICE® and SABER™ Models
  - SPICE and SABER Thermal Impedance Models Available on the WEB at: www.onsemi.com

- Peak Current vs Pulse Width Curve

- UIS Rating Curve

- Related Literature
  - TB334, "Guidelines for Soldering Surface Mount Components to PC Boards"

Ordering Information

PART NUMBER	PACKAGE	BRAND
HUF75329D3ST	TO-252AA	75329D

Symbol
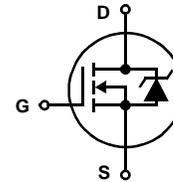
Packaging

JEDEC TO-252AA

Absolute Maximum Ratings T_C = 25°C, Unless Otherwise Specified

		UNITS
Drain to Source Voltage (Note 1) . . . . V$_{DSS}$	55	V
Drain to Gate Voltage (R$_{GS}$ = 20kΩ) (Note 1) . . . . V$_{DGR}$	55	V
Gate to Source Voltage . . . . V$_{GS}$	±20	V
Drain Current		
Continuous (Figure 2). . . . . I$_D$	20	A
Pulsed Drain Current . . . . I$_{DM}$	Figure 4	
Pulsed Avalanche Rating. . . . . E$_{AS}$	Figure 6	
Power Dissipation . . . . P$_D$	128	W
Derate Above 25°C	0.86	W/^{o}C
Operating and Storage Temperature . . . . T$_J$, T$_{STG}$	-55 to 175	^{o}C
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s. . . . . T$_L$	300	^{o}C
Package Body for 10s, See Techbrief 334 . . . . T$_{pkg}$	260	^{o}C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. T$_J$ = 25°C to 150°C.

Electrical Specifications T_C = 25°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
OFF STATE SPECIFICATIONS							
Drain to Source Breakdown Voltage	BV$_{DSS}$	I$_D$ = 250µA, V$_{GS}$ = 0V (Figure 11)		55	-	-	V
Zero Gate Voltage Drain Current	I$_{DSS}$	V$_{DS}$ = 50V, V$_{GS}$ = 0V		-	-	1	µA
		V$_{DS}$ = 45V, V$_{GS}$ = 0V, T$_C$ = 150°C		-	-	250	µA
Gate to Source Leakage Current	I$_{GSS}$	V$_{GS}$ = ±20V		-	-	±100	nA
ON STATE SPECIFICATIONS							
Gate to Source Threshold Voltage	V$_{GS(TH)}$	V$_{GS}$ = V$_{DS}$, I$_D$ = 250µA (Figure 10)		2	-	4	V
Drain to Source On Resistance	r$_{DS(ON)}$	I$_D$ = 20A, V$_{GS}$ = 10V (Figure 9)		-	0.022	0.026	Ω
THERMAL SPECIFICATIONS							
Thermal Resistance Junction to Case	R$_{\theta JC}$	(Figure 3)		-	-	1.17	^{o}C/W
Thermal Resistance Junction to Ambient	R$_{\theta JA}$	TO-252		-	-	100	^{o}C/W
SWITCHING SPECIFICATIONS (V$_{GS}$ = 10V)							
Turn-On Time	t$_{ON}$	V$_{DD}$ = 30V, I$_D \cong$ 20A, R$_L$ = 1.5Ω, V$_{GS}$ = 10V, R$_{GS}$ = 9.1Ω		-	-	60	ns
Turn-On Delay Time	t$_{d(ON)}$			-	7	-	ns
Rise Time	t$_r$			-	30	-	ns
Turn-Off Delay Time	t$_{d(OFF)}$			-	10	-	ns
Fall Time	t$_f$			-	33	-	ns
Turn-Off Time	t$_{OFF}$			-	-	65	ns
GATE CHARGE SPECIFICATIONS							
Total Gate Charge	Q$_{g(TOT)}$	V$_{GS}$ = 0V to 20V	V$_{DD}$ = 30V, I$_D \cong$ 20A, R$_L$ = 1.5Ω I$_{g(REF)}$ = 1.0mA (Figure 13)	-	50	65	nC
Gate Charge at 10V	Q$_{g(10)}$	V$_{GS}$ = 0V to 10V		-	32	40	nC
Threshold Gate Charge	Q$_{g(TH)}$	V$_{GS}$ = 0V to 2V		-	2.0	2.5	nC
Gate to Source Gate Charge	Q$_{gs}$			-	5	-	nC
Reverse Transfer Capacitance	Q$_{gd}$			-	13	-	nC

Electrical Specifications T_C = 25°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
CAPACITANCE SPECIFICATIONS						
Input Capacitance	C_{ISS}	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz (Figure 12)	-	1060	-	pF
Output Capacitance	C_{OSS}		-	405	-	pF
Reverse Transfer Capacitance	C_{RSS}		-	95	-	pF

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	I_{SD} = 20A	-	-	1.25	V
Reverse Recovery Time	t_{rr}	I_{SD} = 20A, dI_{SD}/dt = 100A/μs	-	-	68	ns
Reverse Recovered Charge	Q_{RR}	I_{SD} = 20A, dI_{SD}/dt = 100A/μs	-	-	120	nC

Typical Performance Curves
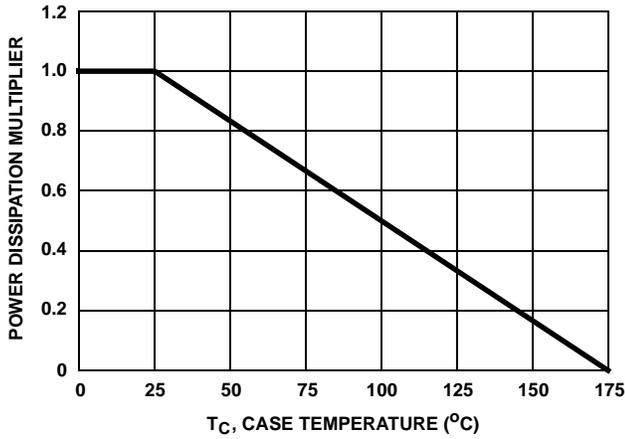
FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE
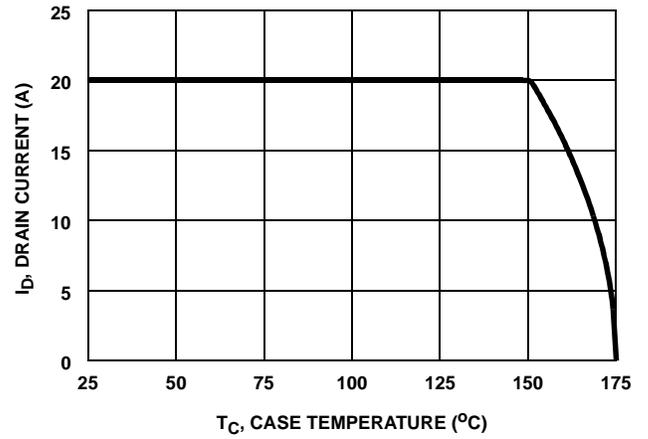
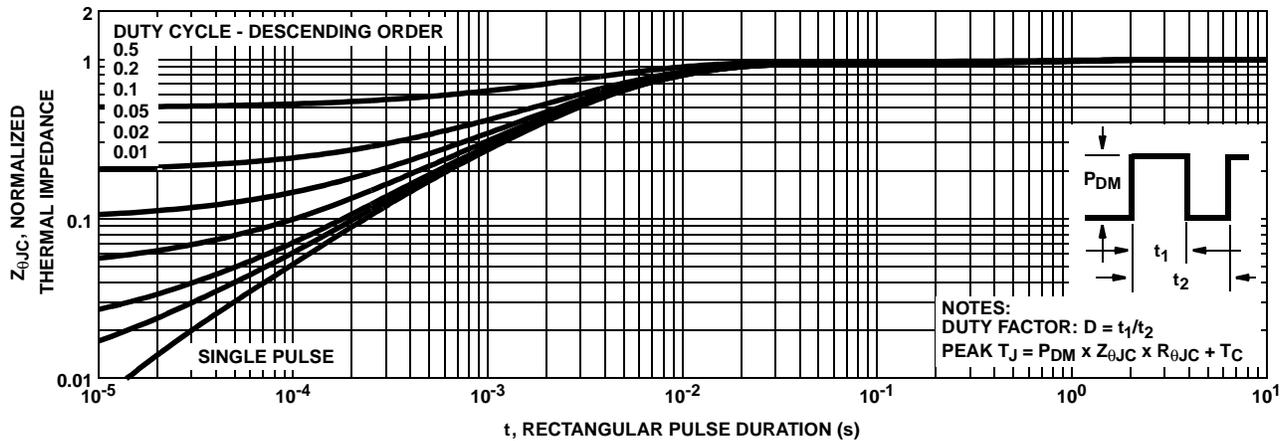FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

NOTES:
DUTY FACTOR: D = t_1/t_2
PEAK T_J = P_{DM} x $Z_{\theta JC}$ x $R_{\theta JC}$ + T_C

FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

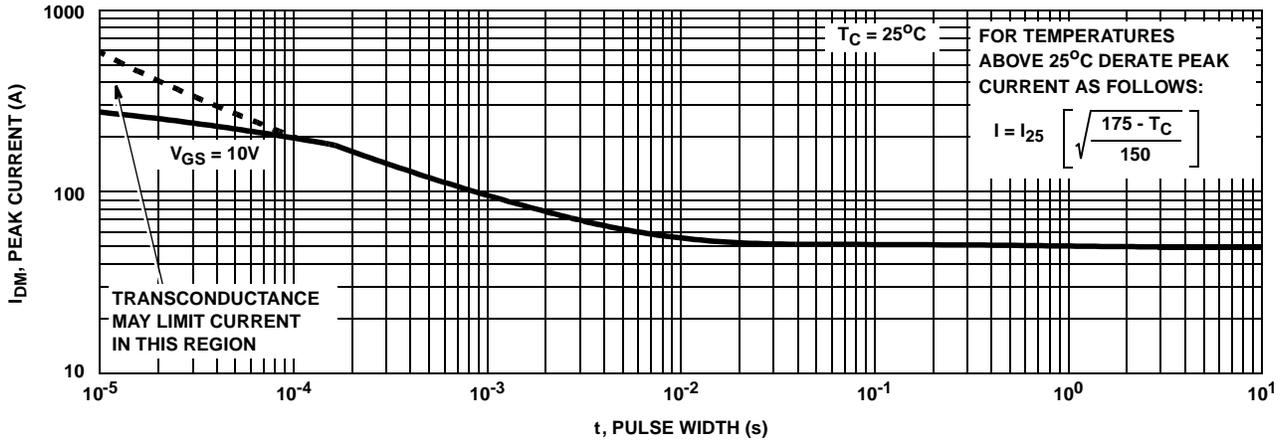## *Typical Performance Curves* (Continued)

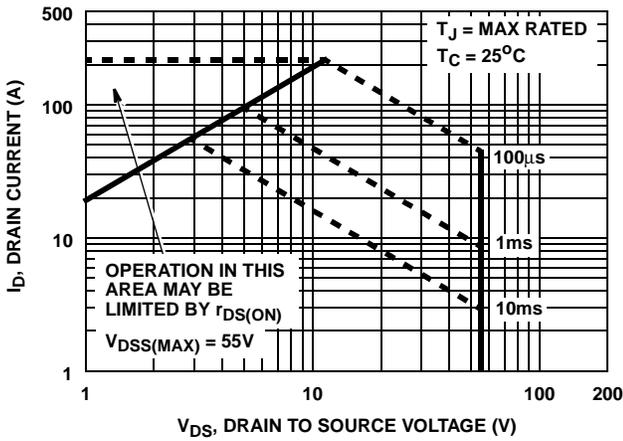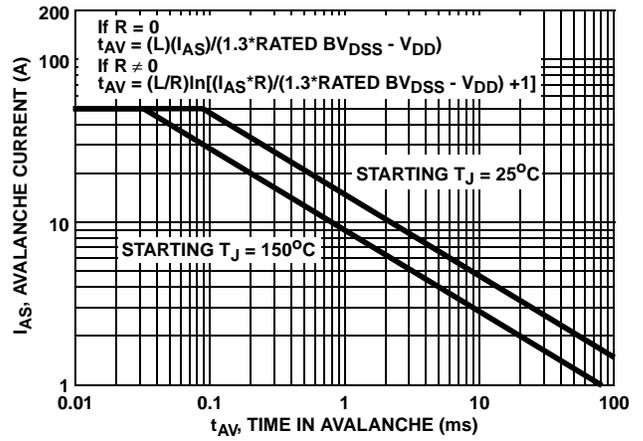**FIGURE 4. PEAK CURRENT CAPABILITY**

FIGURE 5. FORWARD BIAS SAFE OPERATING AREA

NOTE: Refer to ON Semiconductor Application Notes AN9321 and AN9322.

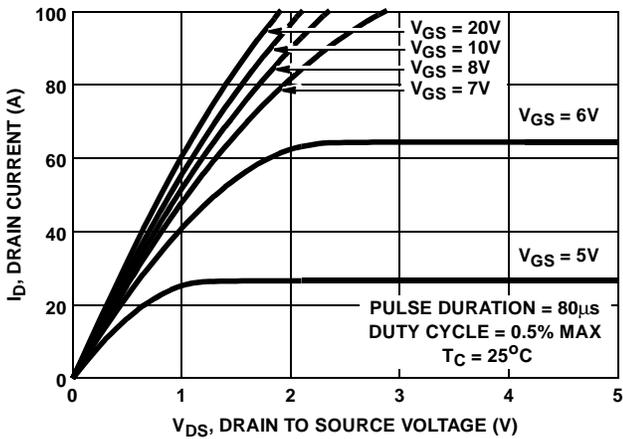**FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY**
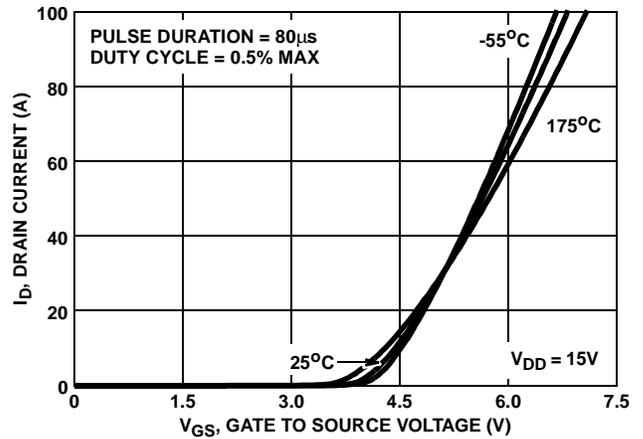

FIGURE 7. SATURATION CHARACTERISTICS

FIGURE 8. TRANSFER CHARACTERISTICS
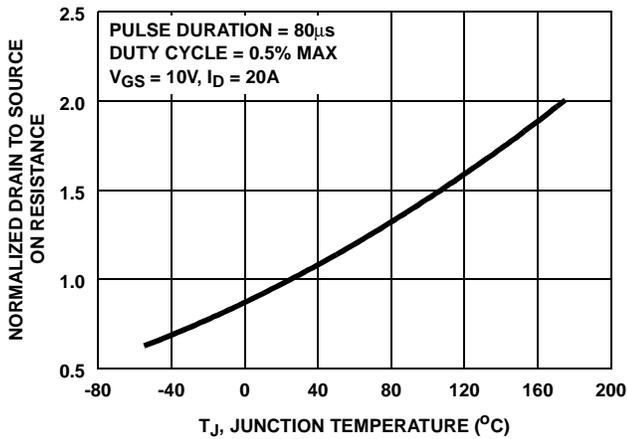
Typical Performance Curves (Continued)

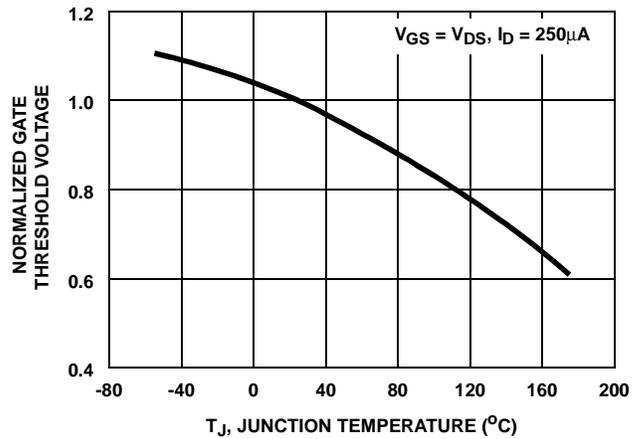FIGURE 9. NORMALIZED DRAIN TO SOURCE ON
RESISTANCE vs JUNCTION TEMPERATURE

FIGURE 10. NORMALIZED GATE THRESHOLD VOLTAGE vs
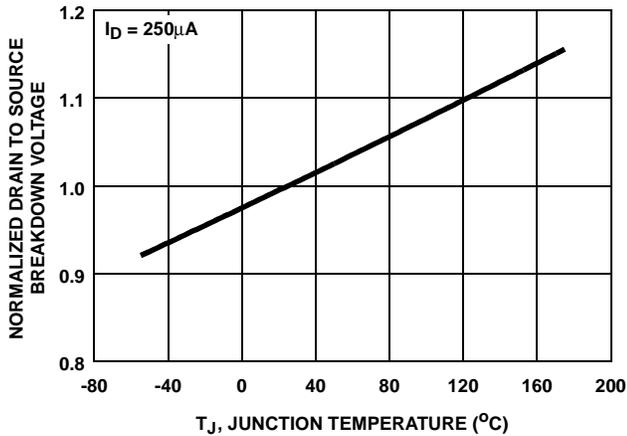JUNCTION TEMPERATURE

FIGURE 11. NORMALIZED DRAIN TO SOURCE BREAKDOWN
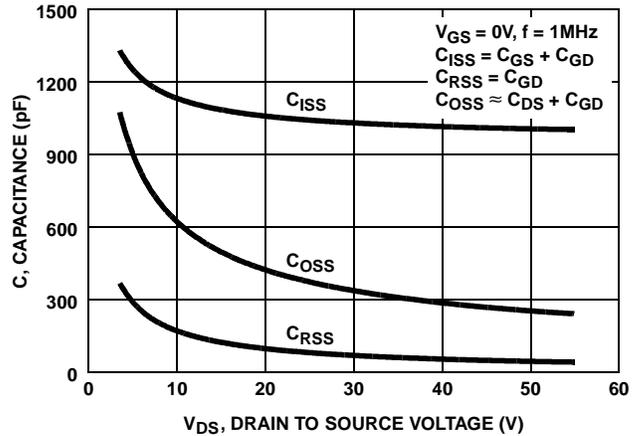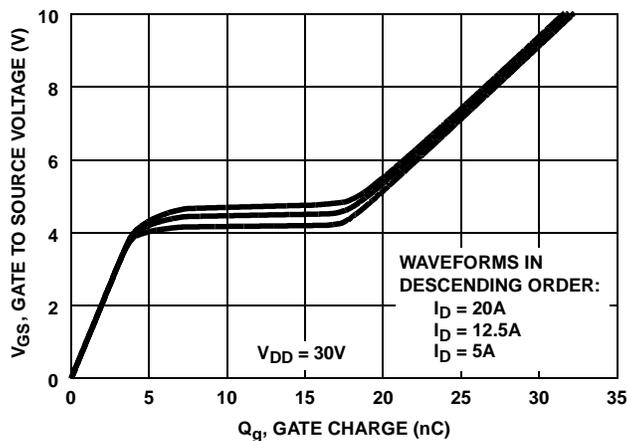VOLTAGE vs JUNCTION TEMPERATURE

FIGURE 12. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

NOTE: Refer to ON Semiconductor Application Notes AN7254 and AN7260.

FIGURE 13. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

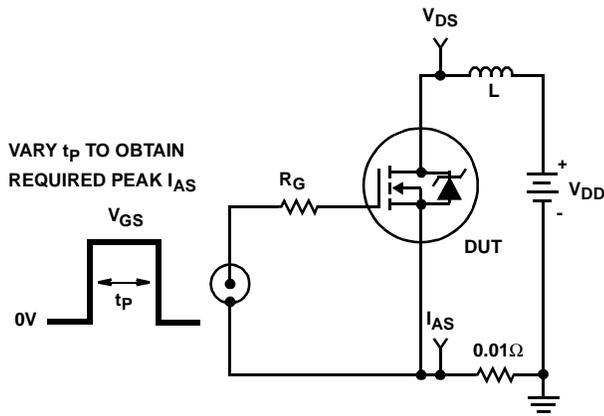## *Test Circuits and Waveforms*

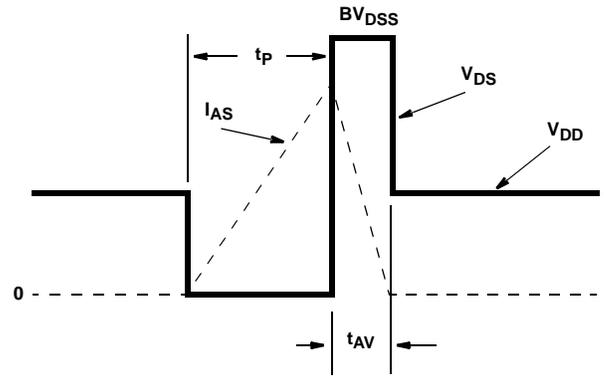FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

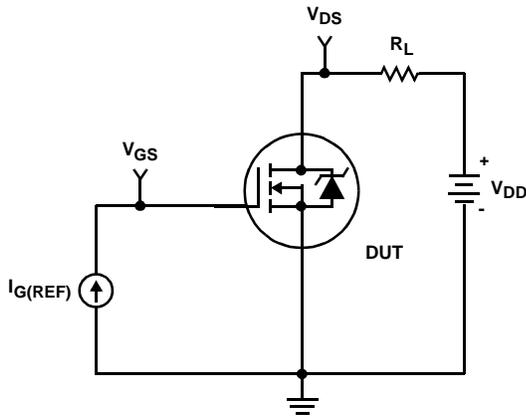FIGURE 15. UNCLAMPED ENERGY WAVEFORMS
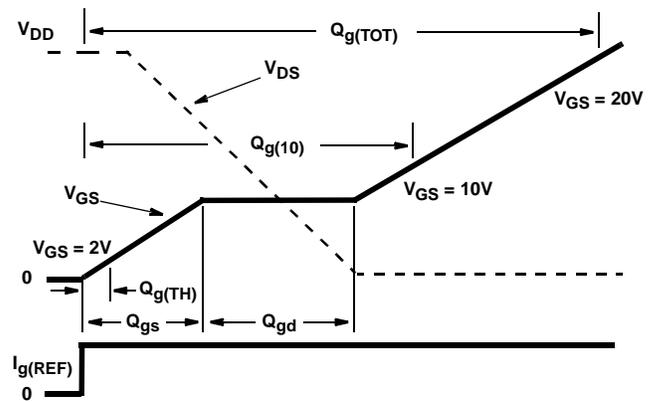

FIGURE 16. GATE CHARGE TEST CIRCUIT

FIGURE 17. GATE CHARGE WAVEFORM
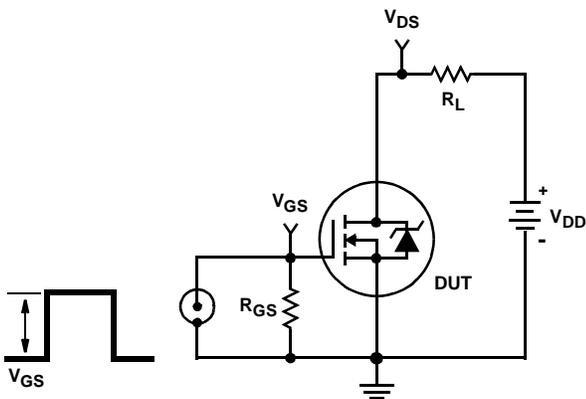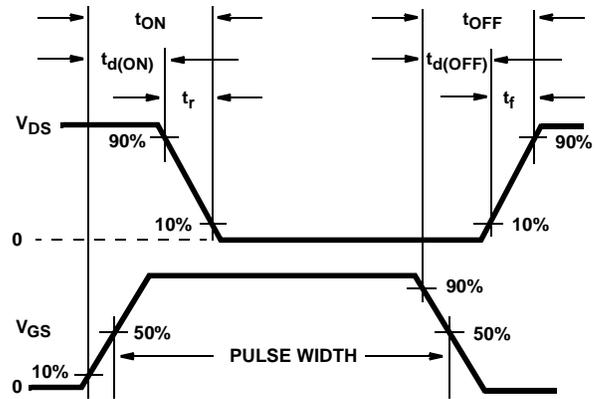

FIGURE 18. SWITCHING TIME TEST CIRCUIT

FIGURE 19. RESISTIVE SWITCHING WAVEFORMS

PSPICE Electrical Model

.SUBCKT HUF75329D 2 1 3 ;   rev 6/19/97

CA 12 8 1.72e-9
CB 15 14 1.52e-9
CIN 6 8 9.61e-10

DBODY 7 5 DBODYMOD
DBREAK 5 11 DBREAKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 58.13
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTHRES 6 21 19 8 1
EVTEMP 20 6 18 22 1

IT 8 17 1

LDRAIN 2 5 1e-9
LGATE 1 9 2.86e-9
LSOURCE 3 7 2.69e-9

MMED 16 6 8 8 MMEDMOD
MSTRO 16 6 8 8 MSTROMOD
MWEAK 16 21 8 8 MWEAKMOD

RBREAK 17 18 RBREAKMOD 1
RDRAIN 50 16 RDRAINMOD 1e-3
RGATE 9 20 1.52
RLDRAIN 2 5 10
RLGATE 1 9 26.9
RLSOURCE 3 7 28.6
RSLC1 5 51 RSLCMOD 1e-6
RSLC2 5 50 1e3
RSOURCE 8 7 RSOURCEMOD 13.85e-3
RVTHRES 22 8 RVTHRESMOD 1
RVTEMP 18 19 RVTEMPMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 22 19 DC 1

ESLC 51 50 VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*135),3.5))}

.MODEL DBODYMOD D (IS = 7.50e-13 RS = 5.05e-3 TRS1 = 2.21e-3 TRS2 = 1.02e-6 CJO = 1.51e-9 TT = 4.05e-8 M = 0.5)
.MODEL DBREAKMOD D (RS = 2.14e- 1TRS1 = 9.62e- 4TRS2 = 1.23e-6)
.MODEL DPLCAPMOD D (CJO = 13.5e-1 0IS = 1e-3 0N = 10 M = 0.85)
.MODEL MMEDMOD NMOS (VTO = 3.25 KP = 2.50 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 1.52)
.MODEL MSTROMOD NMOS (VTO = 3.80 KP = 70.0 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL MWEAKMOD NMOS (VTO = 2.91 KP = 0.06 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 15.2 RS = 0.1)
.MODEL RBREAKMOD RES (TC1 = 1.05e- 3TC2 = 1.94e-7)
.MODEL RDRAINMOD RES (TC1 = 8.04e-2 TC2 = 1.37e-4)
.MODEL RSLCMOD RES (TC1 = 4.83e-3 TC2 = 1.16e-6)
.MODEL RSOURCEMOD RES (TC1 = 0 TC2 = 0)
.MODEL RVTHRESMOD RES (TC = -3.43e-3 TC2 = -1.63e-5)
.MODEL RVTEMPMOD RES (TC1 = -1.35e- 3TC2 = 1.16e-6)

.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -7.90 VOFF= -4.90)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -4.90 VOFF= -7.90)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -0.50 VOFF= 2.50)
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 2.50 VOFF= -0.50)

.ENDS

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.
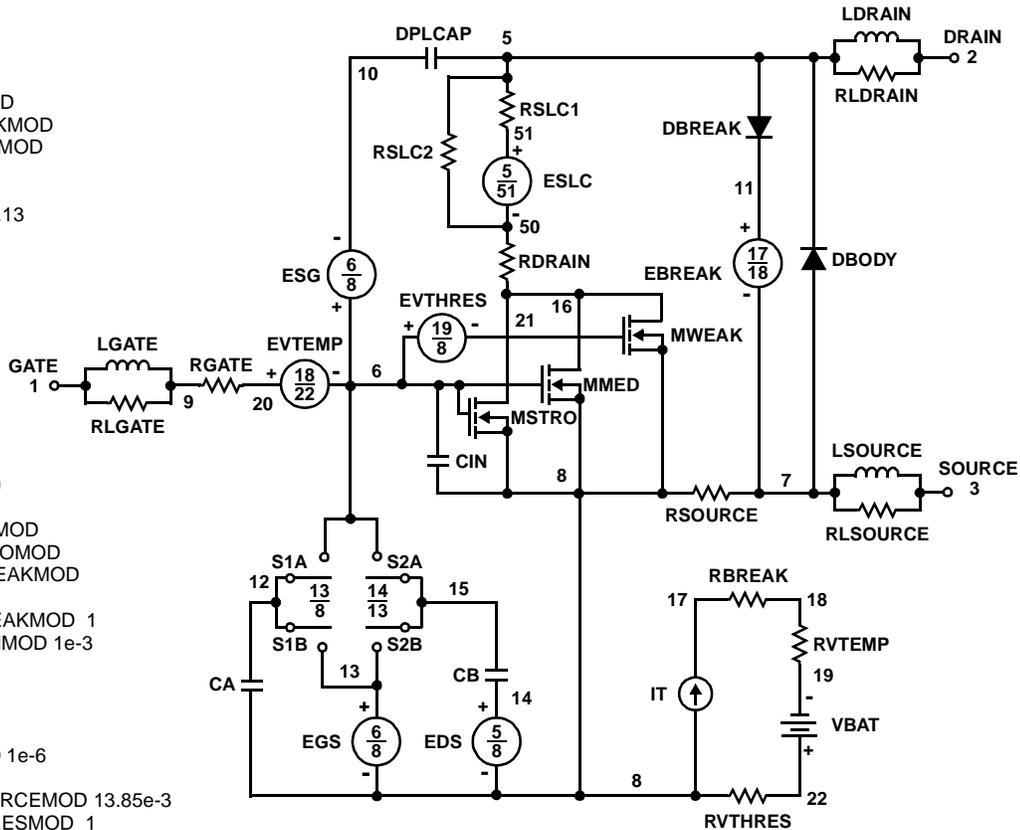
SABER Electrical Model

REV June 1997

```
template huf75329d n2, n1, n3
electrical n2, n1, n3
{
var i iscl
d..model dbodymod =  (is = 7.50e-13, cjo = 1.51e-9, tt = 4.05e-8, m = 0.5)
d..model dbreakmod = ()
d..model dplcapmod =  (cjo = 13.5e-10, is = 1e-30, n = 10, m = 0.85)
m..model mmedmod = (type=_n, vto = 3.25, kp = 2.50, is = 1e-30, tox = 1)
m..model mstrongmod = (type=_n, vto = 3.80, kp = 70, is = 1e-30, tox = 1)
m..model mweakmod = (type=_n, vto = 2.91, kp = 0.06, is = 1e-30, tox = 1)
sw_vcsp..model s1amod =  (ron = 1e-5, roff = 0.1, von = -7.90, voff = -4.90)
sw_vcsp..model s1bmod =  (ron = 1e-5, roff = 0.1, von = -4.90, voff = -7.90)
sw_vcsp..model s2amod =  (ron = 1e-5, roff = 0.1, von = -0.50, voff = 2.50)
sw_vcsp..model s2bmod =  (ron = 1e-5, roff = 0.1, von = 2.50, voff = -0.50)

c.ca n12 n8 = 1.72e-9
c.cb n15 n14 = 1.52e-9
c.cin n6 n8 = 9.61e-10

d.dbody n7 n71 = model=dbodymod
d.dbreak n72 n11 = model=dbreakmod
d.dplcap n10 n5 = model=dplcapmod

i.it n8 n17 = 1

l.ldrain n2 n5 = 1e-9
l.gate n1 n9 = 2.86e-9
l.lsource n3 n7 = 2.69e-9
k.k1 i(l.lgate) i(l.lsource) = l(l.lgate), l(l.lsource), 0.0085

m.mmed n16 n6 n8 n8 = model=mmedmod, l = 1u, w = 1u
m.mstrong n16 n6 n8 n8 = model=mstrongmod, l = 1u, w = 1u
m.mweak n16 n21 n8 n8 = model=mweakmod, l = 1u, w = 1u

res.rbreak n17 n18  = 1, tc1 = 1.05e-3, tc2 = 1.94e-7
res.rdbody n71 n5 = 5.05e-3, tc1 = 2.21e-3, tc2 = 1.02e-6
res.rdbreak n72 n5 = 2.14e-1, tc1 = 9.62e-4, tc2 = 1.23e-6
res.rdrain n50 n16 = 1e-3, tc1 = 8.04e-2, tc2 = 1.37e-4
res.rgate n9 n20 = 1.52
res.rldrain n2 n5 = 10
res.rlgate n1 n9 = 26.9
res.rlsource n3 n7 = 28.6
res.rslc1 n5 n51  = 1e-6, tc1 = 4.83e-3, tc2 = 1.16e-6
res.rslc2 n5 n50 = 1e3
res.rsource n8 n7  = 13.85e-3, tc1 = 0, tc2 = 0
res.rvtemp n18 n19  = 1, tc1 = -1.35e-3, tc2 = 1.16e-6
res.rvthres n22 n8  = 1, tc1 = -3.43e-3, tc2 = -1.63e-5

spe.ebreak n11 n7 n17 n18 = 58.13
spe.eds n14 n8 n5 n8 = 1
spe.egs n13 n8 n6 n8 = 1
spe.esg n6 n10 n6 n8 = 1
spe.evtemp n20 n6 n18 n22 = 1
spe.evthres n6 n21 n19 n8 = 1

sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod
sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod
sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod
sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod

v.vbat n22 n19 = dc = 1

equations {
i (n51->n50) + = iscl
iscl: v(n51,n50) = ((v(n5,n51)/(1e-9+abs(v(n5,n51))))*((abs(v(n5,n51)*1e6/135))** 3.5))
}
}
```
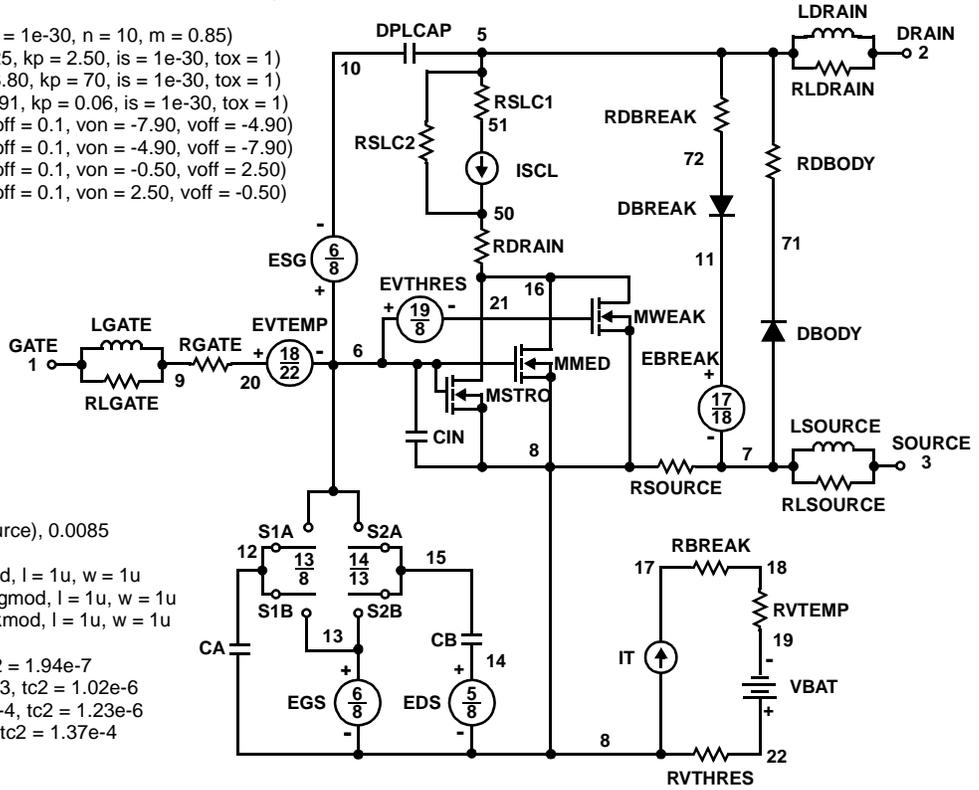
SPICE Thermal Model

REV 23 February 1999

HUF75329D

CTHERM1 th 6 2.80e-3
CTHERM2 6 5 1.00e-2
CTHERM3 5 4 6.80e-3
CTHERM4 4 3 7.00e-3
CTHERM5 3 2 1.60e-2
CTHERM6 2 tl 15.55

RTHERM1 th 6 7.94e-3
RTHERM2 6 5 1.98e-2
RTHERM3 5 4 5.57e-2
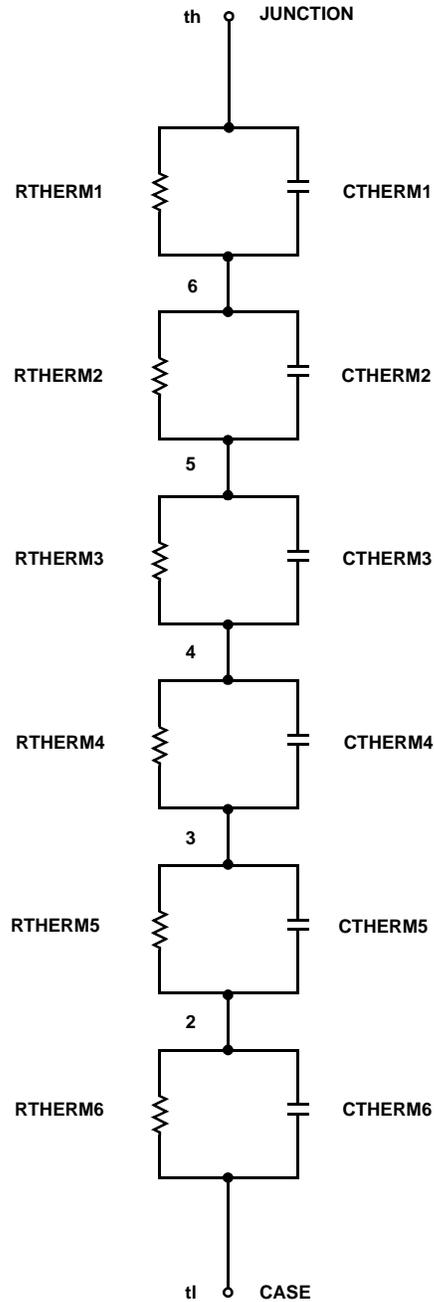RTHERM4 4 3 3.13e-1
RTHERM5 3 2 4.71e-1
RTHERM6 2 tl 6.26e-2

SABER Thermal Model

SABER thermal model HUF75329D

template thermal_model th tl
thermal_c th, tl
{
ctherm.ctherm1 th 6 = 2.80e-3
ctherm.ctherm2 6 5 = 1.00e-2
ctherm.ctherm3 5 4 = 6.80e-3
ctherm.ctherm4 4 3 = 7.00e-3
ctherm.ctherm5 3 2 = 1.60e-2
ctherm.ctherm6 2 tl = 15.55

rtherm.rtherm1 th 6 = 7.94e-3
rtherm.rtherm2 6 5 = 1.98e-2
rtherm.rtherm3 5 4 = 5.57e-2
rtherm.rtherm4 4 3 = 3.13e-1
rtherm.rtherm5 3 2 = 4.71e-1
rtherm.rtherm6 2 tl = 6.26e-2
}

th ○ JUNCTION

RTHERM1   CTHERM1

6

RTHERM2   CTHERM2

5

RTHERM3   CTHERM3

4

RTHERM4   CTHERM4

3

RTHERM5   CTHERM5

2

RTHERM6   CTHERM6

tl ○ CASE

PUBLICATION ORDERING INFORMATION

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