



12 V P-Channel 1.8 V (G-S) MOSFET

PRODUCT SUMMARY					
V _{DS} (V)	$R_{DS(on)}(\Omega)$	I _D (A)			
	0.055 at V _{GS} = - 4.5 V	- 4.9			
- 12	0.070 at V _{GS} = - 2.5 V	- 4.4			
	0.090 at V _{GS} = - 1.8 V	- 4			

FEATURES

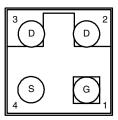
- TrenchFET® Power MOSFET
- MICRO FOOT® Chipscale Packaging Reduces Footprint Area Profile (0.62 mm) and On-Resistance Per Footprint Area

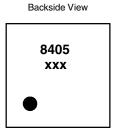


Material categorization: For definitions of compliance please see www.vishav.com/doc?99912

MICRO FOOT







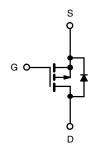
Device Marking: 8405

xxx = Date/Lot Traceability Code

Ordering Information: Si8405DB-T1-E1 (Lead (Pb)-free and Halogen-free)

APPLICATIONS

- · PA, Battery and Load Switch
- Battery Charger Switch



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T _A = 25 °C, unless otherwise noted)						
Parameter		Symbol	5 s	Steady State	Unit	
Drain-Source Voltage		V _{DS}	- 12		V	
Gate-Source Voltage		V _{GS}	± 8		\ \ \ \	
Continuous Dusin Comment /T 150 °C\d	T _A = 25 °C	- I _D	- 4.9	- 3.6		
Continuous Drain Current (T _J = 150 °C) ^a	T _A = 70 °C		- 3.9	- 2.8		
Pulsed Drain Current		I _{DM}	- 10		Α	
Continuous Source Current (Diode Conduction) ^a		I _S	- 2.5	- 1.3		
Mariana Barra Biratinali	T _A = 25 °C	P _D	2.77	1.47	W	
Maximum Power Dissipation ^a	T _A = 70 °C	TD	1.77	0.94	VV	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150		°C	
Package Reflow Conditions ^b	IR/Convection		260			

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Manipular lungtion to Aughient	t ≤ 5 s	R_{thJA}	35	45	
Maximum Junction-to-Ambient ^a	Steady State	' 'thJA	72 85	°C/W	
Maximum Junction-to-Foot (drain)	Steady State	R_{thJF}	16	20	

Notes:

- a. Surface mounted on 1" x 1" FR4 board.
- b. Refer to IPC/JEDEC (J-STD-020), no manual or hand soldering.
- c. In this document, any reference to case represents the body of the MICRO FOOT device and foot is the bump.

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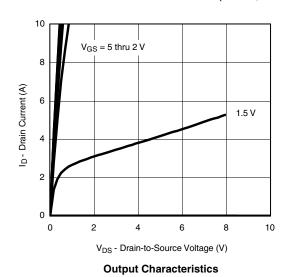
SPECIFICATIONS (T _J = 25 °C, unless otherwise noted)							
Parameter	Symbol	Test Conditions Min.		Тур.	Max.	Unit	
Static							
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -250 \mu A$	- 0.45	- 0.7	- 0.95	٧	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 8 \text{ V}$			± 100	nA	
Zero Gate Voltage Drain Current		$V_{DS} = -12 \text{ V}, V_{GS} = 0 \text{ V}$			- 1		
	I _{DSS}	$V_{DS} = -12 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 70 ^{\circ}\text{C}$			- 5	μΑ	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \le$ - 5 V, $V_{GS} =$ - 4.5 V	- 5			Α	
		V _{GS} = - 4.5 V, I _D = - 1 A		0.045	0.055		
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = - 2.5 V, I _D = - 1 A		0.055	0.070	Ω	
		V _{GS} = - 1.8 V, I _D = - 1 A		0.073	0.090		
Forward Transconductance ^a	9 _{fs}	V _{DS} = - 10 V, I _D = - 1 A		6		S	
Diode Forward Voltage ^a	V_{SD}	$I_{S} = -1 A, V_{GS} = 0 V$		- 0.73	- 1.1	V	
Dynamic ^b							
Total Gate Charge	Q_g			14	21		
Gate-Source Charge	Q_{gs}	V _{DS} = -6 V, V _{GS} = -4.5 V, I _D = -1 A		1.7		nC	
Gate-Drain Charge	Q_{gd}			2.5		1	
Turn-On Delay Time	t _{d(on)}			16	25		
Rise Time	t _r	V_{DD} = - 6 V, R_L = 6 Ω		32	50		
Turn-Off Delay Time	t _{d(off)}	$I_D\cong$ - 1 A, V_{GEN} = - 4.5 V, R_g = 6 Ω		120	180	ns	
Fall Time	t _f			80	120		
Source-Drain Reverse Recovery Time	t _{rr}	I _F = - 1 A, dI/dt = 100 A/μs		46	70		

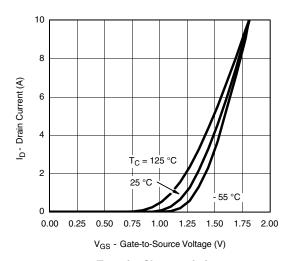
Notes:

- a. Pulse test; pulse width \leq 300 μ s, duty cycle \leq 2 %.
- b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

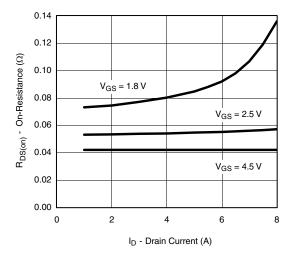




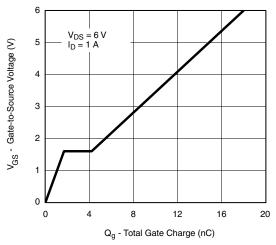
Transfer Characteristics



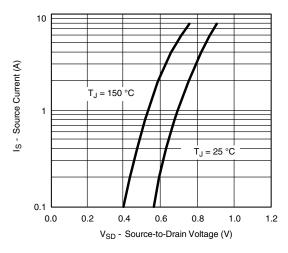
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



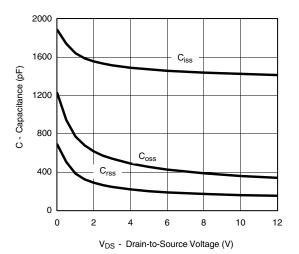
On-Resistance vs. Drain Current



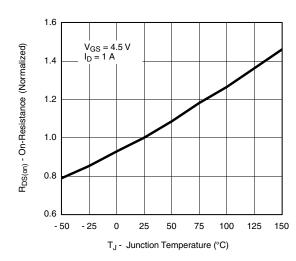
Gate Charge



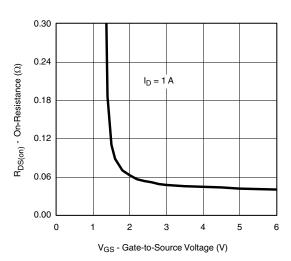
Source-Drain Diode Forward Voltage



Capacitance



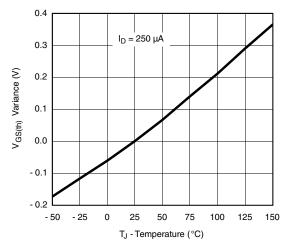
On-Resistance vs. Junction Temperature

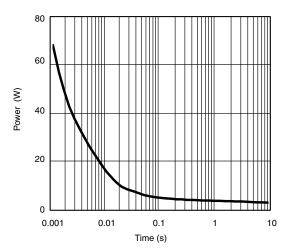


On-Resistance vs. Gate-to-Source Voltage

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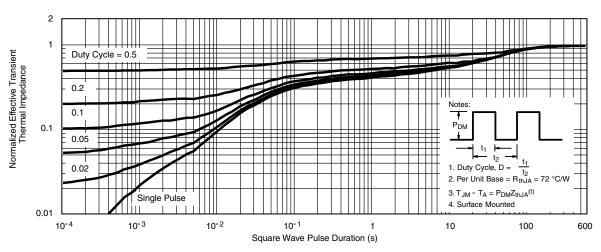
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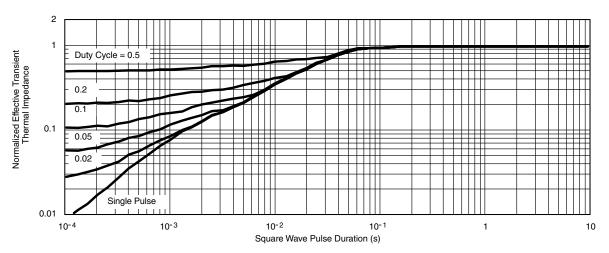


Threshold Voltage

Single Pulse Power, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Ambient

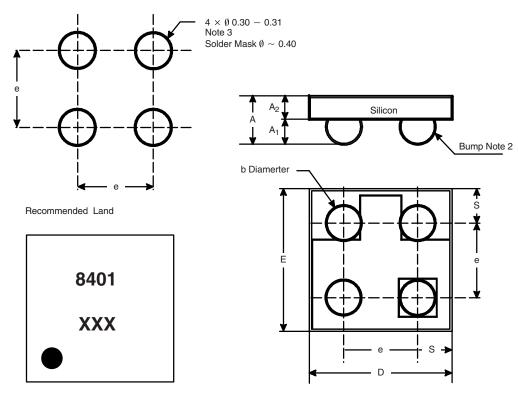


Normalized Thermal Transient Impedance, Junction-to-Foot



PACKAGE OUTLINE

MICRO FOOT: 4-BUMP (0.8 mm PITCH)



Mark on Backside of Die

Notes (unless otherwise specified):

- 1. Laser mark on the silicon die back, coated with a thin metal.
- 2. Bumps are 95.5/3.8/0.7 Sn/Ag/Cu.
- 3. Non-solder mask defined copper landing pad.
- 4. The flat side of wafers is oriented at the bottom.

Dim.	Millimeters ^a		Inches		
	Min.	Max.	Min.	Max.	
A	0.600	0.650	0.0236	0.0256	
A ₁	0.260	0.290	0.0102	0.0114	
A ₂	0.340	0.360	0.0134	0.0142	
b	0.370	0.410	0.0146	0.0161	
D	1.520	1.600	0.0598	0.0630	
E	1.520	1.600	0.0598	0.0630	
е	0.800		0.03	315	
S	0.360	0.400	0.0142	0.0157	

Notes:

a. Use millimeters as the primary measurement.

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