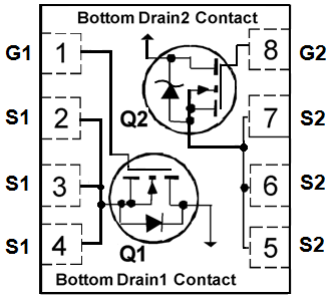
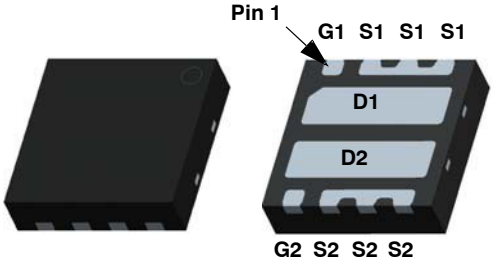
MOSFET – Dual N-Channel, POWERTRENCH®

Q1: 30 V, 12 A, 9.0 mΩ
Q2: 30 V, 16 A, 6.4 mΩ

FDMC7208S





Power 33

WDFN8 3x3, 0.65P
CASE 511DG

General Description

This device includes two 30 V N−Channel MOSFETs in a dual Power 33 (3 mm x 3 mm MLP) package. The package is enhanced for exceptional thermal performance.

Features

Q1: N−Channel

- Max $r_{DS(on)}$ = 9.0 mΩ at V_{GS} = 10 V, I_D = 12 A
- Max $r_{DS(on)}$ = 11.0 mΩ at V_{GS} = 4.5 V, I_D = 11 A

Q2: N−Channel

- Max $r_{DS(on)}$ = 6.4 mΩ at V_{GS} = 10 V, I_D = 16 A
- Max $r_{DS(on)}$ = 7.5 mΩ at V_{GS} = 4.5 V, I_D = 13.5 A
- This Device is Pb−Free and is RoHS Compliant

Applications

- Computing
- Communications
- General Purpose Point of Load
- Notebook System

MARKING DIAGRAM

$Y	= **onsemi** Logo
&Z	= Assembly Plant Code
&2	= Numeric Date Code
&K	= Lot Code
FDMC7208S	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

MOSFET MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Symbol	Rating			Value Q1	Value Q2	Unit
V_{DS}	Drain to Source Voltage			30	30	V
V_{GS}	Gate to Source Voltage (Note 4)			±20	±12	V
I_D	Drain Current	Continuous (Package limited)	T_C = 25°C	22	26	A
		Continuous	T_A = 25°C	12 (Note 1a)	16 (Note 1b)	
		Pulsed		60	80	
E_{AS}	Single Pulse Avalanche Energy (Note 3)			21	21	mJ
P_D	Power Dissipation for Single Operation		T_A = 25°C	1.9 (Note 1a)	1.9 (Note 1b)	W
			T_A = 25°C	0.8 (Note 1c)	0.8 (Note 1d)	
T_J, T_{STG}	Operating and Storage Junction Temperature Range			−55 to +150		°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Characteristic	Value Q1	Value Q2	Unit
$R_{\theta JA}$	Thermal Resistance, Junction−to−Ambient	65 (Note 1a)	65 (Note 1b)	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction−to−Ambient	155 (Note 1c)	155 (Note 1d)	

PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package	Shipping†
FDMC7208S	FDMC7208S	WDFN8 3x3, 0.65P, Power 33 (Pb−Free)	3000 units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Type	Min	Typ	Max	Unit
OFF CHARACTERISTICS							
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V I_D = 1 mA, V_{GS} = 0 V	Q1 Q2	30 30	– –	– –	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C I_D = 10 mA, referenced to 25°C	Q1 Q2	– –	27 21	– –	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V	Q1 Q2	– –	– –	1 500	μA
I_{GSS}	Gate to Source Leakage Current, Forward	V_{GS} = ±20 V, V_{DS} = 0 V V_{GS} = ±12 V, V_{DS} = 0 V	Q1 Q2	– –	– –	100 100	nA
ON CHARACTERISTICS							
$V_{GS(th)}$	Gate to Source Threshold Voltage	I_D = 250 μA, V_{GS} = 0 V I_D = 1 mA, V_{GS} = 0 V	Q1 Q2	1.2 1.2	1.7 1.6	3.0 3.0	V
$\Delta V_{GS(th)}$ / ΔT_J	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C I_D = 1 mA, referenced to 25°C	Q1 Q2	– –	–5 –3	– –	mV/°C
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 12 A V_{GS} = 4.5 V, I_D = 11 A V_{GS} = 10 V, I_D = 12 A, T_J = 125°C	Q1	– – –	6.7 8.8 9.2	9.0 11.0 12.4	mΩ
		V_{GS} = 10 V, I_D = 16 A V_{GS} = 4.5 V, I_D = 13.5 A V_{GS} = 10 V, I_D = 16 A, T_J = 125°C	Q2	– –	4.7 5.3 6.4	6.4 7.5 6.8	
g_{FS}	Forward Transconductance	V_{DD} = 5 V, I_D = 12 A V_{DD} = 5 V, I_D = 16 A	Q1 Q2	– –	53 80	– –	S
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	Q1 V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz	Q1 Q2	– –	848 1685	1130 2245	pF
C_{oss}	Output Capacitance	Q2 V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz	Q1 Q2	– –	270 432	360 575	pF
C_{rss}	Reverse Transfer Capacitance		Q1 Q2	– –	36 42	55 65	pF
R_g	Gate Resistance		Q1 Q2	0.1 0.1	1.1 1.0	2.5 2.5	Ω
SWITCHING CHARACTERISTICS							
$t_{d(on)}$	Turn–On Delay Time	Q1 V_{DD} = 15 V, I_D = 12 A, R_{GEN} = 6 Ω	Q1 Q2	– –	6 7	12 14	ns
t_r	Rise Time	Q2 V_{DD} = 15 V, I_D = 16 A, R_{GEN} = 6 Ω	Q1 Q2	– –	2 3	10 10	ns
$t_{d(off)}$	Turn–Off Delay Time		Q1 Q2	– –	16 23	29 36	ns
t_f	Fall Time		Q1 Q2	– –	2 2	10 10	ns
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to 10 V; Q1 V_{DD} = 15 V, I_D = 12 A	Q1 Q2	– –	13 26	18 36	nC
		V_{GS} = 0 V to 5 V; Q2 V_{DD} = 15 V I_D = 16 A	Q1 Q2	– –	6.7 14	9.4 20	nC
Q_{gs}	Gate to Source Charge	Q1 V_{DD} = 15 V, I_D = 12 A	Q1 Q2	– –	2.3 3.9	– –	nC
Q_{gd}	Gate to Drain “Miller” Charge	Q2 V_{DD} = 15 V I_D = 16 A	Q1 Q2	– –	1.8 2.7	– –	nC

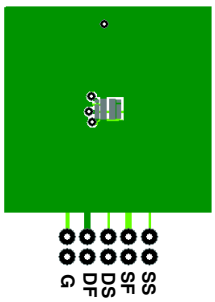
ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted) (continued)

Symbol	Parameter	Test Condition	Type	Min	Typ	Max	Unit
DRAIN−SOURCE DIODE CHARACTERISTICS							
V_{SD}	Source−Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 2 A (Note 2) V_{GS} = 0 V, I_S = 12 A (Note 2) V_{GS} = 0 V, I_S = 2 A (Note 2) V_{GS} = 0 V, I_S = 16 A (Note 2)	Q1 Q1 Q2 Q2	– – – –	0.72 0.82 0.70 0.82	1.2 1.2 1.2 1.2	V
t_{rr}	Reverse Recovery Time	Q1 I_F = 12 A, di/dt = 100 A/μs	Q1 Q2	– –	21 21	34 33	ns
Q_{rr}	Reverse Recovery Charge	Q2 I_F = 16 A, di/dt = 300 A/μs	Q1 Q2	– –	6 16	12 28	nC

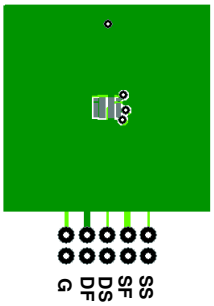
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

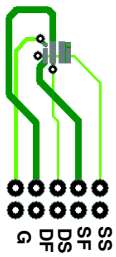
1. $R_{\theta JA}$ is determined with the device mounted on a 1in2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR−4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



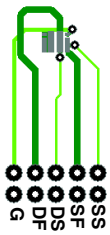
a) 65°C/W when mounted on a 1 in^2 pad of 2 oz copper



b) 65°C/W when mounted on a 1 in^2 pad of 2 oz copper.



c) 155°C/W when mounted on a minimum pad of 2 oz copper.



d) 155°C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. Q1: E_{AS} of 21 mJ is based on starting T_J = 25°C, L = 0.3 mH, I_{AS} = 12 A, V_{DD} = 27 V, V_{GS} = 10 V. 100% test at L = 3 mH, I_{AS} = 5.2 A.
   Q2: E_{AS} of 21 mJ is based on starting T_J = 25°C, L = 0.3 mH, I_{AS} = 12 A, V_{DD} = 27 V, V_{GS} = 10 V. 100% test at L = 3 mH, I_{AS} = 5.4 A.
4. As an N−ch device, the negative V_{GS} rating is for low duty cycle pulse occurrence only. No continuous rating is implied.

TYPICAL CHARACTERISTICS (Q1 N−CHANNEL)

(T_J = 25°C unless otherwise noted)

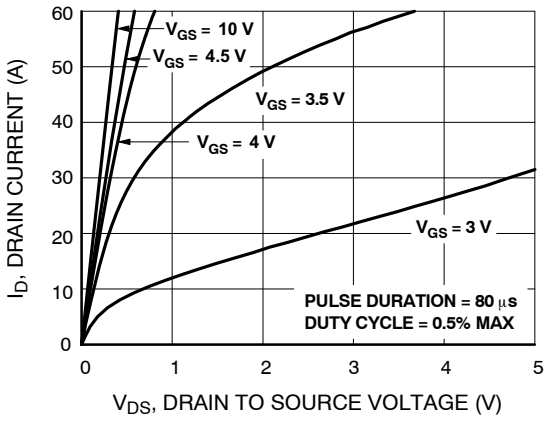


Figure 1. On−Region Characteristics

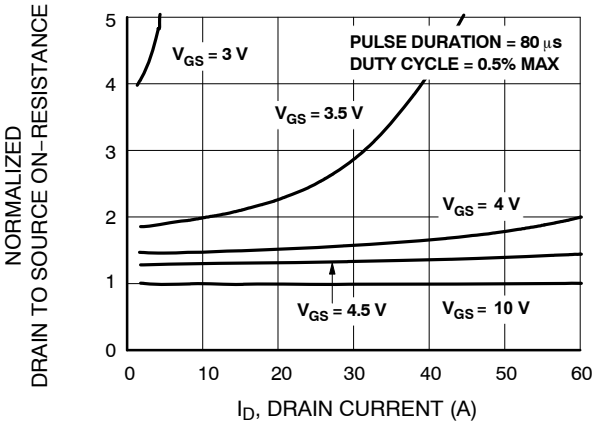


Figure 2. Normalized On−Resistance vs Drain Current and Gate Voltage

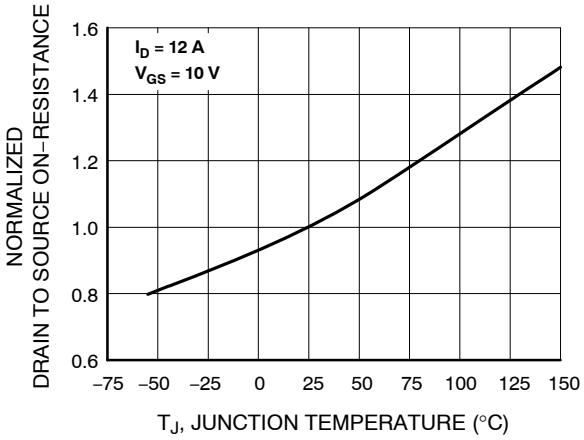


Figure 3. Normalized On−Resistance vs Junction Temperature

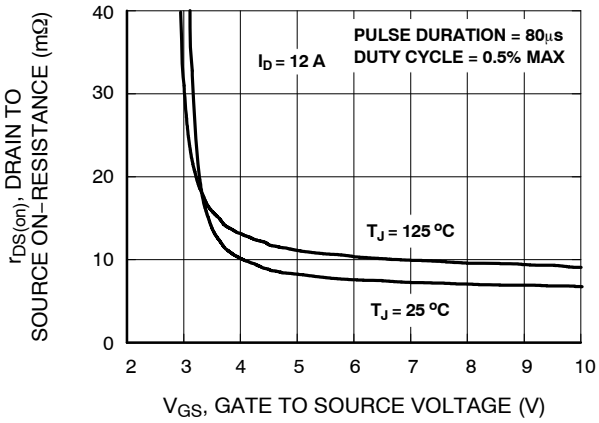


Figure 4. On−Resistance vs Gate to Source Voltage

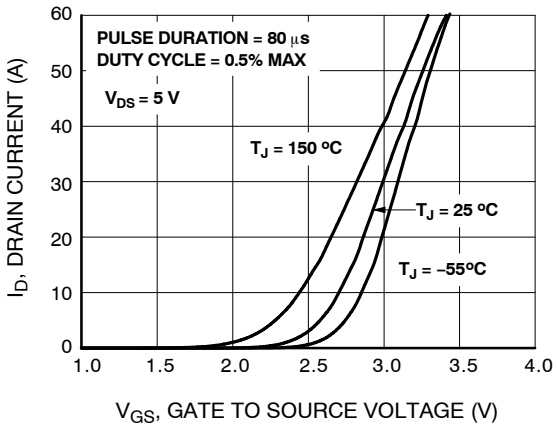


Figure 5. Transfer Characteristics

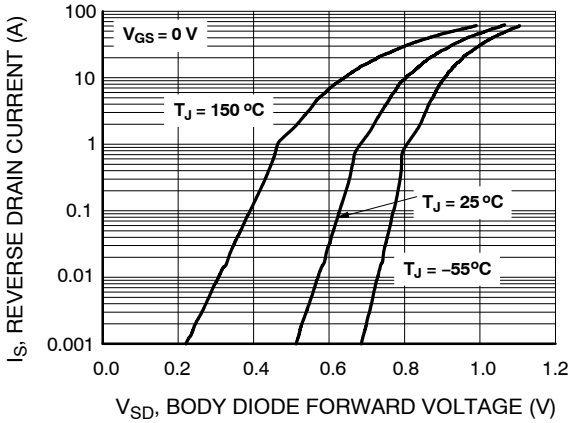


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

TYPICAL CHARACTERISTICS (Q1 N−CHANNEL) (continued)

(T_J = 25°C unless otherwise noted)

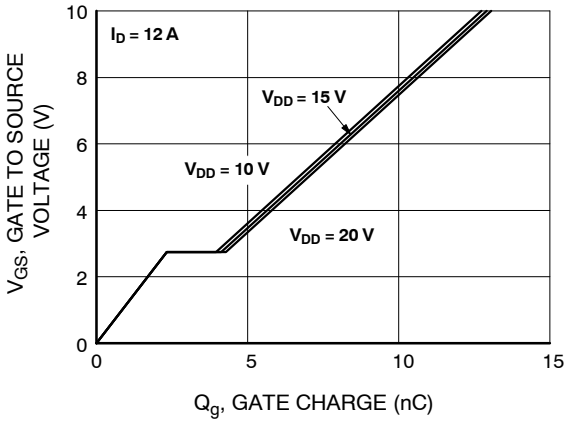


Figure 7. Gate Charge Characteristics

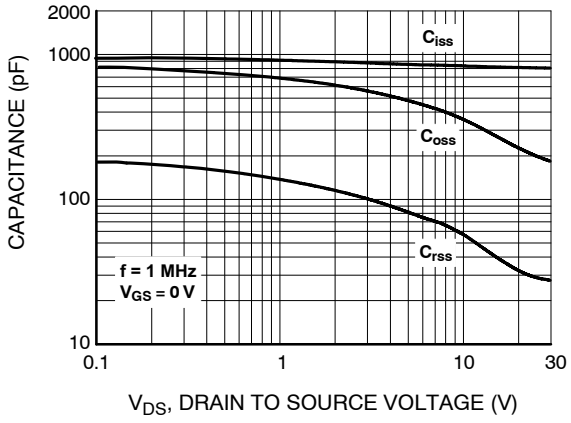


Figure 8. Capacitance vs Drain to Source Voltage

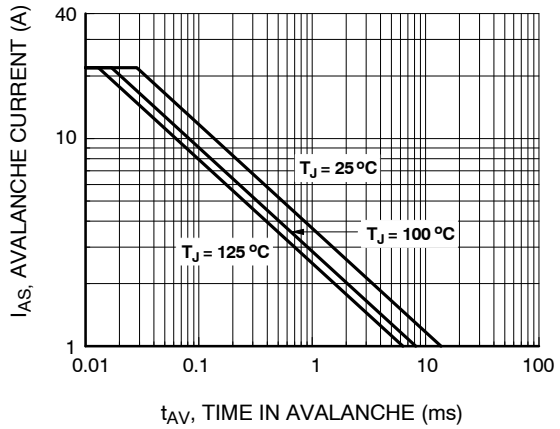


Figure 9. Unclamped Inductive Switching Capability

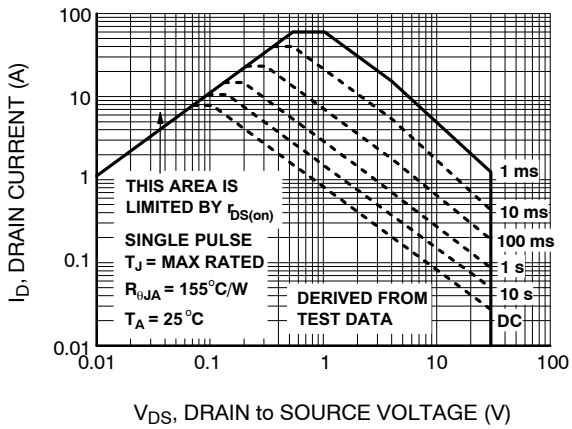


Figure 10. Forward Bias Safe Operating Area

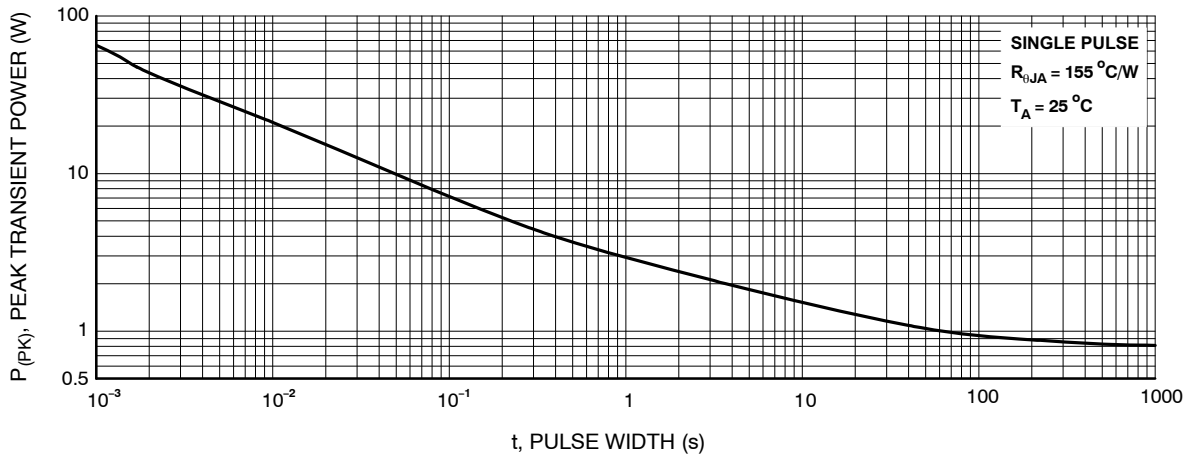


Figure 11. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (Q1 N−CHANNEL) (continued)

(T_J = 25°C unless otherwise noted)

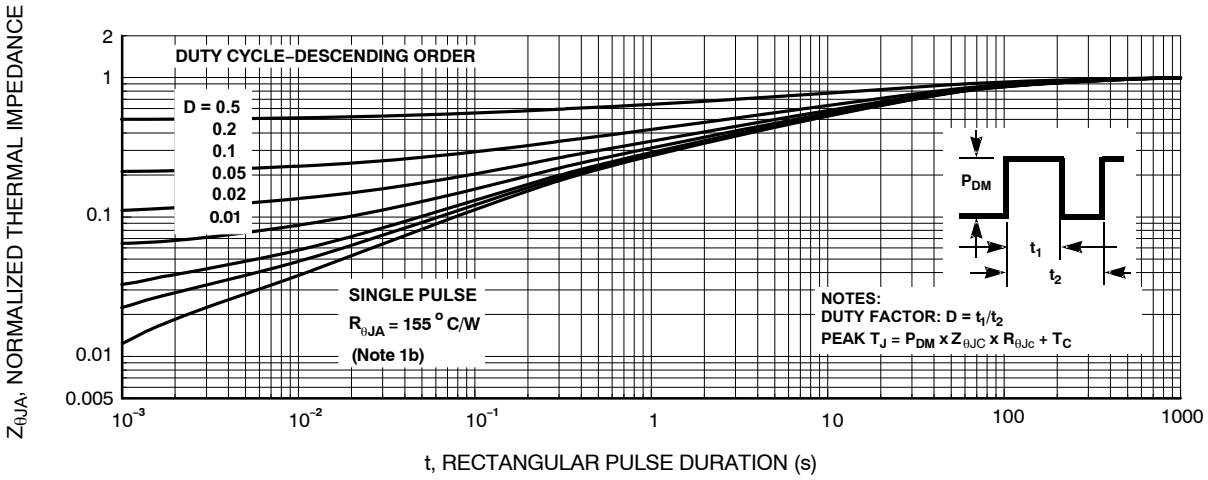


Figure 12. Junction−to−Ambient Transient Thermal Response Curve

TYPICAL CHARACTERISTICS (Q2 N−CHANNEL)

(T_J = 25°C unless otherwise noted)

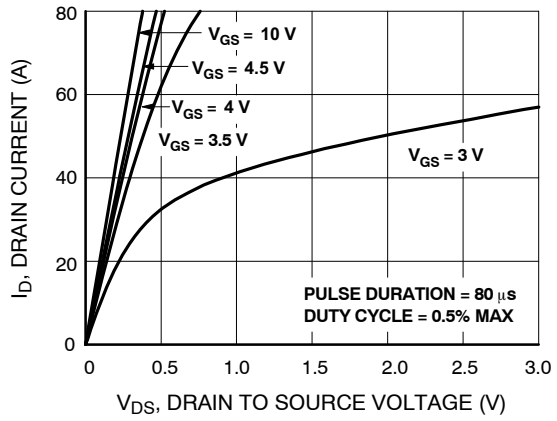


Figure 13. On−Region Characteristics

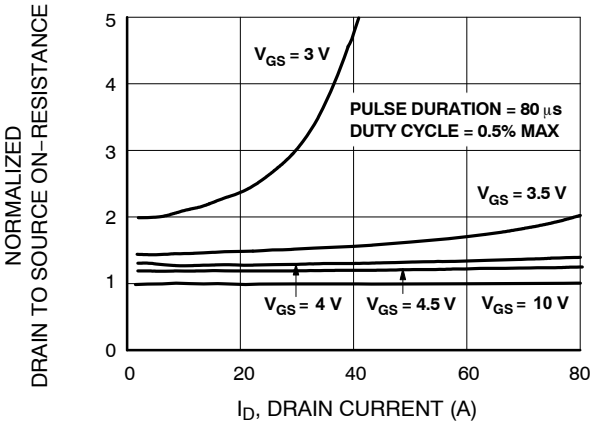


Figure 14. Normalized On−Resistance vs Drain Current and Gate Voltage

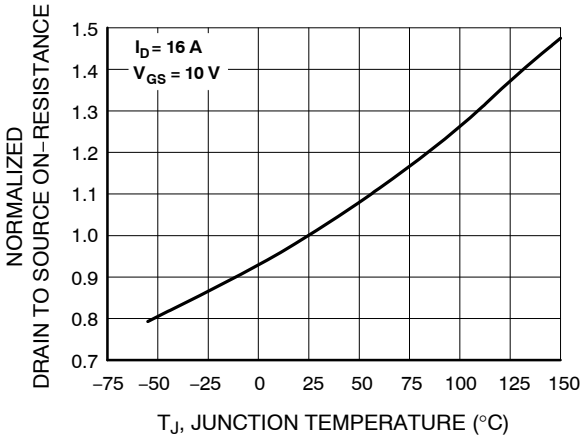


Figure 15. Normalized On−Resistance vs Junction Temperature

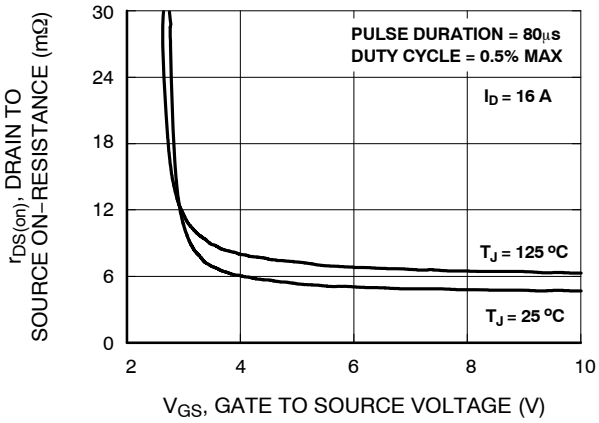


Figure 16. On−Resistance vs Gate to Source Voltage

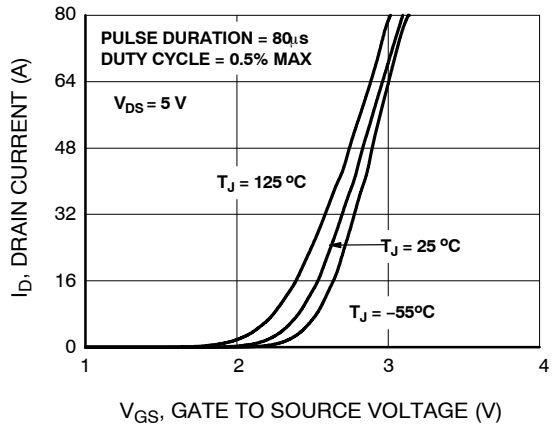


Figure 17. Transfer Characteristics

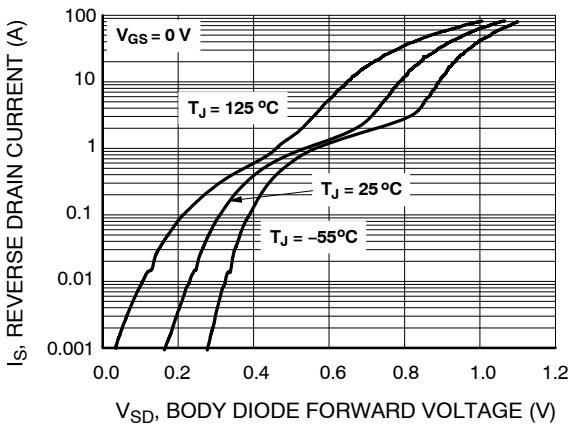


Figure 18. Source to Drain Diode Forward Voltage vs Source Current

TYPICAL CHARACTERISTICS (Q2 N−CHANNEL) (continued)

(T_J = 25°C unless otherwise noted)

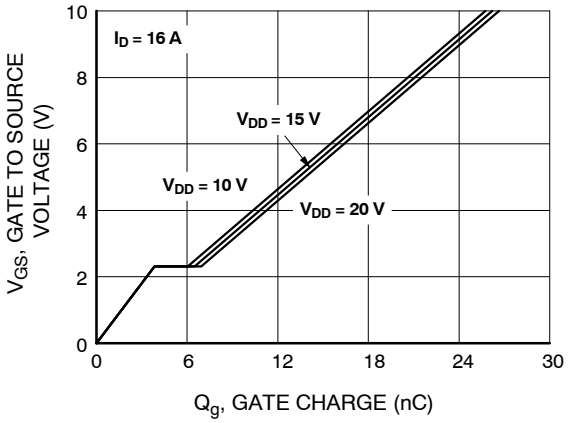


Figure 19. Gate Charge Characteristics

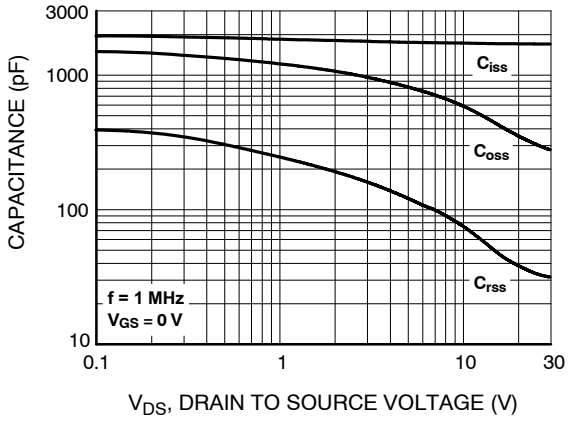


Figure 20. Capacitance vs Drain to Source Voltage

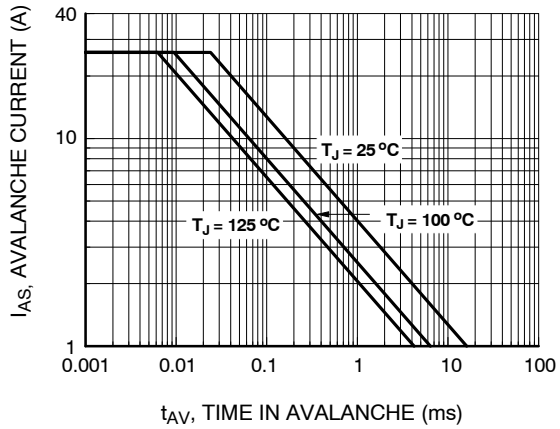


Figure 21. Unclamped Inductive Switching Capability

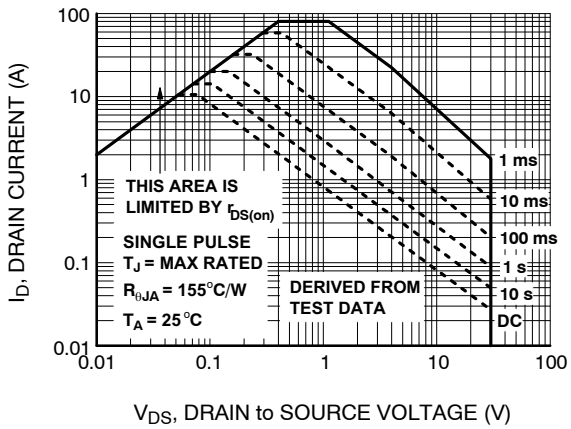


Figure 22. Forward Bias Safe Operating Area

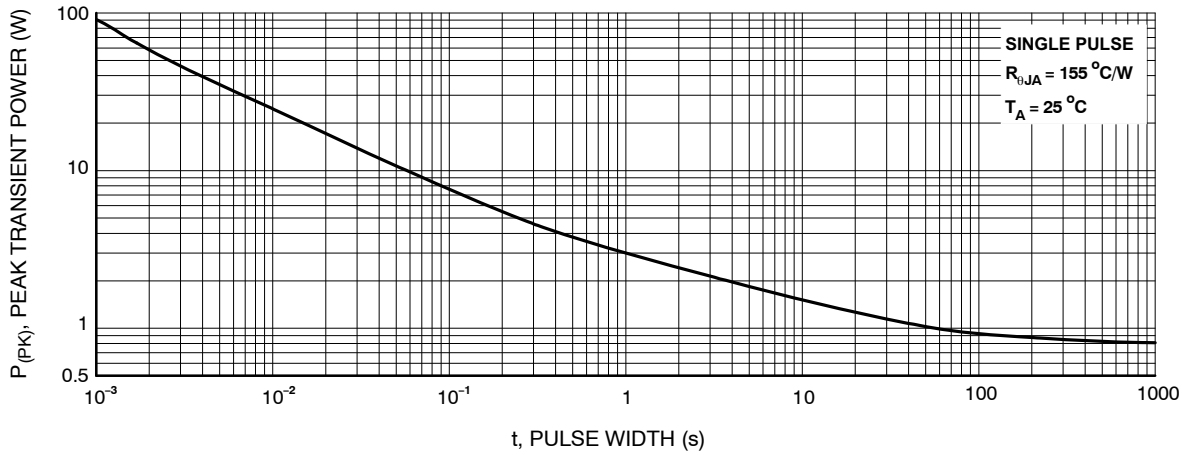


Figure 23. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (Q2 N−CHANNEL) (continued)

(T_J = 25°C unless otherwise noted)

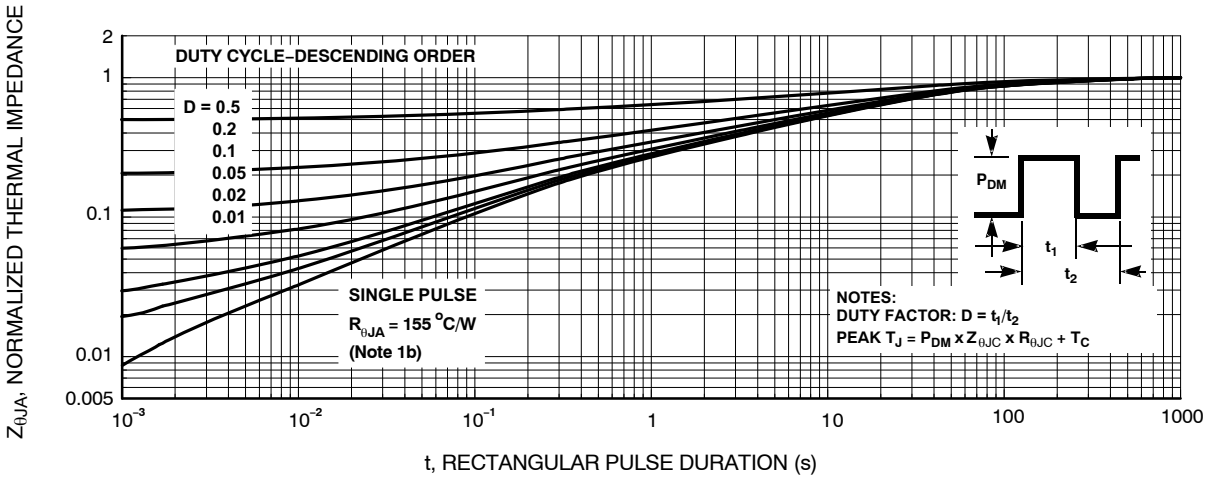


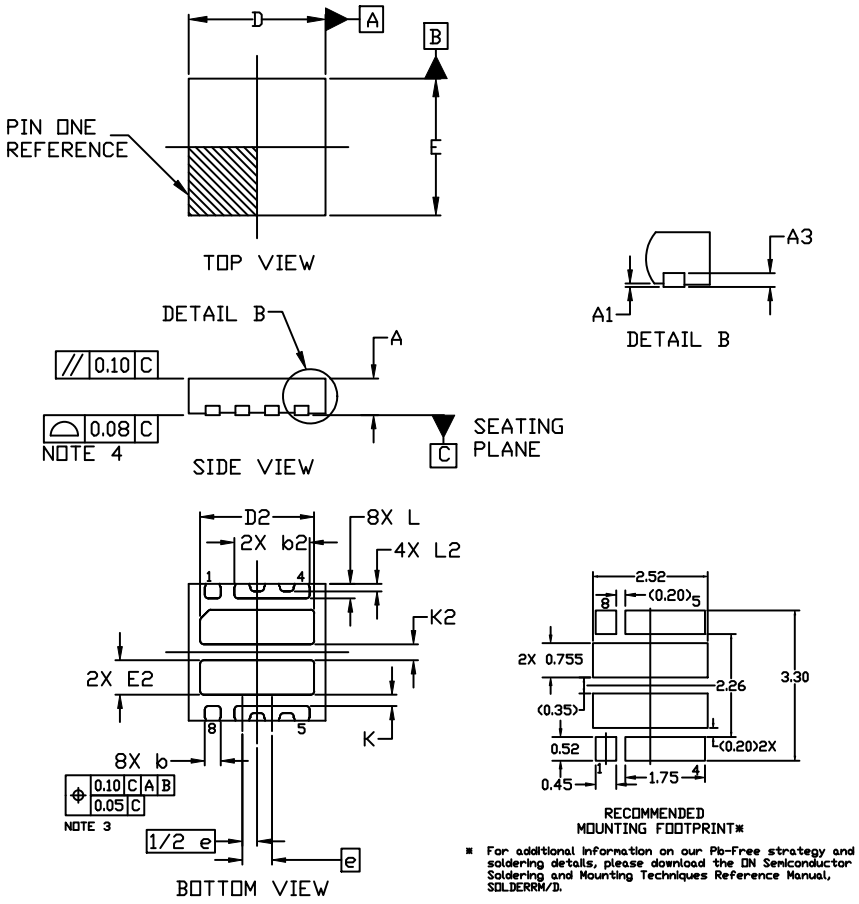
Figure 24. Transient Thermal Response Curve

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

WDFN8 3x3, 0.65P
CASE 511DG
ISSUE A

DATE 12 FEB 2019



* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINALS AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	---	0.05
A3		0.20 REF	
b	0.30	0.35	0.40
b2		1.65 REF	
D	2.90	3.00	3.10
D2	2.45	2.50	2.55
E	2.90	3.00	3.10
E2	1.40	1.50	1.60
e		0.65 BSC	
K	0.25	---	---
K2		0.35 REF	
L	0.27	0.32	0.37
L2		0.163 REF	

GENERIC MARKING DIAGRAM*

XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98AON13623G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**WDFN8 3x3, 0.65P**		**PAGE 1 OF 1**

ADDITIONAL INFORMATION

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