Keywords: CCFL, cold cathode fluorescent lamp, automotive, liquid crystal display, LCD

APPLICATION NOTE 4092

How to Prevent Flicker Caused by Burst Dimming

Jan 28, 2009

Abstract: The DS3881 and DS3882 CCFL controllers are used in automotive, industrial, and avionic applications to backlight LCD panels that require a high dimming ratio. These CCFL controllers use both analog lamp-current amplitude modulation and digital pulse-width burst-dimming techniques to achieve the high dimming ratio. The digital PWM burst dimming can, however, create visible flicker at very low dimming levels. This application note describes how to eliminate the flicker.

Introduction

The DS3881 and DS3882 CCFL controllers use both analog lamp-current amplitude modulation and digital pulse-width-modulation (PWM) burst-dimming techniques to achieve a high dimming ratio. These controllers are typically used in used in automotive, industrial, and avonic applications to backlight LCD panels requiring a high dimming ratio.

Digital PWM burst dimming can cause a problem at very low dimming levels unless an external PWM signal, synchronized to the lamp clock, is used to control the width of the burst-dimming period. If that PWM burst-dimming signal is generated either from the DS3881/DS3882's internal oscillator or from an external oscillator which are asynchronous to the lamp clock, then visible flicker can appear on the LCD panel at very low brightness levels.

This "flicker" problem is easily explained, but harder to solve. At very low brightness levels, there might only be a very few lamp clock cycles per burst-dimming cycle. Therefore, because the burst-dimming clock or signal is not synchronized to the lamp clock, the number of lamp clock cycles in each burst-dimming period can vary by plus or minus one lamp-clock cycle. At most dimming levels this is not a problem. When, however, only a very few burst-dimming cycles (i.e., less than 10) are being generated, the plus/minus variation can appear as flicker in the LCD panel.The flicker is seen because the human eye can detect relative brightness changes greater than about 20%.

There are three work-arounds for this flicker problem. Each approach works with the DS3881/DS3882 controllers.

Work-Around #1: Synchronize the External DPWM to the Lamp Clock

If an external PWM signal is used to control the burst-dimming period, the DS3881/DS3882 internally sample this signal at the PSYNC input on both the rising and the falling edges of the lamp clock. If the external PWM signal is synchronized with the lamp clock, the plus/minus one-lamp-clock-cycle variation

will be eliminated. The LCD panel will not flicker at low dimming levels.

It is important to emphasize that the DS3881/DS3882 sample the external PWM signal on both edges of the lamp clock. As long as the edges of the burst-dimming PWM signal (provided at the PSYNC input) and the lamp clock (provided at the LSYNC input) are not coincident, the plus/minus one-lamp-clock-cycle variation will not occur. *It is recommended that the transitioning edges of the PSYNC input be at least 200ns away from both the rising and falling edge of the lamp clock provided at the LSYNC input.*

Work-Around #2: Provide a Significant Brightness Step at Low Dimming Levels

An alternate approach provides a significant step size between the minimum burst-dimming period and the next brightest step. First, the DS3881/DS3882 are forced into the *minimum* burst-dimming period by either holding the BRIGHT input at 0V, by programming the BPWM register to 01h, or by providing a minimum PWM signal at the PSYNC input. Now the plus/minus one-lamp-clock variation will not occur. The brightness step described here would be the minimum brightness step. If an additional step-up in brightness moves beyond the point at which the user can see flicker, the problem is thus avoided.

As an example, assume a DS3881/DS3882 system like that described in application note 3997, "How to Achieve a 300:1 Dimming Ratio with the DS3881/DS3882 CCFL Controllers." In that system, the minimum burst-dimming period is six lamp cycles. Suppose that the burst-dimming period is increased to 16 lamp cycles, so now the user cannot see flicker. The jump from 6 to 16 lamp cycles is controlled either by the voltage applied at the BRIGHT pin, by the value programmed in the BPWM register, or by the pulse width applied at the PSYNC input.

Work-Around #3: Use the SSP and BLC Registers to Control Brightness

The plus/minus one-lamp-cycle-clock variation mentioned earlier only occurs when the burst-dimming duty cycle begins to exceed the minimum burst created by the DS3881/DS3882. That minimum burst is determined by the programmed number of soft-start lamp cycles and the programmed lamp-cycle sample rate. More details can be found in Application Note 3997 noted above.

As an alternative, the controller can be forced to generate the minimum burst by setting the BPWM register to 01h. Then the user programs the soft-start registers (SSP1 to SSP4) and uses the analog dimming control in the BLC register to control the dimming. The dimming is manipulated until the minimum burst created by the DS3881/DS3882 is long enough that the plus/minus one-lamp-cycle variation will not cause visible flicker.

Table 1 below is based on information in application note 3997, and shows how to accomplish this work-around. The lamp clock rate is assumed to be 60kHz; the burst-dimming frequency is 100Hz. The minimum burst-dimming period will be six lamp cycles, because the soft-start is set to two lamp cycles and the sample rate is set to four lamp cycles.

The minimum brightness occurs at Brightness Step #1. Brightness rises slowly with step-size changes of less than 20%. First the analog lamp current is increased. When the analog lamp current reaches its nominal level (i.e., 100%), the burst-dimming period is increased, not by changing the BPWM register but by increasing the soft-start by two lamp cycles. If increasing the soft-start by two lamp cycles produces too great a brightness jump, then reduce the analog lamp current by a similar amount. As Table 1 illustrates, this latter approach is used until the number of burst-dimming cycles exceeds 20. Then the BPWM register is used to set the brightness.

Table 1. Using the SSP and BLC Registers to Control Brightness

Brightness Step No.	DS3881/DS3882 Register Settings						Configuration		Dimming	
	BPWM	SSP1	SSP2	SSP3	SSP4	BLC	Burst-Dimming Duty Cycle (%)	Analog Lamp-Current Setting (%)	Ratio	Step Size (%)
1	01h	00h	00h	00h	70h	1Fh	1.00	35	286	—
2	01h	00h	00h	00h	70h	1Ch	1.00	41	244	15
3	01h	00h	00h	00h	70h	18h	1.00	49	204	16
4	01h	00h	00h	00h	70h	14h	1.00	57	175	14
5	01h	00h	00h	00h	70h	10h	1.00	66	152	14
6	01h	00h	00h	00h	70h	0Bh	1.00	78	128	15
7	01h	00h	00h	00h	70h	06h	1.00	88	114	11
8	01h	00h	00h	00h	70h	00h	1.00	100	100	12
9	01h	00h	00h	00h	77h	07h	1.33	86	87	13
10	01h	00h	00h	00h	77h	00h	1.33	100	75	14
11	01h	00h	00h	70h	77h	05h	1.67	90	67	12
12	01h	00h	00h	70h	77h	00h	1.67	100	60	10
13	01h	00h	00h	77h	77h	01h	2.00	98	51	15
14	01h	00h	70h	77h	77h	00h	2.33	100	43	16
15	01h	00h	77h	77h	77h	00h	2.67	100	37	13
16	01h	70h	77h	77h	77h	00h	3.00	100	33	11
17	01h	77h	77h	77h	77h	00h	3.33	100	30	10
18	05h	77h	77h	77h	77h	00h	3.91	100	26	15
19	06h	77h	77h	77h	77h	00h	4.69	100	21	17
20	07h	77h	77h	77h	77h	00h	5.47	100	18	14

If the burst-dimming cycle needs to be extended beyond 20 clock cycles to eliminate flicker, the lamp sample rate can be increased first to 8, then 16, and finally 32. Again, the BLC register can be used to increase the number of brightness steps.

A Chinese version of this application note appeared in *EDN China*, August 2008.

Related Parts	
DS3881	Single-Channel, Automotive CCFL Controller
DS3882	Dual-Channel Automotive CCFL Controller

More Information
For Technical Support: http://www.maximintegrated.com/support
For Samples: http://www.maximintegrated.com/samples