PRODUCT / PROCESS CHANGE NOTIFICATION

1. PCN basic data	
1.1 Company	STMicroelectronics International N.V
1.2 PCN No.	MDG/22/13034
1.3 Title of PCN	STM32WB5x and STM32WB3x - product enhancement
1.4 Product Category	STM32WB55Cx, STM32WB55Rx, STM32WB55Vx, STM32WB35Cx, STM32WB50x, STM32WB30Cx
1.5 Issue date	2022-04-21

2. PCN Team	
2.1 Contact supplier	
2.1.1 Name	ROBERTSON HEATHER
2.1.2 Phone	+1 8475853058
2.1.3 Email	heather.robertson@st.com
2.2 Change responsibility	
2.2.1 Product Manager	Ricardo Antonio DE SA EARP
2.1.2 Marketing Manager	Veronique BARLATIER
2.1.3 Quality Manager	Pascal NARCHE

3. Change		
3.1 Category	3.2 Type of change	3.3 Manufacturing Location
General Product & Design	Die redesign : Mask or mask set change with new die design like metallization (specifically chip frontside) or bug fix	TSMC FAB14 (Taiwan)

4. Description of change		
	Old	New
4.1 Description	STM32WB55 and STM32WB35 STM32WB 1M - (Die495 - cut2.1 revision Y) product has limitation as described in Errata Sheet (ES0394 Rev9 / July 2021) - HSE Glitch, 2.2.19, 2.2.20, - SMPS Functionality 2.2.21 STM32WB50 and STM32WB30 - (Die495 - cut2.1 revision Y) product has limitation as described in Errata Sheet (ES0492 - Rev4 - July 2021) - HSE Glitch, 2.2.15 STM32WB5x and STM32WB3x Device Stack-up - Die protective layer over passivation material is PBO (Polybenzoxazole)	STM32WB55 and STM32WB35 - (Die495 - cut2.2 revision X) product fixes those limitations as described in Errata Sheet (ES0394 Rev11 / March 2022): - HSE Glitch in RF Digital/Analog IP is fixed (Note that AN5290 - rev6 describing how to improve tolerance to the glitch is not needed anymore). - SMPS start-up in Analog IP is fixed STM32WB50 and STM32WB30 - (Die495 - cut2.2 revision X) product fixes those limitations as described in Errata Sheet (ES0492 - Rev6 - March 2022): - HSE Glitch in RF Digital/Analog IP is fixed (Note that AN5290 - rev6 describing how to improve tolerance to the glitch is not needed anymore). STM32WB5x and STM32WB3x Device Stack-up - Die protective layer over passivation change from PBO to PI (Polyimide)
4.2 Anticipated Impact on form,fit, function, quality, reliability or processability?	functionality enhancement	

5. Reason / motivation for change	
5.1 Motivation	Improvements was implemented to increase robustness, performances and quality of our products.
5.2 Customer Benefit	SERVICE IMPROVEMENT

6. Marking of parts / traceability of change	
6.1 Description	Traceability ensured by ST internal tools. Die revision changes from "Y" to "X" on Package Marking

7. Timing / schedule	
7.1 Date of qualification results	2022-03-22
7.2 Intended start of delivery	2022-05-16
7.3 Qualification sample available?	Upon Request

8. Qualification / Validation			
8.1 Description	13034 Combined reports RER1613 V3.2 - RER1912 V2.pdf		
8.2 Qualification report and qualification results	Available (see attachment)	**Issue Date**	2022-04-21

9. Attachments (additional documentations)
13034 Public product.pdf 13034 Combined reports RER1613 V3.2 - RER1912 V2.pdf 13034 PCN13034_Additional information.pdf

10. Affected parts		
10. 1 Current		**10.2 New (if applicable)**
10.1.1 Customer Part No	**10.1.2 Supplier Part No**	**10.1.2 Supplier Part No**
	STM32WB30CEU5A	
	STM32WB35CCU6A	
	STM32WB50CGU5	
	STM32WB55CCU6	
	STM32WB55CEU6	
	STM32WB55CGU6	
	STM32WB55CGU6TR	
	STM32WB55RCV6	
	STM32WB55REV6	
	STM32WB55RGV6	
	STM32WB55RGV7	
	STM32WB55VCQ6	
	STM32WB55VEQ6	
	STM32WB55VGQ6	
	STM32WB55VGY6TR	
	STM32WB5MMGH6TR	

Public Products List

Publict Products are off the shelf products. They are not dedicated to specific customers, they are available through ST Sales team, or Distributors, and visible on ST.com

PCN Title : STM32WB5x and STM32WB3x - product enhancement

PCN Reference : MDG/22/13034

Subject : Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change.

STM32WB35CCU6ATR	STM32WB55CCU6	STM32WB55CGU6TR
STM32WB55RCV6	STM32WB5MMGH6TR	STM32WB55RGV7TR
STM32WB55VEQ7	STM32WB55REV6	STM32WB55VGQ6
STM32WB55VCQ7	STM32WB55VGY6TR	STM32WB55CEU6TR
STM32WB35CCU7A	STM32WB55VCY7TR	STM32WB55VCY6TR
STM32WB55CGU7	STM32WB55VEY6TR	STM32WB35CEU7A
STM32WB55VEY7TR	STM32WB55CCU6TR	STM32WB55VEQ6
STM32WB55RGV6	STM32WB55CEU7	STM32WB55CCU7
STM32WB55REV6TR	STM32WB55VCQ6	STM32WB55RCV7
STM32WB30CEU5A	STM32WB55RGV6TR	STM32WB55CEU6
STM32WB55VYY6TR	STM32WB55VGQ7	STM32WB35CEU6A
STM32WB55REV7	STM32WB55CGU6	STM32WB55VGY7TR
STM32WB35CCU6A	STM32WB50CGU5	STM32WB55RGV7

This document is a merge of two reliability report for PCN13034

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MDG-MCD-RERMCD1613
Reliability Report

Qualification Type: Product & Package evaluation

STM32WB55 - 1MBytes
Die 495

Product / Process / Package Information	
Commercial Product:	STM32WB55 – 1MB
Mask Set Revision:	495XXXX (cut 2.2)
Silicon Process Technology:	CMOS 90nm LP RF option
Wafer Fabrication Location:	TSMC(FAB14)
Package:	UFQFPN48 7X7 VFQFPN 8x8 UFBGA 7x7 WLCSP100
Assembly Plant location:	JSCC ATP3 ASE ATT1

Approval List rev 3.2			
Function	Location	Name	Date
Division Q&R Responsible	Grenoble	GALIANO Dominique	09-Feb-2022

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Reliability Evaluation Report

MDG-MCD-RER1912

New System in Package LGA 7.3x11 86L ASEKH

(Package qualification / PCN13034)

General Information	
Commercial Product	:STM32WB5MMGH6TR
Product Line	: 495X66
Die revision	: Cut 2.2
Product Description	: STM32WB5MMGH6TR
Package	: SIP LGA 7.3x11 86L
Silicon Technology	: 90nm eFlash Generic TSMC
Division (2)	: MDG-MCD

Traceability	
WLCSP assembly plant	: AMKOR - ATT1
SIP assembly Plant	: ASEKH TAIWAN

Reliability Assessment	
Pass	☒
Fail	☐

Note: *this report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the electronic device conformance to its specific mission profile. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics or under the approval of the author (see below).*

Version	Date	Author	Function
1.0	16th Nov. 2020	Gabin Bosco	MDG-MCD-QA Back end
2.0	18th Mar. 2022	Berengere Routier-Scappucci	MDG-MCD-QA Back end

MDG-MCD-RERMCD1613
Reliability Report

Qualification Type: Product & Package evaluation

STM32WB55 - 1MBytes
Die 495

Product / Process / Package Information	
Commercial Product:	**STM32WB55 – 1MB**
Mask Set Revision:	**495XXXX (cut 2.2)**
Silicon Process Technology:	**CMOS 90nm LP RF option**
Wafer Fabrication Location:	**TSMC(FAB14)**
Package:	**UFQFPN48 7X7** **VFQFPN 8x8** **UFBGA 7x7** **WLCSP100**
Assembly Plant location:	**JSCC** **ATP3** **ASE** **ATT1**

Approval List rev 1			
Function	**Location**	**Name**	**Date**
Division Q&R Responsible	Grenoble Rousset	GALIANO Dominique BRAVARD Frederic	15-Oct-2018 15-Oct-2018
Division Quality Manager	Rousset	NARCHE Pascal	26-Oct-2018
Approval List rev 2			
Function	**Location**	**Name**	**Date**
Division Q&R Responsible	Grenoble Rousset	GALIANO Dominique BRAVARD Frederic	05-Feb-2019 05-Feb-2019
Approval List rev 3			
Function	**Location**	**Name**	**Date**
Division Q&R Responsible	Rousset Grenoble	SEUBE Gisele GALIANO Dominique	23-Oct-2019 23-Oct-2019

MDG-MCD-RERMCD1613
STM32WB55 - 1MB - Die 495

Approval List rev 3.1			
Function	**Location**	**Name**	**Date**
Division Q&R Responsible	Grenoble	GALIANO Dominique	26-Dec-2019
Approval List rev 3.2			
Function	**Location**	**Name**	**Date**
Division Q&R Responsible	Grenoble	GALIANO Dominique	09-Feb-2022

MDG-MCD-RERMCD1613
STM32WB55 - 1MB - Die 495

Contents

MDG-MCD-RERMCD1613
STM32WB55 - 1MB - Die 495

1 RELIABILITY RESULTS OVERVIEW

1.1 Objectives

The aim of this report is to present results of the reliability evaluation of the STM32WB55 - 1MB - Die 495.

Test vehicle is described here below:

Product	Process	Diffusion	Package	Assembly plant
Die 495	CMOS 90nm LP RF option	TSMC(FAB14)	UFQFPN 7x7	JSCC
			VFQFPN 8x8	ATP3
			UFBGA 7x7	ASEKH
			WLCSP100	ATT1

Qualification is based on standard STMicroelectronics Corporate Procedures for Quality and Reliability, in full compliancy with the JESD-47 international standard

1.2 Conclusion

All reliability tests have been completed with positive results. Neither functional nor parametric rejects were detected at final electrical testing.

According to good reliability tests results in line with validated product mission profile and reliability strategy, the qualification is granted for the STM32WB55 - 1MB - Die 495XXXY (cut 2.2) assembled in all packages listed in the Chapter 1.1, except for WLCSP100 package which will be ready for maturity in Q2 2022.

However, one failure on SMPS leakage test was revealed at HTOL 168h readout on CUT2.2 UFQFN 7x7. Failing root cause has been identified as parasitic inductance from HTOL chipboard PCB layout on SMPS pins is exceeding what will be limited in product Errata Datasheet.

A new HTOL exercise is being launched in the recommended conditions of errata, result will be published in Q3 2022.

Refer to Section 2.4 for reliability test results.

MDG-MCD-RERMCD1613
STM32WB55 - 1MB - Die 495

2 RELIABILITY EVALUATION CONTEXT / PLAN / STRATEGY & RESULTS SUMMARY

2.1 Reliability Evaluation: Context & strategy summary

The STM32WB55 – 1MB (Die 495XXXX) is based on STM32L4x product family, processed in TSMC90nm technology in FAB14

STM32L486x (die 415):	RERMCD1112
STM32L433x (die 435):	RERMCD1424
STM32L452x (die 462):	RERMCD1526
STM32L496x (die 461):	RERMCD1521

The RF option is already qualified via AMG RF products BlueNRG-MS (DM00559663), Reach-1D (DM00559677) and BlueNRG-1(DM00559904).

The STM32WB55 – 1MB (Die 495XXXX) device is assembled in the following package already qualified at Division level:

Package	Reference	Assy Plant location
UFQFPN48 7x7x0.55 P0.5	RERMCD1622	JSCC
VFQFPN68 8x8x1.0 P0.4	RERMCD1701	ATP3
UFBGA129 7X7x0.6 P0.5	RERMCD1901	ASEKH
WLCSP100L P0.4	RERMCD1112	ATT1

Based on these data, and according to “RELIABILITY TESTS AND CRITERIA FOR QUALIFICATION” specification (DMS 0061692), the following qualification strategy has been defined:

- Die Qualification:
  - 3 reliability lots on 495XXXA (Cut 1.0) in UFQFPN48 from SCC (China, Shanghai)
  - 1 reliability lot on 495XXXZ (Cut 1.1) in UFQFPN48 from SCC (China, Shanghai)
  - 1 reliability lot on 495XXXB (Cut 2.0) in UFQFPN48 from JSCC (China, Jiangyin)
  - 1 reliability lot on 495XXXY (Cut 2.1) in UFQFPN48 from JSCC (China, Jiangyin)
  - 1 reliability lot on 495XXXY (Cut 2.1) in UFBGA129 from ASE KH (Taiwan, Kaohsiung)
  - 1 reliability lot on 495XXXX (Cut 2.2) in UFQFPN48 from JSCC (China, Jiangyin)
  - 1 reliability lot on 495XXXY (Cut 2.2) in UFBGA129 from ASE KH (Taiwan, Kaohsiung)

- Package Qualification:

The reliability test plan and result summary are presented in the following tables:

Package	Body	Pitch	Package Code	Wire	Assy	CUT	Trial
UFQFPN48	7x7	0.5	MI	Gold	SCC	1.0	1 lot for ESD CDM
UFQFPN48	7x7	0.5	MI	Gold	JSCC	1.1	1 full reliability lot
UFQFPN48	7x7	0.5	MI	Gold	JSCC	2.0	1 lot for ESD CDM
UFQFPN48	7x7	0.5	MI	Gold	JSCC	2.1	1 lot for ESD CDM
VFQFPN68	8x8	0.4	GB	Gold	ATP3	1.1	3 full reliability lots
VFQFPN68	8x8	0.4	GB	Gold	ATP3	2.0	1 lot for ESD CDM
VFQFPN68	8x8	0.4	GB	Gold	ATP3	2.1	1 lot for ESD CDM
UFBGA129L	7x7	0.65	B09R	Gold	ASEKH	2.1	1 lot for ESD HBM, CDM and LU
UFBGA129L	7x7	0.65	B09R	Gold	ASEKH	2.1	1 lot for package trials
UFBGA129L new RDL	7x7	0.65	B09R	Gold	ASEKH	2.1	1 lot for ESD CDM
WLCSP100L	NA	0.4	A08S	NA	ATT1	2.1	1 lot for ESD CDM
WLCSP100L	NA	0.4	A08S	NA	ATT1	2.1	3 lots for package trials
WLCSP100L new stack up LTC9320	NA	0.4	A08S	NA	ATT1	2.1	1 lot for package trials
WLCSP100L new stack up LTC9320	NA	0.4	A08S	NA	ATT1	2.2	3 lots for package trials

2.2 Reliability Test vehicles description

STM32WB55 – 1MB - is a new product mixing STM32L4 and BLUENRG_LP platforms from STM AMG division.

The STM32WB55 - 1MB is a 32-bits dual core micro-controller based on ARM Cortex M4 and M0+ cores. Featuring innovative power reduction modes and ultra-low-power operation, it embeds a Flash and targets specifically low voltage and low power applications such as IOT.
To support low power radio frequency communication, it embeds a radio supporting Bluetooth low energy and 802.15,4 protocols. The STM32WB55 – 1MB embeds a DC/DC convertor (SMPS for optimizing the low power consumption in some case).

For additional information concerning the product behavior, refer to STM32WB55 datasheet.

MDG-MCD-RERMCD1613
STM32WB55 - 1MB - Die 495

2.3 Reliability Information

Lot ID	Lot 1	Lot 2	Lot 3
Finish Good:	ES32WB52CGU6F$B1	ES32WB52CGU6F$B1	ES32WB52CGU6F$B1
Die Name /cut:	Die 495XXXA / cut 1.0	Die 495XXXA / cut 1.0	Die 495XXXA / cut 1.0
Diffusion Lot Number:	P6W881	P6W881.0G	P6X679
Trace Code :	GH7112BJ	GH71125A	GH72028R
Reliability Lab location :	Grenoble	Grenoble	Grenoble
Fab name location:	TSMC FAB14	TSMC FAB14	TSMC FAB14
Assembly plant location:	SCC CHINA	SCC CHINA	SCC CHINA
Package description:	UFQFPN 7X7X0.55 48L 0.5 MM PITCH GOLD	UFQFPN 7X7X0.55 48L 0.5 MM PITCH GOLD	UFQFPN 7X7X0.55 48L 0.5 MM PITCH GOLD

Lot ID	Lot 4	Lot 5	Lot 6
Finish Good:	ES32WB52CGU6F$B2	ES32WB52CGU6E$S2	ES32WB55CGU7$S3
Die Name /cut:	Die 495XXXZ / cut 1.1	Die 495XXXZ / cut 1.1	Die 495XXXB / cut 2.0
Diffusion Lot Number:	P6W88202A	P60F32B	P60R02X
Trace Code :	GH70227D	GQ7502A7	GQ81225S
Reliability Lab location :	Grenoble	Grenoble	Grenoble Muar
Fab name location:	TSMC FAB14	TSMC FAB14	TSMC FAB14
Assembly plant location:	SCC CHINA	JSCC CHINA	JSCC CHINA
Package description:	UFQFPN 7X7X0.55 48L 0.5 MM PITCH GOLD	UFQFPN 7X7X0.55 48L 0.5 MM PITCH GOLD	UFQFPN 7X7X0.55 48L 0.5 MM PITCH GOLD

Lot ID	Lot 7	Lot 8	Lot 9
Finish Good:	ES32WB55CGU7$74	ES32WB52RGV6B$P2	ES32WB52RGV6B$P2
Die Name /cut:	Die 495XXXY / cut 2.1	Die 495XXXZ / cut 1.1	Die 495XXXZ / cut 1.1
Diffusion Lot Number:	9R804005	9R739071	9R739071
Trace Code :	GQ84526A	7B749A4D	7B748A4D
Reliability Lab location :	Grenoble	Rousset Muar	Rousset Muar
Fab name location:	TSMC FAB14	TSMC FAB14	TSMC FAB14
Assembly plant location:	JSCC CHINA	ATP3 PHILIPPINES	ATP3 PHILIPPINES
Package description:	UFQFPN 7X7X0.55 48L 0.5 MM PITCH GOLD	VFQFPN 8X8X1.0 68L PITCH 0.4 GOLD	VFQFPN 8X8X1.0 68L PITCH 0.4 GOLD

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STM32WB55 - 1MB - Die 495

Lot ID	Lot 10	Lot 11	Lot 12
Finish Good:	ES32WB52RGV6B$P2	ES32WB55RGV7$P3	ES32WB55RGV7$P4
Die Name /cut:	Die 495XXXZ / cut 1.1	Die 495XXXB / cut 2.0	Die 495XXXY / cut 2.1
Diffusion Lot Number:	9R739071	9R752161	9R804005
Trace Code :	7B748A4D	7B813A4E	7B844A3W
Reliability Lab location :	Rousset Muar	Grenoble	Grenoble
Fab name location:	TSMC FAB14	TSMC FAB14	TSMC FAB14
Assembly plant location:	ATP3 PHILIPPINES	ATP3 PHILIPPINES	ATP3 PHILIPPINES
Package description:	VFQFPN 8X8X1.0 68L PITCH 0.4 GOLD	VFQFPN 8X8X1.0 68L PITCH 0.4 GOLD	VFQFPN 8X8X1.0 68L PITCH 0.4 GOLD

Lot ID	Lot 13	Lot 17	Lot 18
Finish Good:	ES32WB55VGQ6K$X4	32WB55VGQ6K$K4	ZZ32WB55CGU7$75
Die Name /cut:	Die 495XXXY / cut 2.1	Die 495XXXY / cut 2.1	Die 495XXXX / cut 2.2
Diffusion Lot Number:	9R847067	9R844194	PBB7020CB
Trace Code :	AA919031	AA946042	GQ1332AU
Reliability Lab location :	Grenoble	Grenoble	Grenoble
Fab name location:	TSMC FAB14	TSMC FAB14	TSMC FAB14
Assembly plant location:	ASEKH	ASEKH	JSCC CHINA
Package description:	UFBGA 7x7 129L 0.5/0.65 PITCH GOLD	UFBGA 7x7 129L 0.5/0.65 PITCH GOLD	UFQFPN 7X7X0.55 48L 0.5 MM PITCH GOLD

Lot ID	Lot 19
Finish Good:	ES32WB55VGQ6K$X4
Die Name /cut:	Die 495XXXX / cut 2.2
Diffusion Lot Number:	PBB703A
Trace Code :	AA137173
Reliability Lab location :	Grenoble
Fab name location:	TSMC FAB14
Assembly plant location:	ASEKH
Package description:	UFBGA 7x7 129L 0.5/0.65 PITCH GOLD

Comment:
ST is certified ISO/TS 16949. This induces certification for all internal and subcontractor plants
ST certification document can be downloaded under the following link:
http://www.st.com/content/st_com/en/support/quality-and-reliability/certifications.html.

MDG-MCD-RERMCD1613
STM32WB55 - 1MB - Die 495

2.4 Reliability Evaluation: Results summary

Die oriented test results in UFQFPN48 7X7X0.55 48L 0.5 MM PITCH GOLD SCC

Die Related Tests						Results		
Description	Test/Method	Conditions	Sample Size	Criteria	Readout / Duration	***Lot 1***	***Lot 2***	***Lot 3***
						495A Cut1.0	495A Cut1.0	495A Cut1.0
Electrostatic discharge - Human Body Model								
ESD HBM	ANSI/ESDA/ JEDEC JS-001	UFQFPN48 1500 Ω, 100 pF	1x3	2kV class 2	2KV	0/3	-	-
Latch Up								
LU	JESD78	UFQFPN48	1x6	A0/R1	130°C	0/6	-	-
NVM Endurance & Data Retention – 10kcy EW @ 125°C then Storage								
EDR	JESD22-A117	HTB 150°C	2x77	A0/R1 10kcyc + 1500h	10Kcy	0/77	0/77	-
					1500h	0/77	0/77	-
NVM Endurance & Data Retention – 10kcy EW @ 25°C then Storage								
EDR	JESD22-A117	HTB 150°C	2x77	A0/R1 10kcyc + 168h	10Kcy	0/77	0/77	-
					168h	0/77	0/77	-
NVM Endurance & Data Retention – 10kcy EW @ -40°C then Storage								
EDR	JESD22-A117	HTB 150°C	2x77	A0/R1 10kcyc + 168h	10Kcy	0/77	0/77	-
					168h	0/77	0/77	-
Early Failure Rate								
ELFR (including SMPS)	MIL-STD-883 Method 1005 JESD22-A108 JESD74	ELFR 125°C, VDD 3V6 SMPS 1.7v/80mA	2x500	A0/R1	48h	0/500	-	0/500
High Temperature Operating Live								
HTOL (including SMPS)	JESD-22A108	HTOL 125°C VDD 3V6 SMPS 1.7v/80mA	2x77	A0/R1	1200h	0/77	0/77	-

MDG-MCD-RERMCD1613
STM32WB55 - 1MB - Die 495

Die Related Tests						
Description	Test/Method	Conditions	Sample Size	Criteria	Readout / Duration	***Lot 4***
						495Z Cut1.1
Electrostatic discharge - Human Body Model						
ESD HBM	ANSI/ESDA/ JEDEC JS-001	UFQFPN48 1500 Ω, 100 pF	1x3	2kV class 2	2KV	0/3
Latch Up						
LU	JESD78	UFQFPN48	1x6	A0/R1	130°C	0/6
High Temperature Operating Live						
HTOL (including RF)	JESD-22A108	HTOL 125°C, VDD 3V6 Vin_RF 1v7	1x77	A0/R1	1200h	0/77

Die Related Tests						
Description	Test/Method	Conditions	Sample Size	Criteria	Readout / Duration	***Lot 6***
						495B Cut2.0
Electrostatic discharge - Human Body Model						
ESD HBM	ANSI/ESDA/ JEDEC JS-001	UFQFPN48 1500 Ω, 100 pF	1x3	2kV class 2	2KV	0/3
Latch Up						
LU	JESD78	UFQFPN48	1x6	A0/R1	130°C	0/6
NVM Endurance & Data Retention – 10kcy EW @ 125°C then Storage						
EDR	JESD22-A117	HTB 150°C	1x77	A0/R1 10kcyc + 1500h	10Kcy	0/77
					1500h	0/77
NVM Endurance & Data Retention – 10kcy EW @ 25°C then Storage						
EDR	JESD22-A117	HTB 150°C	1x77	A0/R1 10kcyc + 168h	10Kcy	0/77
					168h	0/77
NVM Endurance & Data Retention – 10kcy EW @ 25°C then Storage						
EDR	JESD22-A117	HTB 150°C	1x77	A0/R1 10kcyc + 168h	10Kcy	0/77
					168h	0/77
Early Failure Rate						
ELFR (including RF and SMPS)	MIL-STD-883 Method 1005 JESD22-A108 JESD74	HTOL 125°C VDD 3V6 VIN_RF 1v7 SMPS 1.7v/80mA	1x500	A0/R1	48h	0/500
High Temperature Operating Live						
HTOL (including RF and SMPS)	JESD-22A108	HTOL 125°C VDD 3V6 VIN_RF 1v7 SMPS 1.7v/80mA	1x77	A0/R1	1200h	0/77

MDG-MCD-RERMCD1613
STM32WB55 - 1MB - Die 495

Die Related Tests						
Description	Test/Method	Conditions	Sample Size	Criteria	Readout / Duration	***Lot 7***
						495Y Cut2.1
Electrostatic discharge - Human Body Model						
ESD HBM	ANSI/ESDA/ JEDEC JS-001	UFQFPN48 1500 Ω, 100 pF	1x3	2kV class 2	2KV	0/3
Latch Up						
LU	JESD78	UFQFPN48	1x6	A0/R1	130°C	0/6
High Temperature Operating Live						
HTOL (including RF)	JESD-22A108	HTOL 125°C VDD 3V6 VIN_RF 1v7	1x77	A0/R1	168h	0/77

Die Related Tests						
Description	Test/Method	Conditions	Sample Size	Criteria	Readout / Duration	***Lot 18***
						495X Cut2.2
Electrostatic discharge - Human Body Model						
ESD HBM	ANSI/ESDA/ JEDEC JS-001	UFQFPN48 1500 Ω, 100 pF	1x3	2kV class 2	2KV	0/3
Latch Up						
LU	JESD78	UFQFPN48	1x6	A0/R1	130°C	0/6
High Temperature Operating Live						
HTOL (including SMPS)	JESD-22A108	HTOL 125°C VDD 3V6 VIN_RF 1v7 SMPS 1.7v/80mA	1x77	A0/R1	168h	1[1]/77

Comment:

1. 1 failure on SMPS leakage test was revealed at HTOL 168h readout. Failing root cause has been identified as parasitic inductance from HTOL chipboard PCB layout on SMPS pins is exceeding what will be limited in product Errata Datasheet. A new HTOL exercise is being launched in the recommended conditions of errata, result will be published in Q3 2022.

MDG-MCD-RERMCD1613
STM32WB55 - 1MB - Die 495

Die oriented test results in UFBGA 7X7 0.55/0.65 MM PITCH GOLD ASEKH

Die Related Tests						
Description	Test/Method	Conditions	Sample Size	Criteria	Readout / Duration	***Lot 13***
						495Y Cut2.1
Electrostatic discharge - Human Body Model						
ESD HBM	ANSI/ESDA/ JEDEC JS-001	UFBGA129L 1500 Ω, 100 pF	1x3	2kV class 2	2KV	0/3
Latch Up						
LU	JESD78	UFBGA129L	1x6	A0/R1	130°C	0/6

Die Related Tests						
Description	Test/Method	Conditions	Sample Size	Criteria	Readout / Duration	***Lot 19***
						495X Cut2.2
Electrostatic discharge - Human Body Model						
ESD HBM	ANSI/ESDA/ JEDEC JS-001	UFBGA129L 1500 Ω, 100 pF	1x3	2kV class 2	2KV	0/3
Latch Up						
LU	JESD78	UFBGA129L	1x6	A0/R1	130°C	0/6

MDG-MCD-RERMCD1613
STM32WB55 - 1MB - Die 495

Package oriented test results in UFQFPN48 7X7X0.55 48L 0.5 MM PITCH GOLD SCC

Cut 1.x

Package Related Tests						Results	
Description	Test/Method	Conditions	Sample Size	Criteria	Readout / Duration	**Lot 1**	**Lot 4**
						495Z Cut1.0	495Z Cut1.1
Electrostatic discharge – Charge Device Model							
ESD	ANSI/ESDA/ JEDEC JS-002	UFQFPN48	2x3	500V Class C2a	500V	0/3	0/3

Package oriented test results in UFQFPN48 7X7X0.55 48L 0.5 MM PITCH GOLD JSCC

Cut 1.1

Package Related Tests						
Description	Test/Method	Conditions	Sample Size	Criteria	Readout / Duration	**Lot 5**
						495Z Cut1.1
Electrostatic discharge – Charge Device Model						
ESD	ANSI/ESDA/ JEDEC JS-002	UFQFPN48	1x3	500V Class C2a	500V	0/3
Preconditioning: moisture sensitivity level 3						
PC	J-STD-020 JESD22-A113	24h bake @125°C 192h @ 30°C / 60% RH Reflow simulation (3 times) @ 260°C peak temperature	1x308	A0/R1	N.A	0/308
High Temperature Storage Life after preconditioning						
HTSL	JESD 22-A103	150°C	1x77	A0/R1 1000h		0/77
Thermal Cycling after Preconditioning						
TC	JESD 22-A104	-65c/+150°c	1x77	A0/R1 500cy	500cy	0/77
Unbiased Highly Accelerated Temperature and Humidity Stress after Preconditioning						
UHAST	JESD 22-A118	130°C ,85% 2Atm RH	1x77	A0/R1 96h	96h	0/77
Temperature Humidity Bias after Preconditioning						
THB	JESD 22-A110	85°C/85%RH Bias VDD=3v6	1x77	A0/R1 1000h	1000h	0/77

MDG-MCD-RERMCD1613
STM32WB55 - 1MB - Die 495

Cut 2.0

Package Related Tests						Results
Description	Test/Method	Conditions	Sample Size	Criteria	Readout / Duration	**Lot 6**
						495Z Cut2.0
Electrostatic discharge – Charge Device Model						
ESD	ANSI/ESDA/ JEDEC JS-002	UFQFPN48	1x3	500V Class C2a	500V	0/3
Construction analysis						
CA	Construction Analysis including : -Wire bond shear -Wire bond pull -Solderability -Physical Dimension	JESD 22B102 JESDB100/B108	50	No concern	NA	No concern

Cut 2.1

Package Related Tests						Results
Description	Test/Method	Conditions	Sample Size	Criteria	Readout / Duration	**Lot 6**
						495Z Cut2.0
Electrostatic discharge – Charge Device Model						
ESD	ANSI/ESDA/ JEDEC JS-002	UFQFPN48	1x3	500V Class C2a	500V	0/3

Cut 2.2

Package Related Tests						Results
Description	Test/Method	Conditions	Sample Size	Criteria	Readout / Duration	**Lot 18**
						495Z Cut2.2
Electrostatic discharge – Charge Device Model						
ESD	ANSI/ESDA/ JEDEC JS-002	UFQFPN48	1x3	500V Class C2a	500V	0/3

MDG-MCD-RERMCD1613
STM32WB55 - 1MB - Die 495

Package oriented test results in VFQFPN68 8X8X1.0 68L 0.4 MM PITCH GOLD ATP3

Cut 1.1

Package Related Tests						Results		
						VFQFPN68		
Description	***Test/Method***	***Conditions***	***Sample Size***	***Criteria***	***Readout / Duration***	***Lot 8***	***Lot 9***	***Lot 10***
Electrostatic discharge – Charge Device Model								
ESD	ANSI/ESDA/ JEDEC JS-002	VFQFPN68	1x3	500V	500V Class C2a		0/3	
Preconditioning: moisture sensitivity level 3								
PC	J-STD-020 JESD22-A113	24h bake @125°C 192h @ 30°C / 60% RH Reflow simulation (3 times) @ 260°C peak temperature	3x308	A0/R1	NA	0/308	0/308	0/308
		Delamination	3x60	No delamination				
High Temperature Storage Life after preconditioning								
HTSL	JESD 22-A103	150°C	3x77	A0/R1 1000h	1000h	0/77	0/77	0/77
Thermal Cycling after Preconditioning								
TC	JESD 22-A104	-65°C/+150°C	3x77	A0/R1 500cyc	500cy	0/77	0/77	0/77
					1000cy for monitoring	0/77	0/77	0/77
Unbiased Highly Accelerated Temperature and Humidity Stress after Preconditioning								
uHAST	JESD 22A118	130°C, 85%RH 2Atm	3x77	A0/R1 96h	96h	0/77	0/77	0/77
Temperature Humidity Bias after Preconditioning								
THB	JESD 22A101	85°C/85%RH Bias VDD=3v6	3x77	A0/R1 1000h	1000h	0/77	0/77	0/77
Construction Analysis								
CA	Construction Analysis including : -Wire bond shear -Wire bond pull -Solderability -Physical Dimension	JESD 22B102 JESDB100/B108	3 x 50	No concern	NA	No concern	No concern	No concern

Cut 2.x

Package Related Tests						Results	
Description	***Test/Method***	***Conditions***	***Sample Size***	***Criteria***	***Readout / Duration***	***Lot 11***	***Lot 12***
						495B Cut2.0	495Y Cut2.1
Electrostatic discharge – Charge Device Model							
ESD	ANSI/ESDA/ JEDEC JS-002	VFQFPN68	2x3	500V Class C2a	500V	0/3	0/3

MDG-MCD-RERMCD1613
STM32WB55 - 1MB - Die 495

Package oriented test results in UFBGA 7X7 129L 0.55/0.65 MM PITCH GOLD ASEKH

Cut 2.1

Package Related Tests						Results
Description	***Test/Method***	***Conditions***	***Sample Size***	***Criteria***	***Readout / Duration***	***UFBGA129L Lot 13***
Electrostatic discharge – Charge Device Model						
ESD	ANSI/ESDA/ JEDEC JS-002	UFBGA129L	1x3	250V Class C1	250V	0/3
Preconditioning: moisture sensitivity level 3						
PC	J-STD-020 JESD22-A113	24h bake @125°C 192h @ 30°C / 60% RH Reflow simulation (3 times) @ 260°C peak temperature	1x308	A0/R1	NA	0/308
		Delamination	1x60	No delamination		
High Temperature Storage Life after preconditioning						
HTSL	JESD 22-A103	150°C	1x77	A0/R1 1000h	1000h	0/77
Thermal Cycling after Preconditioning						
TC	JESD 22-A104	-65°C/+150°C	1x77	A0/R1 500cyc	500cy	0/77
					1000cy for monitoring	0/77
Unbiased Highly Accelerated Temperature and Humidity Stress after Preconditioning						
uHAST	JESD 22A118	130°C, 85%RH 2Atm	1x77	A0/R1 96h	96h	0/77
Temperature Humidity Bias after Preconditioning						
THB	JESD 22A101	85°C/85%RH Bias VDD=3v6	1x77	A0/R1 1000h	1000h	0/77
Construction Analysis						
CA	Construction Analysis including: -Ball shear -Solderability -Physical Dimension	JESD 22B102 JESDB100/B108	3 x 50	No concern	NA	No concern

Package Related Tests						Results
Description	***Test/Method***	***Conditions***	***Sample Size***	***Criteria***	***Readout / Duration***	***UFBGA129L Lot 17***
Electrostatic discharge – Charge Device Model						
ESD	ANSI/ESDA/ JEDEC JS-002	UFBGA129L new RDL	1x3	250V Class C1	250V	0/3

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STM32WB55 - 1MB - Die 495

Cut 2.2

Package Related Tests						Results
Description	***Test/Method***	***Conditions***	***Sample Size***	***Criteria***	***Readout / Duration***	***UFBGA129L*** ***Lot 19***
Electrostatic discharge – Charge Device Model						
ESD	ANSI/ESDA/ JEDEC JS-002	UFBGA129L new RDL	1x3	250V Class C1	250V	0/3

MDG-MCD-RERMCD1613
STM32WB55 - 1MB - Die 495

3 RELIABILITY TEST VEHICLES CHARACTERISTICS

3.1 Front-End information

Front-End	Diffusion FAB
Wafer Fab Name	TSMC FAB14
Wafer Fab Location/ Address	1-1, Nan-Ke North Rd., Tainan Science Park, Tainan 741-44, Taiwan
Process Technology Name	TSMC090 ULL
Wafer Diameter	12 inch
Wafer Thickness	775µm +/- 25µm
Die Size	19.50 mm²
Technology Mask Number	48
Scribe Line size x/y:	80 x 80µm
Pad Die Size /Pad type:	123x59um
Layer Under Metallization Material Thickness	Silicon oxide 180nm
Metal Layers Number Materials Thickness	Metal 1 TaN/Ta/CuSeed/Cu 0.240 um Metal 2 TaN/Ta/CuSeed/Cu 0.310 um Metal 3 TaN/Ta/CuSeed/Cu 0.310 um Metal 4 TaN/Ta/CuSeed/Cu 0.310 um Metal 5 TaN/Ta/CuSeed/Cu 0.310 um Metal 6 TaN/Ta/CuSeed/Cu 0.850 um Metal 7 TaN/CuSeed/Cu 3.400 um Metal 8 AlCu 1.450 um
Passivation Layers Number Materials Thickness	750Å nit+ 4000Å oxide + 750 Å nit + 2500 Å oxide
Back Metal Finishing Thickness	NA
Die overcoat: Material Thickness	NA
Other Device using same process	STM32L4x family
FIT Level (Ea=0.7eV, C.L: 60%, 55°C)	3.5 FITs at qualification date
Soft Error Rate Alpha SER [FIT/Mb] Neutron SER [FIT/Mb] Conditions	Alpha SER: 491 FIT/Mb Neutron SER: 445 FIT/Mb Neutron SER is an estimation at sea level of NYC (14n/h/cm²). Alpha result is estimated using a nominal flux of 0.001α/h/cm²
Wafer Level Reliability Electro-Migration (EM) Time Dependent Dielectric Breakdown (TDDB) or Gate Oxide Integrity (GOI) Hot Carrier Injection (HCI) Negative Bias Thermal Instability (NBTI) Stress Migration (SM)	 Yes Yes Yes Yes Yes

3.2 Back-End information

Back-End	Lot 4	Lot 5	Lot 6
Assembly Plant Location/ Address:	Statschippac Semi-conductor Shanghai Co., Ltd. 188 Hua Xu Road Shanghai (China)	Statschippac Semi-conductor Jiangyin Co., Ltd. No. 78 Changshan Rd, Jiangyin (China)	Statschippac Semi-conductor Jiangyin Co., Ltd. No. 78 Changshan Rd, Jiangyin (China)
Die Thickness after Back grinding:	150 +/- 25µm	150 +/- 25µm	150 +/- 25µm
Die sawing method:	Laser Grooving + Mechanical dicing	Laser Grooving + Mechanical dicing	Laser Grooving + Mechanical dicing
Die attach material: **Type:** **Supplier:**	Glue EN4900GC HITACHI	Glue EN4900GC HITACHI	Glue EN4900GC HITACHI
Lead frame material: **L/F Finishing Type:** **Die paddle size:**	Rough Cu LF UQFN48L 5.2sq	Rough Cu LF UQFN48L 5.2sq	Rough Cu LF UQFN48L 5.2sq
Wire bonding: **Type /Diameter:**	Gold wire 0.8 mil	Gold wire 0.8 mil	Gold wire 0.8 mil
Lead Plating **Natures** **Thickness**	Pure Tin (e3) Tolerance 7 to 20 µm	Pure Tin (e3) Tolerance 7 to 20 µm	Pure Tin (e3) Tolerance 7 to 20 µm
Molding Compound Supplier:	EME-G770 Sumitomo	EME-G770 Sumitomo	EME-G770 Sumitomo
Package Moisture Sensitivity Level (JEDEC J-STD020D):	3	3	3

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STM32WB55 - 1MB - Die 495

Back-End	Lot 7	Lot 8	Lot 9
Assembly Plant Location/ Address:	Statschippac Semi-conductor Jiangyin Co., Ltd. No. 78 Changshan Rd, Jiangyin (China)	AMKOR ATP Site P3 119 North Science Avenue Special Economic Processing Zone Laguna Technopark, Binan Laguna PHILIPPINES 4024	AMKOR ATP Site P3 119 North Science Avenue Special Economic Processing Zone Laguna Technopark, Binan Laguna PHILIPPINES 4024
Die Thickness after Back grinding:	150 +/- 25µm	250 +/- 25 µm	250 +/- 25 µm
Die sawing method:	Laser Grooving + Mechanical dicing	Laser Grooving + Mechanical dicing	Laser Grooving + Mechanical dicing
Die attach material: **Type:** **Supplier:**	Glue EN4900GC HITACHI	GLUE 1234-100 Dexter	GLUE 1234-100 Dexter
Lead frame material: **L/F Finishing Type:** **Die paddle size:**	Rough Cu LF UQFN48L 5.2sq	Rc Cu LF VQFN8x8 68L Pad 6.6 mm x 6.6 mm	Rc Cu LF VQFN8x8 68L Pad 6.6 mm x 6.6 mm
Wire bonding: **Type /Diameter:**	Gold wire 0.8 mil	Gold wire 0.8 mil	Gold wire 0.8 mil
Lead Plating Natures **Thickness**	Pure Tin (e3) Tolerance 7 to 20 µm	Pure Tin (e3) Tolerance 7 to 20 µm	Pure Tin (e3) Tolerance 7 to 20 µm
Molding Compound Supplier:	EME-G770 Sumitomo	EME-G770Y Sumitomo	EME-G770Y Sumitomo
Package Moisture Sensitivity Level (JEDEC J-STD020D):	3	3	3

MDG-MCD-RERMCD1613
STM32WB55 - 1MB - Die 495

Back-End	Lot 10	Lot 11	Lot 12
Assembly Plant Location/ Address:	AMKOR ATP Site P3 119 North Science Avenue Special Economic Processing Zone Laguna Technopark, Binan Laguna PHILIPPINES 4024	AMKOR ATP Site P3 119 North Science Avenue Special Economic Processing Zone Laguna Technopark, Binan Laguna PHILIPPINES 4024	AMKOR ATP Site P3 119 North Science Avenue Special Economic Processing Zone Laguna Technopark, Binan Laguna PHILIPPINES 4024
Die Thickness after Back grinding:	250 +/- 25 µm	250 +/- 25 µm	250 +/- 25 µm
Die sawing method:	Laser Grooving + Mechanical dicing	Laser Grooving + Mechanical dicing	Laser Grooving + Mechanical dicing
Die attach material: **Type:** **Supplier:**	GLUE 1234-100 Dexter	GLUE 1234-100 Dexter	GLUE 1234-100 Dexter
Lead frame material: **L/F Finishing Type:** **Die paddle size:**	Rc Cu LF VQFN8x8 68L Pad 6.6 mm x 6.6 mm	Rc Cu LF VQFN8x8 68L Pad 6.6 mm x 6.6 mm	Rc Cu LF VQFN8x8 68L Pad 6.6 mm x 6.6 mm
Wire bonding: **Type /Diameter:**	Gold wire 0.8 mil	Gold wire 0.8 mil	Gold wire 0.8 mil
Lead Plating Natures **Thickness**	Pure Tin (e3) Tolerance 7 to 20 µm	Pure Tin (e3) Tolerance 7 to 20 µm	Pure Tin (e3) Tolerance 7 to 20 µm
Molding Compound Supplier:	EME-G770Y Sumitomo	EME-G770Y Sumitomo	EME-G770Y Sumitomo
Package Moisture Sensitivity Level (JEDEC J-STD020D):	3	3	3

MDG-MCD-RERMCD1613
STM32WB55 - 1MB - Die 495

Back-End	Lot 13	Lot 19
Assembly Plant Location/ Address:	ASE (Kaohsiung) 26, Chin 3rd Nantze Export Nantze Export Processing Zone Kaohsiung 81170 Taiwan	ASE (Kaohsiung) 26, Chin 3rd Nantze Export Nantze Export Processing Zone Kaohsiung 81170 Taiwan
Die Thickness after Back grinding:	75 +/- 10 µm	75 +/- 10 µm
Die sawing method:	Laser Grooving + Mechanical dicing	Laser Grooving + Mechanical dicing
Die attach material: **Type:** **Supplier:**	ABLESTICK ATB-125	ABLESTICK ATB-125
Lead frame material: **L/F Finishing** **Type:** **Die paddle size:**	UFBGA129 7x7	UFBGA129 7x7
Wire bonding: **Type /Diameter:**	Gold wire 0.8 mil	Gold wire 0.8 mil
Lead Plating **Natures** **Thickness**	e2 Sn alloys with no Bi or Zn	e2 Sn alloys with no Bi or Zn
Molding Compound Supplier:	G1250AAS ULA KYOCERA	G1250AAS ULA KYOCERA
Balls metallurgy/ diameter/supplier (BGA/CSP)	Solder ball Diam 200um SN96.5 AG3.5%	Solder ball Diam 200um SN96.5 AG3.5%
Package Moisture Sensitivity Level (JEDEC J-STD020D):	3	3

MDG-MCD-RERMCD1613
STM32WB55 - 1MB - Die 495

Back-End	Lot 18
Assembly Plant Location/ Address:	Statschippac Semi-conductor Jiangyin Co., Ltd. No. 78 Changshan Rd, Jiangyin (China)
Die Thickness after Back grinding:	150 +/- 25µm
Die sawing method:	Laser Grooving + Mechanical dicing
Die attach material: **Type:** **Supplier:**	Glue EN4900GC HITACHI
Lead frame material: **L/F Finishing** **Type:** **Die paddle size:**	Rough Cu LF UQFN48L 5.2sq
Wire bonding: **Type /Diameter:**	Gold wire 0.8 mil
Lead Plating **Natures** **Thickness**	Pure Tin (e3) Tolerance 7 to 20 µm
Molding Compound **Supplier:**	EME-G770 Sumitomo
Package Moisture Sensitivity Level (JEDEC J-STD020D):	3

APPLICABLE AND REFERENCE DOCUMENTS

DMS 0061692 :	Reliability Tests And Criteria For Qualifications
SOP 2.6.2:	Process qualification and transfer management
SOP 2.6.7:	Product Maturity Level
SOP 2.6.9:	Package and process maturity management in Back End
SOP 2.6.11:	Program management from product qualification
SOP 2.6.19:	Process maturity level
JESD47	Stress-Test-Driven Qualification of Integrated Circuits
ANSI/ESDA/ JEDEC JS-001	Electrostatic discharge (ESD) sensitivity testing human body model (HBM)
ANSI/ESDA/ JEDEC JS-002	Electrostatic discharge (ESD) sensitivity testing charge device model (CDM)
JESD78	IC Latch-up test
JESD 22-A108	Temperature, Bias and Operating Life
JESD 22-A117	Endurance and Data retention
JESD 22-A103	High Temperature Storage Life
J-STD-020:	Moisture/reflow sensitivity classification for non-hermetic solid state surface mount devices
JESD22-A113:	Preconditioning of non-hermetic surface mount devices prior to reliability testing
JESD22-A118:	Unbiased Highly Accelerated temperature & humidity Stress Test
JESD22-A104:	Temperature cycling
JESD22-A101:	Temperature Humidity Bias
JESD22-A110:	Biased Highly Accelerated temperature & humidity stress Test
JESD 22B102:	Solderability test
JESD22B100/B108:	Physical dimension

4 GLOSSARY AND TESTS DESCIPTION

HTOL	High Temperature Operating Life
EDR	Endurance and Data Retention
ELFR	Early Failure Rate
PC	Preconditioning (solder simulation)
THB	Temperature Humidity Bias
TC	Temperature cycling
uHAST	Unbiased Highly Accelerated Stress Test
HTSL	High temperature storage life
DMS	ST Advanced Documentation Controlled system/ Documentation Management system
ESD HBM	Electrostatic discharge (human body model)
ESD CDM	Electrostatic discharge (charge device model)
LU	Latch-up
CA	Construction Analysis

MDG-MCD-RERMCD1613
STM32WB55 - 1MB - Die 495

REVISION HISTORY

Version	Date	Author	Comment
1	1st of October, 2018	Laurent CLARAMOND Muriel GALTIER Berengere ROUTIER-SCAPUCCI	Initial release
1.1	21st of January, 2019	Laurent Claramond	UFQFPN48 cut 2.1
2.0	1st of February, 2019	Laurent CLARAMOND Berengere ROUTIER-SCAPUCCI	Correction typo error table §3.1 Update with VFQFPN68
3.0	22nd of October,2019	Laurent CLARAMOND Céline Navarro	Updated with UFBGA129 cut 2.1
3.1	16th of December,2019	Laurent CLARAMOND	Updated with UFBGA129 New RDL cut 2.1 LOT17
3.2	21st of January, 2022	Moses TAN	Updated with cut 2.2

MDG-MCD-RERMCD1613
STM32WB55 - 1MB - Die 495

Reliability Evaluation Report

MDG-MCD-RER1912

New System in Package LGA 7.3x11 86L ASEKH

(Package qualification / PCN13034)

General Information	
Commercial Product	*:STM32WB5MMGH6TR*
Product Line	*: 495X66*
Die revision	*: Cut 2.2*
Product Description	*: STM32WB5MMGH6TR*
Package	*: SIP LGA 7.3x11 86L*
Silicon Technology	*: 90nm eFlash Generic TSMC*
Division (2)	*: MDG-MCD*

Traceability	
WLCSP assembly plant	*: AMKOR - ATT1*
SIP assembly Plant	*: ASEKH TAIWAN*

Reliability Assessment	
Pass	☒
Fail	☐

Note: *this report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the electronic device conformance to its specific mission profile. This report and its contents shall not be disclosed to a third party without previous written agreement from STMicroelectronics or under the approval of the author (see below).*

Version	Date	Author	Function
1.0	16th Nov. 2020	Gabin Bosco	MDG-MCD-QA Back end
2.0	18th Mar. 2022	Berengere Routier-Scappucci	MDG-MCD-QA Back end

APPROVED BY:

Function	Location	Name	Version	Date
Division Q&R Responsible	RSST	Pascal NARCHE	1.0	16th Nov. 2020
Division Quality Manager	RSST	Gisele SEUBE	1.0	16th Nov. 2020
Division Q&R Responsible	RSST	Pascal NARCHE	2.0	22nd Mar. 2022

TABLE OF CONTENTS

1 RELIABILITY EVALUATION OVERVIEW

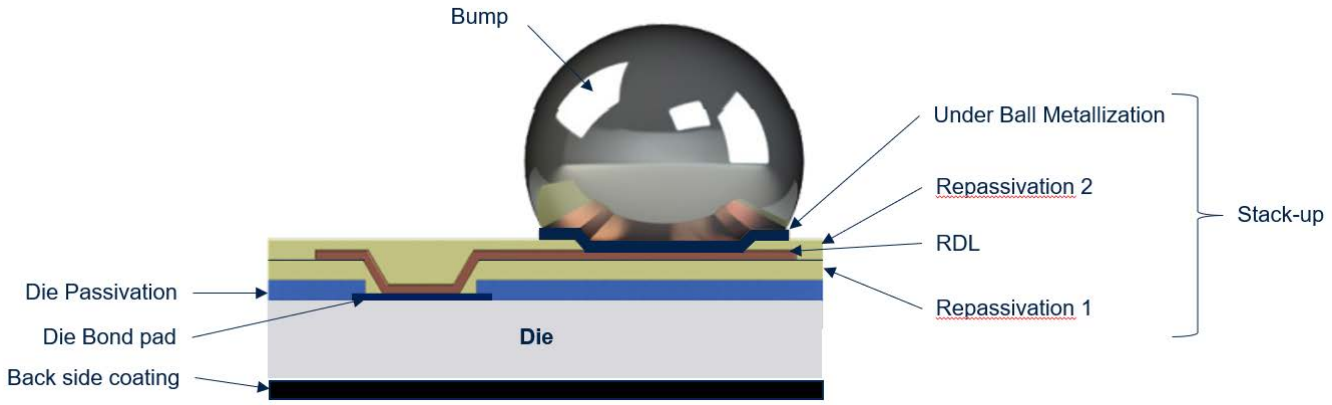
1.1 Objective

The aim of this report is to present results of the reliability evaluation of new System in Package LGA 7.3x11 86L in ASEKH, including die 495 in WLCSP 100L.

In order to increase robustness and quality of the package, a Production Change Notification (PCN) was initiated with change described below:

PCN13034:

		STM32WB 1M Die 495	
		Before Cut 2.1	New condition Cut 2.2
Die revision		"Y"	"X"
Stack-up	Die protective layer over passivation (Repassivation 1 & repassivation 2)	PBO (Polybenzoxazole)	PI (Polyimide)
	RDL thickness	Plated Copper 4um	Plated Copper 6um



Qualification is based on standard STMicroelectronics Corporate Procedures for Quality and Reliability, in full compliancy with the JESD-47 international standard.

1.2 Reliability Strategy

ST Microcontrollers Division intends to qualify a new System in Package LGA7.3x11 86L at ASEKH.

According to "RELIABILITY TESTS AND CRITERIA FOR QUALIFICATION" specification (DMS 0061692), the following qualification strategy has been defined:

Package	Assembly Plant	Cut die 495	Stack up	Trial
SIP LGA 7.3x11 86L	ASEKH TAIWAN	2.1	PBO	3 full reliability lots
SIP LGA 7.3x11 86L with Daisy Chain	ASEKH TAIWAN	2.1	PBO	1 lot for evaluation of package soldered to a printed circuit board
SIP LGA 7.3x11 86L	ASEKH TAIWAN	2.1	LTC9320	1 full reliability lot
SIP LGA 7.3x11 86L	ASEKH TAIWAN	2.2	LTC9320	1 full reliability lot

Reliability test conditions have been defined according to specification limit values of components.

1.3 Conclusion

All reliability tests have been completed with positive results. Neither functional nor parametric rejects were detected at final electrical testing.

According to good reliability tests results in line with validated product mission profile and reliability strategy, the qualification is granted for the System in Package LGA 7.3x11 86L in ASEKH.

Refer to Section 3.0 for reliability test results.

2 PRODUCT CHARACTERISTICS

2.1 Generalities

Package line	Assembly Line Package	Device (Partial RawLine Code)	Diffusion Process	Number of Lots
SIP LGA	*SIP LGA 7.3x11 86L*	*7D*495*	*90nm eFlash Generic TSMC*	*6*

2.2 Traceability

2.2.1 WLCSP assembly information

Table 1

Assembly Information	
Package 1 – WLCSP 100L (PBO passivation) lot1, Lot2 & lot3	
Assembly plant name / location	*AMKOR ATT1* *1F, No. 1, Kao-Ping Sec, Chung-Feng Rd,Lungtan Township,Taoyuan County* *325 TAIWAN*
Pitch (mm)	*0.4*
Die thickness	*355 µm*
Die sawing method	*Laser grooving + Mechanical dicing*
Bill of Material elements	
Balls metallurgy/diameter	*Solder ball SAC405 Diam 230 µm*
Routing/Redistribution layer (RDL) material/thickness	*RDL Copper 4 µm*
Passivation material	*PBO passivation HD8820*
Backside coating material/thickness	*Backside coating PET film 25 µm*
Package Moisture Sensitivity Level (JEDEC J-STD020D)	*1*
Package 2 – WLCSP 100L (LTC9320 passivation) lot5, lot6 & lot7	
Assembly plant name / location	*AMKOR ATT1* *1F, No. 1, Kao-Ping Sec, Chung-Feng Rd,Lungtan Township,Taoyuan County* *325 TAIWAN*
Pitch (mm)	*0.4*
Die thickness	*355 µm*
Die sawing method	*Laser grooving + Mechanical dicing*
Bill of Material elements	
Balls metallurgy/diameter	*Solder ball SAC405 Diam 230 µm*
Routing/Redistribution layer (RDL) material/thickness	*RDL Copper 6 µm*
Passivation material	*Low temp Polyimide passivation – LTC9320*
Backside coating material/thickness	*Backside coating PET film 25 µm*
Package Moisture Sensitivity Level (JEDEC J-STD020D)	*1*

2.2.2 SIP assembly information

Table 2

Assembly Information	
SIP LGA 7.3x11 86L	
Assembly plant name / location	*ASE TAIWAN* *No.26, Chin 3rd Rd. Nantze, Kaohsiung, Taiwan*
Bill of Material elements	
Integrated Passive Device /frequency/reference	*IPD LPF 1016 2.4GHz MLPF-WB55-01E3 FLT1*
Microcontroller device/reference	*STM32WB55 WLCSP100 U1*
Substrate material/reference	*SUBSTRATE LGA 7.3X11 86L 4L ASE A27167*
Shielding sputtering/material/reference	*Shielding sputtering Cu 3500038111* *Shielding sputtering SUS 3500037111*
Lid material/reference	*M Lid MTL C7521 82.35 34.675 0.95 ASE 5600132101*
Ferrite bead/resistance/current/reference	*Ferrite Bead/600o/RDC 0.5o/1A PBY160808T-601Y-N*
Solder paste/reference	*Solder paste M705-WSG36-T6J ASE 2100151111*
Capacitor/voltage/capacity/reference	*CAP 0201 6.3V 100nF 10 T0.3 X5R GRM033R60J104KE19D* *CAP 0201 25V 100pF 10 T0.3 X7R GRM033R71E101KA01D* *CAP 0201 2P 25V 10pF 5 T0.3C0G GRM0335C1E100JA01D* *CAP 0402 6.3V 4.7uF 20 T0.5X5R GRM155R60J475ME47D*
Inductor/inductance/reference	*10uH inductor LQM18FN100M00D* *10nH inductor LQG15WZ10NJ02D* *2.2 nH inductor LQP03TN4N7H02D MUR* *4.7 nH inductor LQP03TN4N7H02D MUR*
Resistance/voltage/reference	*RES 0402 50V 10Kohm 1 T0.35 RC0402FR-0710KL*
Oscillator/supplier/reference	*TXC 1610 9H 32K768 9H03200030* *NDK NX2016 32M Crystal Oscillator*
Antena/supplier/reference	*Chip Antenna YAGEO ANT1608LL14R2400A*
Molding compound material/supplier/reference	*Molding Compound SMMT ASE 1801695101*
Package Moisture Sensitivity Level (JEDEC J-STD020D)	*3*

2.2.3 Reliability testing information

Table 3

Reliability Testing Information	
Reliability laboratory name / location	ST Rousset (France) / ST Muar (Malaysia)
	ASE Kaohsiung (Taiwan)

Note: ST is ISO 9001 certified. This induces certification of all internal and subcontractor labs.
ST certification document can be downloaded under the following link:
http://www.st.com/content/st_com/en/support/quality-and-reliability/certifications.html

3 TESTS RESULTS SUMMARY

3.1 Lot Information

Table 4

Lot #	Diffusion Lot / Wafer ID	Die Revision (Cut)	Assy Lot / Trace Code	Raw Line	Package	Note
1	9R847067	Cut 2.1	AA022146	E07D*495ESDY	SIP LGA 7.3x11 86L	Package Reliability assessment
2	9R920100	Cut 2.1	AA022145	E07D*495ESDY		Package Reliability assessment
3	9R920100	Cut 2.1	AA022145	E07D*495ESDY		Package Reliability assessment
4	9R847067	Cut 2.1	AA008087	E07D*495BLRY	SIP LGA 7.3x11 86L with Daisy Chain	Board Level reliability assessment
5	9R108B71	Cut 2.1	AA141256	E07D*495ESDY	SIP LGA 7.3x11 86L	Package Reliability assessment
6	9R127551	Cut 2.2	AA147090	E07D*495ESDX	SIP LGA 7.3x11 86L	Package Reliability assessment

3.2 Test plan and results summary

Table 5 – ACCELERATED LIFETIME SIMULATION TESTS

SIP LGA 7.3x11 86L, ASEKH

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
ESD HBM	ANSI/ESDA/ JEDEC JS-001	1500 Ω, 100 pF 2kV class2	3	3	9	Lot1: 0/3 Lot5: 0/3 Lot6: 0/3	
LatchUp	JESD78	130°C	3	3	9	Lot1: 0/3 Lot5: 0/3 Lot6: 0/3	

Table 6 – ACCELERATED ENVIRONMENT STRESS TESTS

SIP LGA 7.3x11 86L, ASEKH

Test code	Stress method	Stress Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments: (N/A =Not Applicable)
ESD CDM	ANSI/ESDA/ JEDEC JS-002	250V	1	3	3	Lot1: 0/3 Lot5: 0/3 Lot6: 0/3	
PC	J-STD-020	24hrs bake@125°C, MSL3 (192hrs@30C/60%RH) 3x Reflow simulation Peak Reflow Temp= 260°C	3	256	768	Lot1: 0/256 Lot2: 0/256 Lot3: 0/256 Lot5: 0/308 Lot6: 0/308	
TC	JESD22-A104	Ta=-65/150°C Duration= 500cyc ☒ After PC	3	77	231	Lot1: 0/77 Lot2: 0/77 Lot3: 0/77 Lot5: 0/77 Lot6: Q2'2022	
UHAST	JESD22-A118	Ta=130°C ,85% RH, 2 Atm Duration= 96hrs ☒ After PC	3	77	231	Lot1: 0/77 Lot2: 0/77 Lot3: 0/77 Lot5: 0/77 Lot6: Q2'2022	
HTSL	JESD 22-A103	Ta=150°C , Duration= 1000hrs ☒ After PC	3	77	231	Lot1: 0/77 Lot2: 0/77 Lot3: 0/77 Lot5: 0/77 Lot6: Q2'2022	
THB	JESD 22-A101	Ta=85°C/85%RH VDD=3v6 Duration= 500hrs ☒ After PC	3	25	75	Lot1: 0/25 Lot2: 0/25 Lot3: 0/25 Lot5: 0/77 Lot6: Q2'2022	

Note: Test method revision reference is the one active at the date of reliability trial execution

Table 7 - PACKAGE ASSEMBLY INTEGRITY TESTS

Test code	Method	Tests Conditions	Lots	S.S.	Total	Results/Lot Fail/S.S.	Comments:
CA	Construction Analysis including -POA -Solderability	JESD 22B102 JESDB100/ B108	4	50	200	Lot1: 0/50 Lot2: 0/50 Lot3: 0/50 Lot5: 0/50	ST internal report ref.: CA-01-0120 (lot1/lot2/lot3) CA-21-00039 (lot5)

Table 8 - BOARD LEVEL RELIABILITY

Test code	Method	Tests Conditions	Lot	S.S.	Total	Results/Lot Fail/S.S.	Comments:
Drop test	JESD22 - B111	Peak acceleration=1500g Pulse duration=0,5ms 30 drops	1	60	60	Lot4: 0/60	ASE report ref.: 5110-00-2020-07-047
TC	JESD22 - A104	Ta=-40/125°C Duration= 100cyc	1	30	30	Lot4: 0/30	ASE report ref.: 5110-00 2020-07-048

4 APPLICABLE AND REFERENCE DOCUMENTS

Reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits
SOP2.6.2	Internal Change Management
SOP2.6.7	Finished Good Maturity Management
SOP2.6.9	Package & Process Maturity Management in BE
SOP2.6.11	Program Management for Product Development
SOP2.6.19	Front-End Technology Platform Development and Qualification
DMS 0061692	Reliability Tests and Criteria for Product Qualification
ANSI/ESDA JEDEC JS-002	Electrostatic discharge (ESD) sensitivity testing charge device model (CDM)
JESD 22-A103	High Temperature Storage Life
JEDEC JS-001	Electrostatic discharge (ESD) sensitivity testing human body model (HBM)
JESD78	IC Latch-up test
J-STD-020:	Moisture/reflow sensitivity classification for non-hermetic solid state surface mount devices
JESD22-A113:	Preconditioning of non-hermetic surface mount devices prior to reliability testing
JESD22-A118:	Unbiased Highly Accelerated temperature & humidity Stress Test
JESD22-A104:	Temperature cycling
JESD22-A110:	Temperature Humidity Bake
JESD 22B102:	Solderability test
JESD22B100/B108:	Physical dimension
JESD22 - B111	Board Level Drop Test Method of Components for Handheld Electronic products
JESD22 - B104	Board Level Temperature Cycling Test

5 GLOSSARY

Reference	Short description
MCD	Microcontroller Division
IPD	Integrated Passive Device
PC	Preconditioning (solder simulation)
THB	Temperature Humidity Bias
TC	Temperature cycling
uHAST	Unbiased Highly Accelerated Stress Test
HTSL	High temperature storage life
DMS	ST Advanced Documentation Controlled system/ Documentation Management system
ESD CDM	Electrostatic discharge (charge device model)
ESD HBM	Electrostatic discharge (human body model)
LU	Latch-up
CA	Construction Analysis
BLR	Board Level Reliability

6 REVISION HISTORY

Revision	Author	Content description	Approval List			
			Function	Location	Name	Date
1.0	Gabin Bosco	Initial release	Division Quality Manager	RSST	Pascal NARCHE	16th Nov. 2020
			Division Back-End Quality Manager	RSST	Gisele SEUBE	16th Nov. 2020
2.0	Berengere Routier-Scappucci	Added PCN	Division Quality Manager	RSST	Pascal NARCHE	22nd Mar. 2022

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