LMK05028 Low-Jitter Dual-Channel Network Synchronizer Clock With EEPROM

1 Features

- Two Independent PLL Channels Featuring:
  - Jitter: 150-fs RMS for Outputs ≥ 100 MHz
  - Phase Noise: –112 dBc/Hz at 100-Hz Offset for 122.88 MHz
  - Hitless Switching: 50-ps Phase Transient With Phase Cancellation
  - Programmable Loop Bandwidth With Fastlock
  - Standards-Compliant Synchronization and Holdover Using a Low-Cost TCXO/OCXO
  - Any Input to Any Output Frequency Translation
- Four Reference Clock Inputs
  - Priority-Based Input Selection
  - Digital Holdover on Loss of Reference
- Eight Clock Outputs With Programmable Drivers
  - Up to Six Different Output Frequencies
  - AC-LVDS, AC-CML, AC-LVPECL, HCSL, and 1.8-V or 2.5-V LVCMOS Output Formats
- EEPROM/ROM for Custom Clocks on Power-Up(2)
- Flexible Configuration Options
  - 1 Hz (1 PPS) to 750 MHz on Input and Output
  - XO: 10 to 100 MHz, TCXO: 10 to 54 MHz
  - DCO Mode: < 1 ppt/Step for Fine Frequency and Phase Steering (IEEE 1588 Slave)
  - Zero Delay for Deterministic Phase Offset
  - Robust Clock Monitoring and Status
  - I^2C or SPI Interface
- Excellent Power Supply Noise Rejection (PSNR)
- 3.3-V Supply With 1.8-V, 2.5-V, or 3.3-V Outputs
- Industrial Temperature Range: –40°C to +85°C

2 Applications

- SyncE (G.8262), SONET/SDH (Stratum 3/3E, G.813, GR-1244, GR-253), IEEE 1588 PTP Slave Clock, or Optical Transport Network (G.709)
- Telecom and Enterprise Line Cards
- Wireless Base Station (BTS), Wireless Backhaul
- Test and Measurement, Broadcast Infrastructure, and Medical Ultrasound
- Jitter and Wander Attenuation, Precise Frequency Translation, and Low-Jitter Clock Generation for FPGA, DSP, ASIC, and CPU Devices

3 Description

The LMK05028 is a high-performance network synchronizer clock device that provides jitter cleaning, clock generation, advanced clock monitoring, and superior hitless switching performance to meet the stringent timing requirements of communications infrastructure and industrial applications. The device's low jitter and high PSNR reduce bit error rates (BER) in high-speed serial links.

The device has two PLL channels and generates up to eight output clocks with 150-fs RMS jitter. Each PLL domain can select from any four reference inputs to synchronize its outputs.

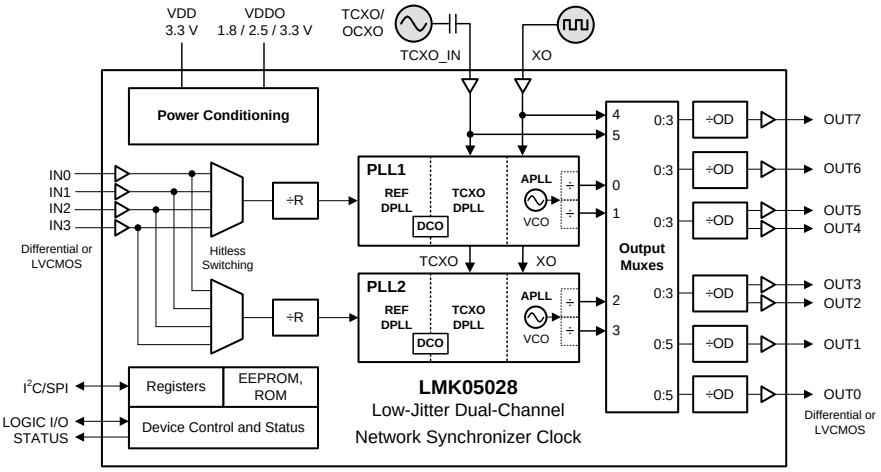
Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMK05028	VQFN (64)	9.00 mm × 9.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

(2) Contact TI Field Sales to inquire about custom factory pre-programmed devices.

Simplified Block Diagram



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4 Revision History

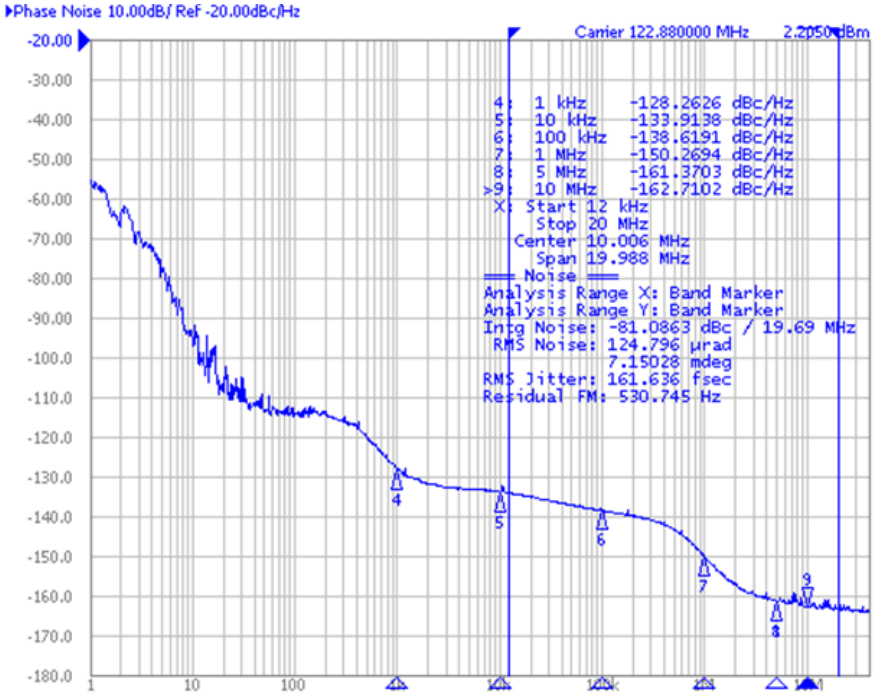
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (February 2018) to Revision A	Page
• Changed device status from Advanced Information to Production Data	1

5 Description (continued)

Each PLL channel supports programmable loop bandwidth for jitter and wander attenuation and fractional frequency translation for flexible frequency configuration. Synchronization options supported on each PLL channel includes hitless switching with phase cancellation, digital holdover, DCO mode with <1 ppt/step for precise clock steering (IEEE 1588 PTP slave), and zero-delay mode for deterministic input-to-output phase offset. The advanced reference input monitoring block ensures robust clock fault detection and helps to minimize output clock disturbance when a loss of reference (LOR) occurs.

The device can use a low-frequency TCXO/OCXO to determine the free-run or holdover frequency stability to maintain standards-compliant synchronization during LOR, or a standard XO when holdover frequency stability and wander are not critical. The device is fully programmable through I^2C or SPI interface and supports custom frequency configuration on power-up with the internal EEPROM or ROM. The EEPROM is factory pre-programmable and in-system programmable.

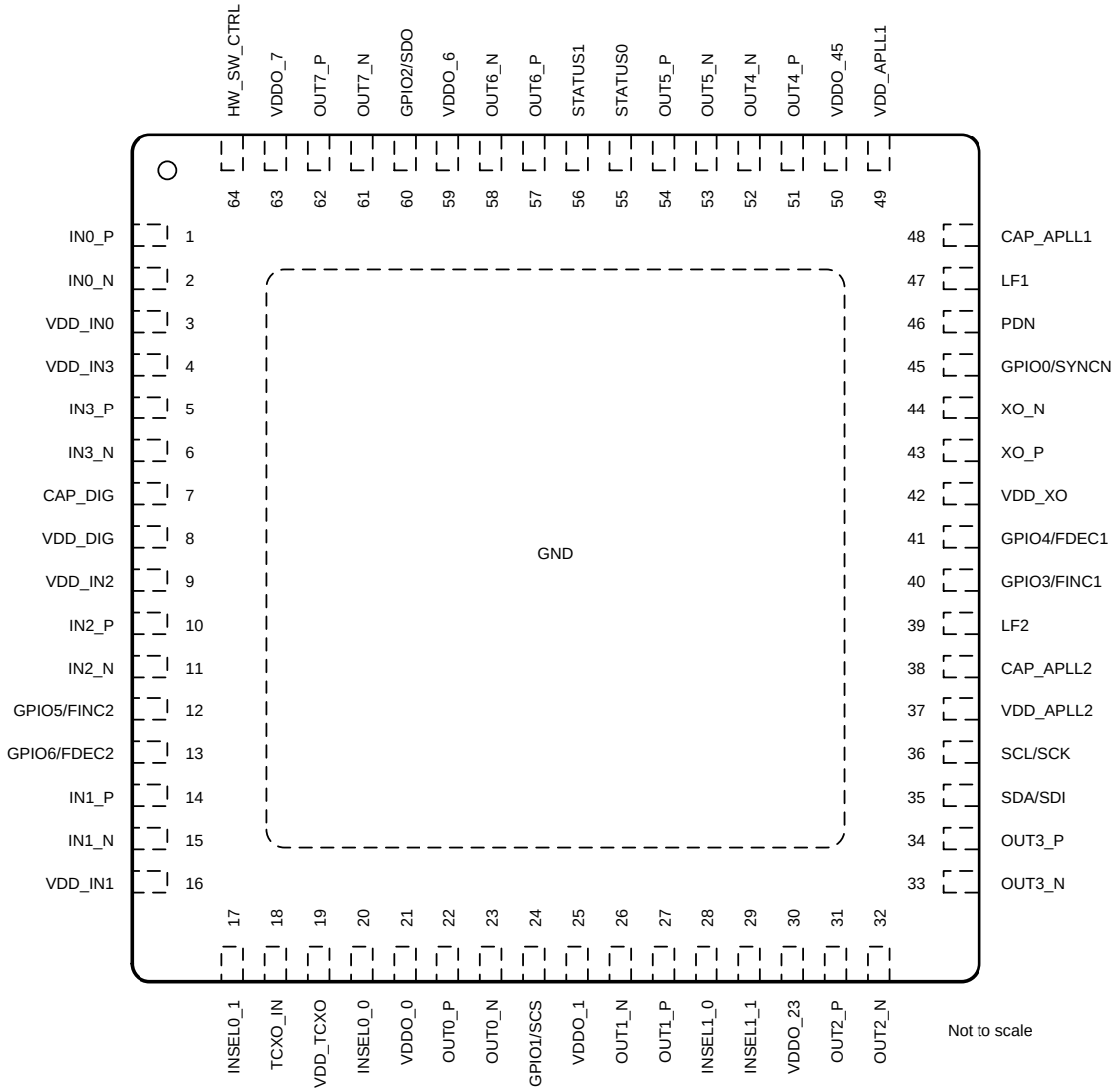


AC-LVPECL output, f_{IN} = 25 MHz, f_{TCXO} = 10 MHz (OCXO), f_{XO} = 48.0048 MHz, $f_{TCXO-TDC}$ = 20 MHz

Figure 1. 122.88-MHz Output Phase Noise (3-Loop)

6 Pin Configuration and Functions

RGC Package
64-Pin VQFN
Top View



Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
POWER			
GND	PAD	G	**Ground / Thermal Pad.** The exposed pad must be connected to PCB ground for proper electrical and thermal performance. A 7x7 via pattern is recommended to connect the IC ground pad to the PCB ground layers.
VDD_IN0	3	P	**Core Supply (3.3 V) for Reference Inputs 0 to 3.** Place a nearby 0.1-µF bypass capacitor on each pin.
VDD_IN1	16	P	
VDD_IN2	9	P	
VDD_IN3	4	P	

(1) G = Ground, P = Power, I = Input, O = Output, I/O = Input or Output, A = Analog.

Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
VDD_XO	42	P	**Core Supply (3.3 V) for XO and TCXO Inputs.** Place a nearby 0.1-µF bypass capacitor on each pin.
VDD_TCXO	19	P	
VDD_APLL1	49	P	**Core Supply (3.3 V) for PLL1, PLL2, and Digital Blocks.** Place a nearby 0.1-µF bypass capacitor on each pin.
VDD_APLL2	37	P	
VDD_DIG	8	P	
VDDO_0	21	P	**Output Supply (1.8, 2.5, or 3.3 V) for Clock Outputs 0 to 7.** Place a nearby 0.1-µF bypass capacitor on each pin.
VDDO_1	25	P	
VDDO_23	30	P	
VDDO_45	50	P	
VDDO_6	59	P	
VDDO_7	63	P	
CORE BLOCKS			
LF1	47	A	**External Loop Filter Capacitor for APLL1 and APLL2.** Place a nearby 0.1-µF capacitor on each pin.
LF2	39	A	
CAP_APLL1	48	A	**External Bypass Capacitors for APLL1, APLL2, and Digital Blocks.** Place a nearby 10-µF bypass capacitor on each pin.
CAP_APLL2	38	A	
CAP_DIG	7	A	
INPUT BLOCKS			
IN0_P	1	I	**DPLL Reference Clock Inputs 0 to 3.** Each input pair can accept a differential or single-ended clock signal for synchronizing the DPLLs. Each pair has a programmable input type with internal termination to support AC- or DC-coupled clocks. A single-ended LVCMOS clock can be applied to the P input with the N input pulled down to ground. An unused input pair can be left floating. LVCMOS input mode is recommended for input frequencies from 5 MHz down to 1 Hz (1 PPS or pulse-per-second).
IN0_N	2	I	
IN1_P	14	I	
IN1_N	15	I	
IN2_P	10	I	
IN2_N	11	I	
IN3_P	5	I	
IN3_N	6	I	
XO_P	43	I	**XO Input.** This input pair can accept a differential or single-ended clock signal from a low-jitter local oscillator to lock the APLLs. This input has a programmable input type with internal termination to support AC- or DC-coupled clocks. A single-ended LVCMOS clock (up to 2.5 V) can be applied to the P input with the N input pulled down to ground.
XO_N	44	I	
TCXO_IN	18	I	**TCXO Input.** This input can accept an AC-coupled sinewave, clipped-sinewave, or single-ended clock signal from a stable oscillator (TCXO/OCXO) to lock the TCXO-DPLL if used by a DPLL configuration. The input swing must be less than 1.3 Vpp before AC-coupling to the input pin, which has weak internal biasing of 0.6 V and no internal termination. Leave pin floating if unused.
OUTPUT BLOCKS			
OUT0_P	22	O	**Clock Outputs 0 to 3 Bank.** Each programmable output driver pair can support AC-LVDS, AC-CML, AC-LVPECL, HCSL, or 1.8/2.5-V LVCMOS clocks (one or two per pair). Unused differential outputs should be terminated if active or left floating if disabled through registers. The OUT[0:3] bank requires at least one clock from the PLL2 domain if enabled. This bank is preferred for PLL2 clocks to minimize output crosstalk.
OUT0_N	23	O	
OUT1_P	27	O	
OUT1_N	26	O	
OUT2_P	31	O	
OUT2_N	32	O	
OUT3_P	34	O	
OUT3_N	33	O	

Pin Functions (continued)

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
OUT4_P	51	O	**Clock Outputs 4 to 7 Bank.** Each programmable output driver pair can support AC-LVDS, AC-CML, AC-LVPECL, HCSL, or 1.8/2.5-V LVCMOS clocks (one or two per pair). Unused differential outputs should be terminated if active or left floating if disabled through registers. The OUT[4:7] bank requires at least one clock from the PLL1 domain. This bank is preferred for PLL1 clocks to minimize output crosstalk.
OUT4_N	52	O	
OUT5_P	54	O	
OUT5_N	53	O	
OUT6_P	57	O	
OUT6_N	58	O	
OUT7_P	62	O	
OUT7_N	61	O	
LOGIC CONTROL / STATUS (2)(3)			
HW_SW_CTRL	64	I	**Device Start-Up Mode Select** (3-level, 1.8-V compatible). This input selects the device start-up mode that determines the memory page used to initialize the registers, serial interface, and logic pin functions. The input level is sampled only at device power-on reset (POR). See Table 1 for start-up mode descriptions and logic pin functions.
PDN	46	I	**Device Power-Down** (active low). When PDN is pulled low, the device is in hard reset and all blocks including the serial interface are powered down. When PDN is pulled high, the device is started according to device mode selected by HW_SW_CTRL and begins normal operation with all internal circuits reset to their initial state.
SDA/SDI	35	I/O	**I²C Serial Data I/O (SDA) or SPI Serial Data Input (SDI).** See Table 1. The default 7-bit I²C address is 11000xxb, where the MSB bits (11000b) are initialized from on-chip EEPROM and the LSB bits (xxb) are determined by the logic input pins. When HW_SW_CTRL is 0, the LSBs are determined by the GPIO[2:1] input levels during POR. When HW_SW_CTRL is 1, the LSBs are fixed to 00b.
SCL/SCK	36	I	**I²C Serial Clock Input (SCL) or SPI Serial Clock Input (SCK).** See Table 1.
GPIO0/SYNCN	45	I	**Multifunction Inputs or Outputs.** See Table 1.
GPIO1/SCS	24	I	
GPIO2/SDO	60	I/O	
GPIO3/FINC1	40	I	
GPIO4/FDEC1	41	I	
GPIO5/FINC2	12	I/O	
GPIO6/FDEC2	13	I/O	
STATUS1	56	I/O	**Status Outputs [1:0].** Each output has programmable status signal selection, driver type (3.3-V LVCMOS or open-drain), and status polarity. Open-drain requires an external pullup resistor. Leave pin floating if unused.
STATUS0	55	I/O	
INSEL0_1	17	I	**Manual Reference Input Selection for DPLL1.** INSEL0_[1:0] = 00b (IN0), 01b (IN1), 10b (IN2), or 11b (IN3). Leave pin floating if unused.
INSEL0_0	20	I	
INSEL1_1	29	I	**Manual Reference Input Selection for DPLL2.** INSEL1_[1:0] = 00b (IN0), 01b (IN1), 10b (IN2), or 11b (IN3). Leave pin floating if unused.
INSEL1_0	28	I	

(2) Internal resistors: PDN pin has 200-kΩ pullup to VDD. Each HW_SW_CTRL, GPIO, and STATUS pin has a 150-kΩ bias to V_{IM} (approximately 0.8 V) when PDN = 0 or 400-kΩ pulldown when PDN = 1. Each INSEL pin has an 85-kΩ pullup to 1.8 V when PDN = 0 or 400-kΩ pulldown when PDN = 1.
(3) Unless otherwise noted: Logic inputs are 2-level, 1.8-V compatible inputs. Logic outputs are 3.3-V LVCMOS levels.

6.1 Device Start-Up Modes

The HW_SW_CTRL input pin selects the device start-up mode that determines the memory page used to initialize the registers, serial interface, and logic pin functions at power-on reset. The initial register settings determine the device's frequency configuration stored in the internal EEPROM (NVM) or ROM. After start-up, the device registers can be accessed through the selected serial interface for device status monitoring or programming, and the logic pins will function as defined by the mode configuration.

Table 1. Device Start-Up Modes

HW_SW_CTRL INPUT LEVEL(1)	START-UP MODE	MODE DESCRIPTION
0	EEPROM + I^2C (Soft pin mode)	Registers are initialized from EEPROM, and I^2C interface is enabled. Logic pins: • SDA, SCL: I^2C Data, I^2C Clock (open-drain). Pins require external pullups > 1 kΩ. • GPIO0: Output SYNC Input (active low). Tie pin high externally if not used. • GPIO[2:1](1): I^2C Address LSB Select Input (00, 01, 10, 11b) • GPIO[4:3](2): DPLL1 DCO Frequency Decrement and Increment Inputs (active high) • GPIO[6:5](2)(3): DPLL2 DCO Frequency Decrement and Increment Inputs (active high), or Status Outputs
Float (V_{IM})	EEPROM + SPI (Soft pin mode)	Registers are initialized from EEPROM, and SPI interface is enabled. Logic pins: • SDA, SCL: SPI Data Input (SDI), SPI Clock (SCK) • GPIO1: SPI Chip Select (SCS) • GPIO2: SPI Data Output (SDO) • GPIO[6:3, 0]: Same as for HW_SW_CTRL = 0
1	ROM + I^2C (Hard pin mode)	Registers are initialized from the ROM page selected by GPIO pins, and I^2C interface is enabled. Logic pins: • SDA, SCL: I^2C Data, I^2C Clock (open-drain). Pins require external pullups > 1 kΩ. • GPIO[3:0](1): ROM Page Select Input (0000 to 1111b) • GPIO[6:5](3): Status Outputs • GPIO4: Not used during POR After POR, GPIO[6:3] can function the same as for HW_SW_CTRL = 0 if enabled by registers.

(1) The input levels on these pins are sampled only during POR.
(2) These GPIO pins are only functional when the DCO feature and FINC/FDEC pin controls are enabled by registers.
(3) As status outputs, the GPIO[6:5] pins have the same configuration options as the STATUS[1:0] pins.

NOTE

To ensure proper start-up into EEPROM + SPI Mode, the HW_SW_CTRL, STATUS0, and STATUS1 pins must all be floating or biased to V_{IM} (0.8-V typical) before the PDN pin is pulled high. These three pins momentarily operate as 3-level inputs and get sampled at the low-to-high transition of PDN to determine the device start-up mode during POR. If any of these pins are connected to a host device (MCU or FPGA), TI recommends using external biasing resistors on each pin (10-kΩ pullup to 3.3 V with 3.3-kΩ pulldown to GND) to set the inputs to V_{IM} during POR. After power-up, the STATUS pins can operate as LVCMOS outputs to overdrive the external resistor bias for normal status operation.

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
VDD(2)	Core supply voltages	-0.3	3.6	V
VDDO(3)	Output supply voltages	-0.3	3.6	V
V_{IN}	Input voltage range for clock and logic inputs	-0.3	VDD+0.3	V
V_{OUT_LOGIC}	Output voltage range for logic outputs	-0.3	VDD+0.3	V
V_{OUT}	Output voltage range for clock outputs	-0.3	VDDO+0.3	V
T_j	Junction temperature		150	°C
T_{stg}	Storage temperture range	-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) VDD refers to all core supply pins or voltages. All VDD core supplies should be powered-on before the PDN is pulled high to trigger the internal power-on reset (POR).
(3) VDDO refers to all output supply pins or voltages. VDDO_x refers to the output supply for a specific output channel, where x denotes the channel index.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDD(1)	Core supply voltages	3.135	3.3	3.465	V
VDDO_x(2)	Output supply voltage for AC-LVDS/CML/LVPECL or HCSL driver	1.71	1.8, 2.5, 3.3	3.465	V
VDDO_x(2)	Output supply voltage for 1.8-V LVCMOS driver(3)	1.71	1.8	1.89	V
VDDO_x(2)	Output supply voltage for 2.5-V LVCMOS driver(3)	2.375	2.5	2.625	V
V_{IN}	Input voltage range for clock and logic inputs	0		3.465	V
T_J	Junction temperature			135	°C
t_{VDD}	Power supply ramp time(4)	0.01		100	ms
n_{EEcyc}	EEPROM program cycles(5)			100	cycles
SR_{OUT}	Output slew rate mode(6)		Fast		-

(1) VDD refers to all core supply pins or voltages. All VDD core supplies should be powered-on before internal power-on reset (POR).
(2) VDDO refers to all output supply pins or voltages. VDDO_x refers to the output supply for a specific output channel, where x denotes the channel index.
(3) The LVCMOS driver supports full rail-to-rail swing when VDDO_x is 1.8 V or 2.5 V ±5%. When VDDO_x is 3.3 V, the LVCMOS driver will not fully swing to the positive rail due to the dropout voltage of the output channel's internal LDO regulator.
(4) Time for VDD to ramp monotonically above 2.7 V for proper internal power-on reset. For slower or non-monotonic VDD ramp, hold PDN low until after VDD voltages are valid.
(5) n_{EEcyc} specifies the maximum EEPROM program cycles allowed for customer programming. The initial count of factory-programmed cycles is non-zero due to production tests, but factory-programmed cycles are excluded from the n_{EEcyc} limit. The total number of EEPROM program cycles can be read from the 8-bit NVM count status register (NVMCNT), which automatically increments by 1 on each successful programming cycle. TI does not ensure EEPROM endurance if the n_{EEcyc} limit is exceeded by the customer.
(6) Clock output characteristics are specified for all driver types with the output slew rate mode programmed to Fast. Some specifications may not be met with the output slew rate programmed to Nominal.

7.4 Thermal Information

THERMAL METRIC[1] [2] [3]		LMK05028 RGC (VQFN) 64 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	20.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	6.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	4.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	4.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) The thermal information is based on a 10-layer 200 mm x 250 mm board with 49 thermal vias (7 x 7 pattern, 0.3 mm holes).
(3) Ψ_{JB} can allow the system designer to measure the board temperature (T_{PCB}) with a fine-gauge thermocouple and back-calculate the device junction temperature, $T_J = T_{PCB} + (\Psi_{JB} \times \text{Power})$. Measurement of Ψ_{JB} is defined by JESD51-6.

7.5 Electrical Characteristics

Over Recommended Operating Conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Supply Characteristics						
IDD_IN0, IDD_IN1, IDD_IN3	Core Supply Current (VDD_INx)			3.5	10	mA
IDD_IN2	Core Supply Current (VDD_IN2)			6	14	mA
IDD_XO	Core Supply Current (VDD_XO)			25	33	mA
IDD_TCXO	Core Supply Current (VDD_TCXO)	Configuration A[1]		1	4	mA
		Configuration B[2]		6	9	mA
IDD_PLL1	Core Supply Current (VDD_PLL1)	Configuration A[1]		160	188	mA
		Configuration B[2]		185	217	mA
IDD_PLL2	Core Supply Current (VDD_PLL2)	Configuration A[1]		138	160	mA
		Configuration B[2]		160	187	mA
IDD_DIG	Core Supply Current (VDD_DIG)	Configuration A[1]		34	59	mA
		Configuration B[2]		42	70	mA
IDDO_x	Output Supply Current[3] (VDDO_x = 3.3 V ± 5%)	AC-LVDS		22	28	mA
		AC-CML		24	32	mA
		AC-LVPECL		27	34	mA
		HCSL		33	42	mA
IDDO_x	Output Supply Current[4] (VDDO_x = 3.3 V ± 5%)	AC-LVDS (x2)		32	40	mA
		AC-CML (x2)		37	45	mA
		AC-LVPECL (x2)		41	51	mA
		HCSL (x2)		55	67	mA
IDD_{PDN}	Total Supply Current (all VDD and VDDO pins, 3.3 V)	Device powered-down (PDN pin held low)		40		mA

(1) Configuration A (All blocks on except TCXO_IN and both TCXO-DPLLs): $f_{IN[0:3]}$ = 25 MHz, f_{XO} = 48.0048 MHz, TCXO_IN disabled. Both DPLL[1:2] in 2-loop mode, f_{VCO1} = 5 GHz, f_{VCO2} = 5.5296 GHz, PLL1_P1 = 8, PLL2_P1 = 9.
(2) Configuration B (All blocks on): $f_{IN[0:3]}$ = 25 MHz, f_{XO} = 48.0048 MHz, f_{TCXO} = 10 MHz. Both DPLL[1:2] in 3-loop mode, f_{VCO1} = 5 GHz, f_{VCO2} = 5.5296 GHz, PLL1_P1 = 8, PLL2_P1 = 9.
(3) IDDO_x includes supply current for output divider and one output driver with f_{OUT} = 156.25 MHz or 122.88 MHz.
(4) IDDO_x includes supply current for output divider and two output drivers with f_{OUT} = 156.25 MHz or 122.88 MHz.

Electrical Characteristics (continued)

Over Recommended Operating Conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Reference Input Characteristics (INx)						
f_{IN}	Input frequency range(5)	Differential input(6)	5		750	MHz
		LVCMOS input	1E-6		250	
V_{IN-SE}	Single-ended input voltage swing	LVCMOS input, DC-coupled to INx_P	1			V
V_{IDpp}	Differential input voltage swing, peak-peak ($\|V_P - V_N\|$)(7)	Differential input	0.4		2	V
dV/dt	Input slew rate(5)		0.2			V/ns
I_{IN}	Input leakage	50-Ω and 100-Ω internal terminations disabled	-350		350	µA
C_{IN}	Input capacitance	Single-ended, each pin		2		pF
XO Input Characteristics (XO)						
f_{CLK}	Input frequency range(5)		10		100	MHz
V_{IN-SE}	Single-ended input voltage swing	LVCMOS input, DC-coupled to XO_P	1		2.6	V
V_{IDpp}	Differential input voltage swing, peak-peak ($\|V_P - V_N\|$)(7)	Differential input	0.4		2	V
dV/dt	Input slew rate(5)		0.2			V/ns
IDC	Input duty cycle		40		60	%
I_{IN}	Input leakage	50-Ω and 100-Ω internal terminations disabled	-350		350	µA
C_{IN}	Input capacitance	Single-ended, each pin		1		pF
TCXO/OCXO Input Characteristics (TCXO_IN)						
f_{TCXO}	Input frequency(5)		10		54	MHz
V_{IN}	Input voltage swing	AC-coupled	0.8		1.3	V
V_{BIAS}	Input bias voltage	Weak internal bias		0.6		V
dV/dt	Input slew rate(5)		0.2			V/ns
IDC	Input duty cycle		40		60	%
C_{IN}	Input capacitance			10		pF
APLL/VCO Charateristics						
f_{VCO1}	VCO1 Frequency range		4.8		5.4	GHz
f_{VCO2}	VCO2 Frequency range		5.5		6.2	GHz

(5) Parameter is specified by characterization and is not tested in production.
(6) For a differential input clock below 5 MHz, TI recommends to disable the differential input amplitude monitor and enable at least one other monitor (frequency, window detectors) to validate the input clock. Otherwise, consider using an LVCMOS clock for an input below 5 MHz.
(7) Minimum limit applies for the minimum setting of the differential input amplitude monitor.

Electrical Characteristics (continued)

Over Recommended Operating Conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
1.8-V LVCMOS Output Characteristics (OUTx)						
f_{OUT}	Output frequency(5)		1E-6		200	MHz
V_{OH}	Output high voltage	I_{OH} = 1 mA	1.2			V
V_{OL}	Output low voltage	I_{OL} = 1 mA			0.4	V
I_{OH}	Output high current			-23		mA
I_{OL}	Output low current			24		mA
t_R/t_F	Output rise/fall time(5)	20% to 80%		250		ps
t_{SK}	Output-to-output skew(5)	Same post divider, output divide values, and output type			100	ps
		Same post divider, output divide values, LVCMOS-to-DIFF			1.5	ns
PN_{FLOOR}	Output phase noise floor (f_{OFFSET} > 10 MHz)	66.66 MHz		-155		dBc/Hz
ODC	Output duty cycle(5) (8)		45		55	%
R_{OUT}	Output impedance			50		Ω
2.5-V LVCMOS Output Characteristics (OUTx)						
f_{OUT}	Output frequency(5)		1E-6		200	MHz
V_{OH}	Output high voltage	I_{OH} = 1 mA	1.9			V
V_{OL}	Output low voltage	I_{OL} = 1 mA			0.525	V
I_{OH}	Output high current			-48		mA
I_{OL}	Output low current			55		mA
t_R/t_F	Output rise/fall time(5)	20% to 80%		250		ps
t_{SK}	Output-to-output skew(5)	Same post divider, output divide values, and output type			100	ps
		Same post divider, output divide values, LVCMOS-to-DIFF			1.5	ns
PN_{FLOOR}	Output phase noise floor (f_{OFFSET} > 10 MHz)	66.66 MHz		-155		dBc/Hz
ODC	Output duty cycle(5) (8)		45		55	%
R_{OUT}	Output impedance			50		Ω
AC-LVDS Output Characteristics (OUTx)						
f_{OUT}	Output frequency(5) (9)				750	MHz
V_{OD}	Output voltage swing (V_{OH} - V_{OL})	f_{OUT} > 25 MHz	250	400	450	mV
V_{ODpp}	Differential output voltage swing, peak-to-peak			2×V_{OD}		V
V_{OS}	Output common mode		100		430	mV
t_{SK}	Output-to-output skew(5)	Same post divider, output divide values, and output type			100	ps
t_R/t_F	Output rise/fall time(5)	20% to 80%, < 300 MHz		225	350	ps
		± 100 mV around center point, ≥ 300 MHz		75	150	ps
PN_{FLOOR}	Output phase noise floor (f_{OFFSET} > 10 MHz)	156.25 MHz		-160		dBc/Hz
ODC	Output duty cycle(5) (8)		45		55	%

(8) Parameter is specified for PLL outputs divided from either VCO domain.
(9) An output frequency over the f_{OUT} max spec is possible, but the output swing may be less than the V_{OD} min spec.

Electrical Characteristics (continued)

Over Recommended Operating Conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC-CML Output Characteristics (OUTx)						
f_{OUT}	Output frequency(5) (9)				750	MHz
V_{OD}	Output voltage swing (V_{OH} - V_{OL})		400	600	800	mV
V_{ODpp}	Differential output voltage swing, peak-to-peak			2×V_{OD}		V
V_{OS}	Output common mode		150		550	mV
t_{SK}	Output-to-output skew(5)	Same post divider, output divide values, and output type			100	ps
t_R/t_F	Output rise/fall time(5)	20% to 80%, < 300 MHz		150	300	ps
		± 100 mV around center point, ≥ 300 MHz		50	125	ps
PN_{FLOOR}	Output duty cycle(5) (8)	156.25 MHz		-160		dBc/Hz
ODC	Output duty cycle(5)		45		55	%
AC-LVPECL Output Characteristics (OUTx)						
f_{OUT}	Output frequency(5) (9)				750	MHz
V_{OD}	Output voltage swing (V_{OH} - V_{OL})		500	850	1000	mV
V_{ODpp}	Differential output voltage swing, peak-to-peak			2×V_{OD}		V
V_{OS}	Output common mode		0.3		0.7	V
t_{SK}	Output-to-output skew(5)	Same post divider, output divide values, and output type			100	ps
t_R/t_F	Output rise/fall time(5)	20% to 80%, < 300 MHz		150	300	ps
		± 100 mV around center point, ≥ 300 MHz		25	100	ps
PN_{FLOOR}	Output phase noise floor (f_{OFFSET} > 10 MHz)	156.25 MHz		-162		dBc/Hz
ODC	Output duty cycle(5) (8)		45		55	%
HCSL Output Characteristics (OUTx)						
f_{OUT}	Output frequency(5) (9)				400	MHz
V_{OH}	Output high voltage		600		880	mV
V_{OL}	Output low voltage		-150		150	mV
t_{SK}	Output-to-output skew(5)	Same post divider, output divide values, and output type			100	ps
dV/dt	Output slew rate(5)	Measured from -150 mV to +150 mV on the differential waveform	2.5		6	V/ns
PN_{FLOOR}	Output phase noise floor (f_{OFFSET} > 10 MHz)	100 MHz		-158		dBc/Hz
ODC	Output duty cycle(5) (8)	100 MHz	45		55	%
3-Level Logic Input Characteristics (HW_SW_CTRL, STATUS[1:0])						
V_{IH}	Input high voltage		1.4			V
V_{IM}	Input mid voltage	Input floating with internal bias and PDN pulled low	0.7		0.9	V
V_{IL}	Input low voltage				0.4	V
I_{IH}	Input high current	V_{IH} = VDD	-40		40	µA
I_{IL}	Input low current	V_{IL} = GND	-40		40	µA
C_{IN}	Input capacitance			2		pF

Electrical Characteristics (continued)

Over Recommended Operating Conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
2-Level Logic Input Characteristics (PDN, GPIO[6:0], SDI, SCK, SCS, INSELx_[1:0])						
V_{IH}	Input high voltage		1.2			V
V_{IL}	Input low voltage				0.6	V
I_{IH}	Input high current	V_{IH} = VDD	-40		40	µA
I_{IL}	Input low current	V_{IL} = GND	-40		40	µA
C_{IN}	Input capacitance			2		pF
Logic Output Characteristics (STATUS[1:0], GPIO[6:5], SDO)						
V_{OH}	Output high voltage	I_{OH} = 1 mA	1.2			V
V_{OL}	Output low voltage	I_{OL} = 1 mA			0.6	V
t_R/t_F	Output rise/fall time	20% to 80%, LVCMOS mode, 1 kΩ to GND		500		ps
SPI Timing Requirements (SDI, SCK, SCS, SDO)						
f_{SCK}	SPI clock rate				20	MHz
t_1	SCS to SCK setup time		10			ns
t_2	SDI to SCK setup time		10			ns
t_3	SDI to SCK hold time		10			ns
t_4	SCK high time		25			ns
t_5	SCK low time		25			ns
t_6	SCK to SDO valid read-back data		10			ns
t_7	SCS pulse width		20			ns
t_8	SDI to SCK hold time		10			ns
I^2C Interface Characteristics (SDA, SCL)						
V_{IH}	Input high voltage		1.2			V
V_{IL}	Input low voltage				0.5	V
I_{IH}	Input leakage		-15		15	µA
C_{IN}	Input capacitance			2		pF
V_{OL}	Output low voltage	I_{OL} = 3 mA			0.3	V
f_{SCL}	I^2C clock rate	Standard			100	kHz
		Fast mode			400	kHz
$t_{SU(START)}$	START condition setup time	SCL high before SDA low	0.6			µs
$t_{H(START)}$	START condition hold time	SCL low after SDA low	0.6			µs
$t_{W(SCLH)}$	SCL pulse width high		0.6			µs
$t_{W(SCLL)}$	SCL pulse width low		1.3			µs
$t_{SU(SDA)}$	SDA setup time		100			ns
$t_{H(SDA)}$	SDA hold time	SDA valid after SCL low	0		0.9	µs
$t_{R(IN)}$	SDA/SCL input rise time				300	ns
$t_{F(IN)}$	SDA/SCL input fall time				300	ns
$t_{F(OUT)}$	SDA output fall time	C_{BUS} ≤ 400 pF			300	ns
$t_{SU(STOP)}$	STOP condition setup time		0.6			µs
t_{BUS}	Bus free time between STOP and START		1.3			µs

Electrical Characteristics (continued)

Over Recommended Operating Conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Other Characteristics						
t_{PHO}	Input-to-output phase offset	Zero delay mode		2		ns
PSNR	Spur induced by power supply noise (V_N = 50 mVpp)(10) (11)	VDDO_x = 2.5 V or 3.3 V, AC-DIFF or HCSL output		-70		dBc
		VDDO_x = 2.5 V, LVCMOS output		-55		
PSNR	Spur induced by power supply noise (V_N = 25 mVpp)(10) (11)	VDDO_x = 1.8 V, AC-DIFF or HCSL output		-70		
		VDDO_x = 1.8 V, LVCMOS output		-45		
SPUR	Spur level due to output-to-output crosstalk (adjacent channels)(11)	f_{OUTx} = 156.25 MHz, f_{OUTy} = 155.52 MHz, AC-DIFF or HCSL (same output type for both channels)		-75		dBc
PLL Clock Output Performance Characteristics						
RJ	RMS phase jitter (12 kHz to 20 MHz)	156.25 MHz AC-DIFF or HCSL output, f_{XO} = 48.0048 MHz		150	250	fs RMS
PN_{TDC}	Output close-in phase noise (f_{OFFSET} = 100 Hz)	122.88 MHz AC-DIFF or HCSL, 3-loop mode, f_{XO} = 48.0048 MHz, f_{TCXO} = 10 MHz, $f_{TCXO-TDC}$ = 20 MHz, BW_{REF} = 5 Hz, BW_{TCXO} = 400 Hz		-112		dBc/Hz
BW	DPLL bandwidth range(12)	Programmed bandwidth setting		0.01 to 4000		Hz
J_{PK}	DPLL closed-loop jitter peaking(13)	f_{IN} = 25 MHz, f_{OUT} = 10 MHz, DPLL BW = 0.1 Hz or 10 Hz		0.1		dB
J_{TOL}	Jitter tolerance	Jitter modulation = 10 Hz, 25.78125 Gbps		6455		UI p-p
$t_{HITLESS}$	Phase transient during hitless switch	Valid for a single switchover event between two clock inputs at the same frequency		± 50		ps
$f_{HITLESS}$	Frequency transient during hitless switch	Valid for a single switchover event between two clock inputs at the same frequency		± 10		ppb
$t_{STARTUP}$	Initial PLL clock start-up time(14)	From rising edge of PDN to free-running output clocks		20		ms

(10) PSNR is the single-sideband spur level (in dBc) measured when sinusoidal noise with ampitude V_N and frequency between 100 kHz and 1 MHz is injected onto VDD and VDDO_x pins.
(11) DJ_{SPUR} (ps pk-pk) = [2 × $10^{(dBc/20)}$ / (π × f_{OUT}) × 1E6], where dBc is the PSNR or SPUR level (in dBc) and f_{OUT} is the output frequency (in MHz).
(12) Actual loop bandwidth may be lower. Applies to REF-DPLL and TCXO-DPLL. The valid loop bandwidth range may be constrained by the DPLL loop mode and REF-TDC and/or TCXO-TDC frequencies used in a given configuration.
(13) The TICS Pro software configures the closed-loop jitter peaking for 0.1 dB or less based on the programmed DPLL bandwidth setting.
(14) Assumes XO input clock is stable in frequency and amplitude before rising edge of PDN, PLLs start-up using parallel calibration mode, VCO wait timers set to 0.4 ms, PLL wait timers set to 3 ms, and outputs auto-mute during APLL lock only (DPLL auto-mute options disabled).

7.6 Timing Diagrams

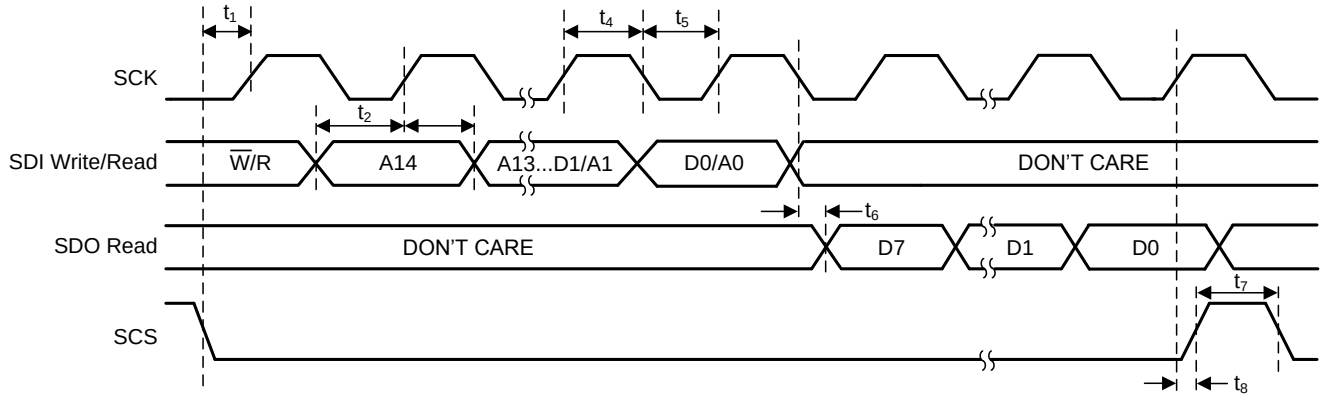


Figure 2. SPI Timing Parameters

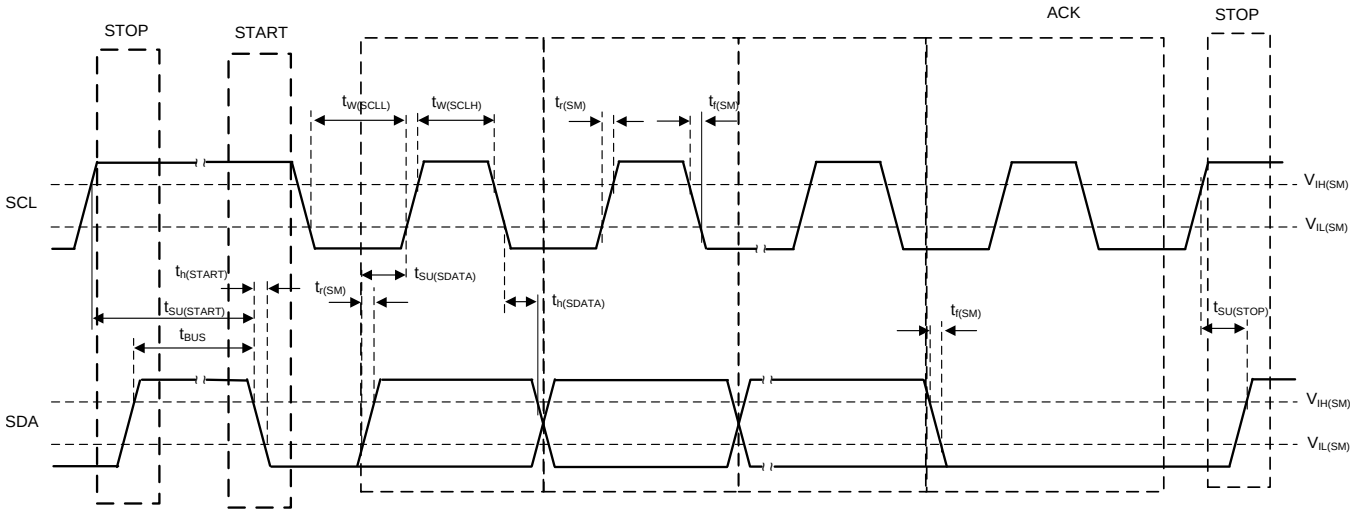


Figure 3. I²C Timing Diagram

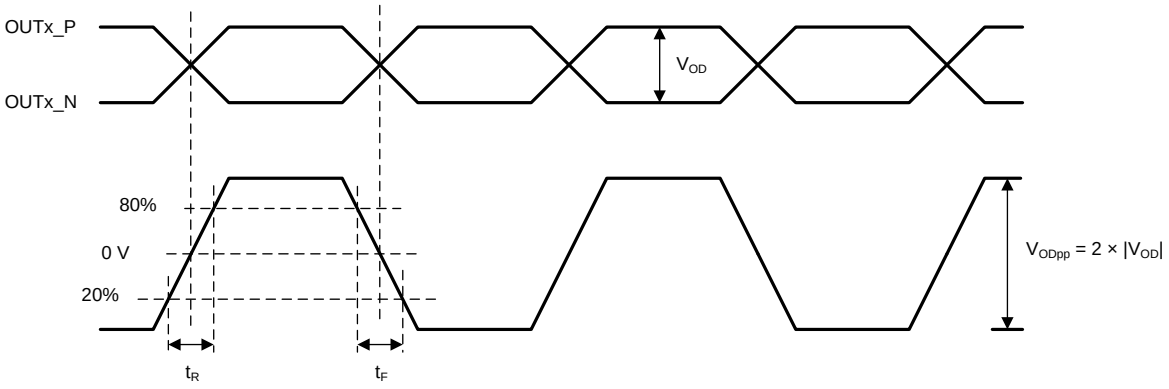


Figure 4. Differential Output Voltage and Rise/Fall Time

Timing Diagrams (continued)

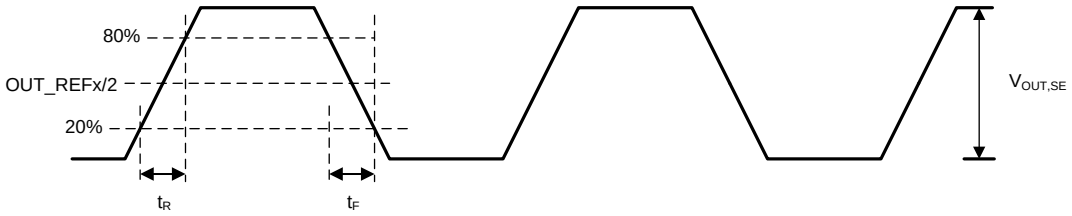


Figure 5. Single-Ended Output Voltage and Rise/Fall Time

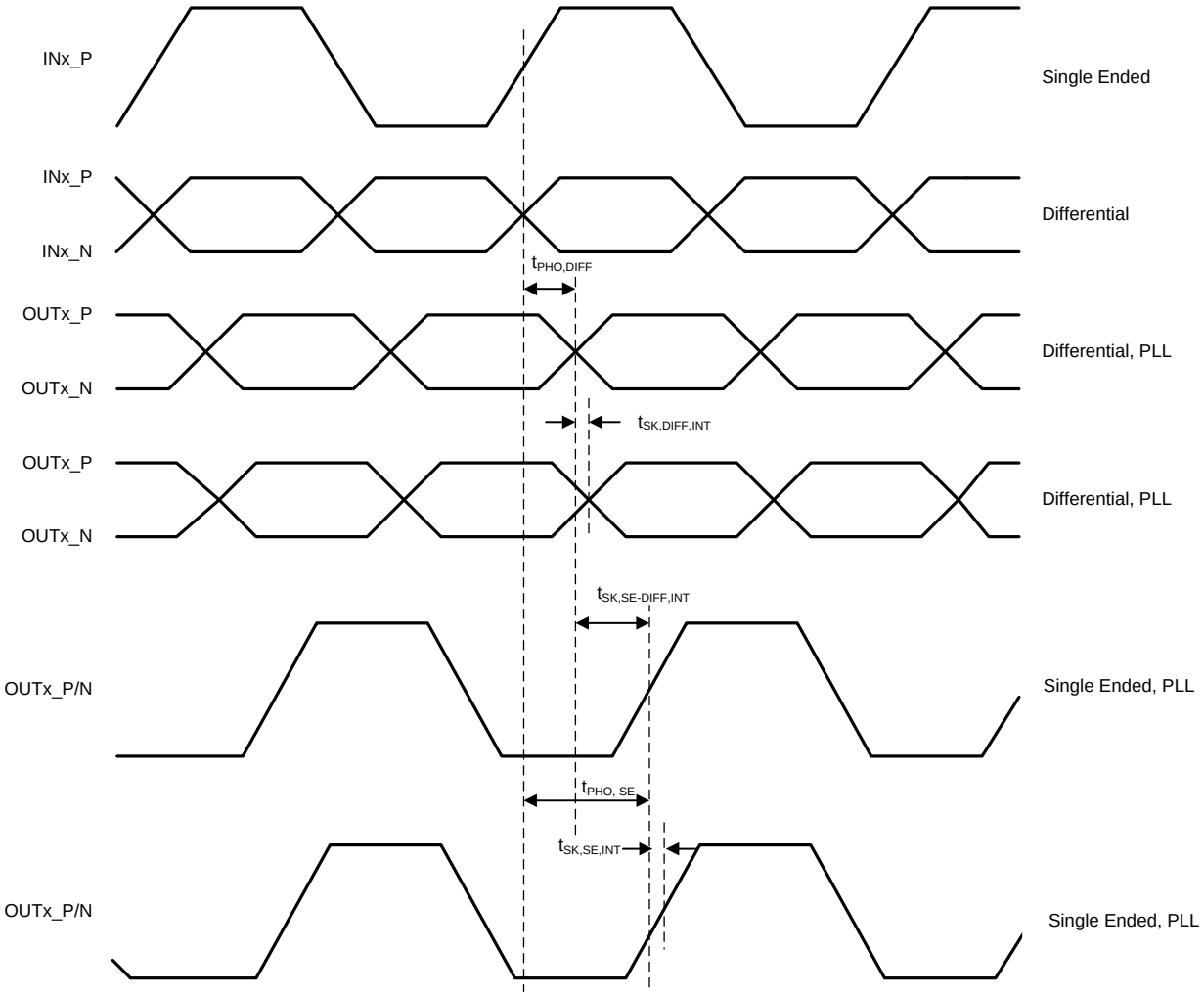
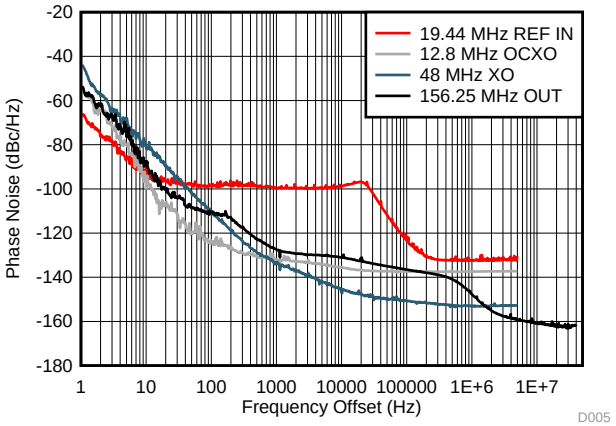


Figure 6. Differential and Single-Ended Output Skew and Phase Offset

7.7 Typical Characteristics

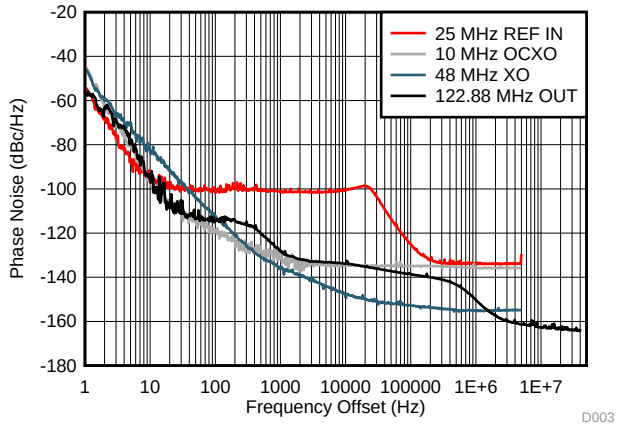
Unless otherwise noted: VDD = 3.3 V, VDDO = 1.8 V, T_A = 25°C, BW_{APLL} = 500 kHz, AC-LVPECL output.

The PLL output clock phase noise at different frequency offsets are determined by different noise contributors, such as external clock input sources (REF IN, OCXO, XO) and internal noise sources (PLL, VCO), as well as the configured PLL loop bandwidths ($BW_{REF-DPLL}$, $BW_{TCXO-DPLL}$, BW_{APLL}). The phase noise profile shown for each external clock source (f_{SOURCE}) was normalized to the PLL output frequency (f_{OUT}) by adding $20\times LOG_{10}(f_{OUT} / f_{SOURCE})$ to the measured source's phase noise.



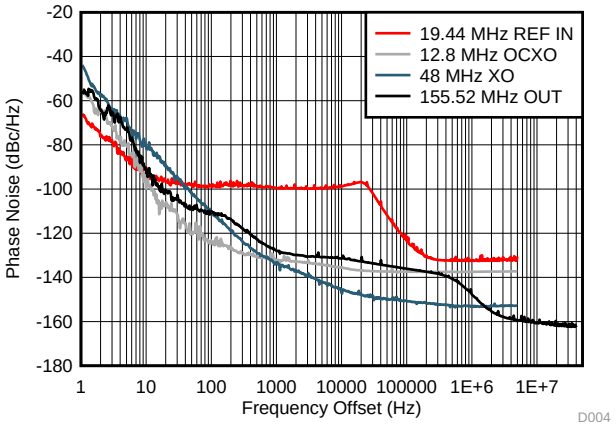
Output Phase Jitter = 175-fs RMS (12 kHz to 20 MHz)
f_{IN} = 25 MHz, f_{TCXO} = 10 MHz (OCXO), f_{XO} = 48.0048 MHz,
$f_{TCXO-TDC}$ = 20 MHz, $BW_{REF-DPLL}$ = 4 Hz, $BW_{TCXO-DPLL}$ = 200 Hz

Figure 7. 156.25-MHz Output Phase Noise (3-Loop) With Phase Noise of External Inputs



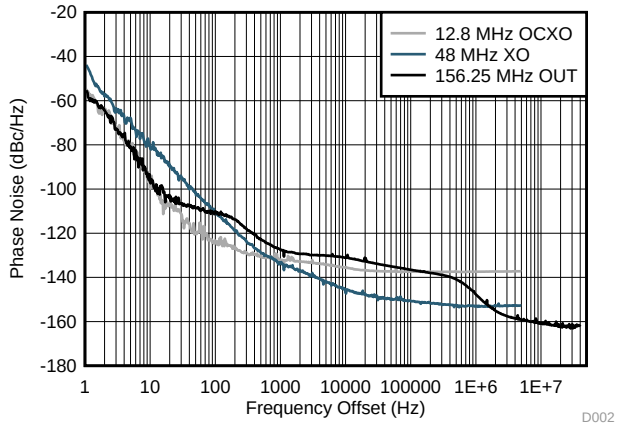
Output Phase Jitter = 160-fs RMS (12 kHz to 20 MHz)
f_{IN} = 25 MHz, f_{TCXO} = 10 MHz (OCXO) , f_{XO} = 48.0048 MHz,
$f_{TCXO-TDC}$ = 20 MHz, $BW_{REF-DPLL}$ = 5 Hz, $BW_{TCXO-DPLL}$ = 400 Hz

Figure 8. 122.88-MHz Output Phase Noise (3-Loop) With Phase Noise of External Inputs



Output Phase Jitter = 170-fs RMS (12 kHz to 20 MHz)
f_{IN} = 19.44 MHz, f_{TCXO} = 12.8 MHz (OCXO), f_{XO} = 48.0048 MHz,
$f_{TCXO-TDC}$ = 25.6 MHz, $BW_{REF-DPLL}$ = 1 Hz, $BW_{TCXO-DPLL}$ = 200 Hz

Figure 9. 155.52-MHz Output Phase Noise (3-Loop) With Phase Noise of External Inputs



Output Phase Jitter = 170-fs RMS (12 kHz to 20 MHz)
f_{TCXO} = 12.8 MHz (OCXO), f_{XO} = 48.0048 MHz,
$f_{TCXO-TDC}$ = 25.6 MHz, $BW_{TCXO-DPLL}$ = 200 Hz

Figure 10. 156.25-MHz Output Phase Noise (2-Loop TCXO) With Phase Noise of External Inputs

8 Parameter Measurement Information

8.1 Output Clock Test Configurations

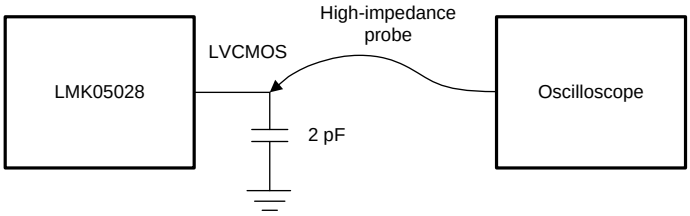


Figure 11. LVCMOS Output Test Configuration

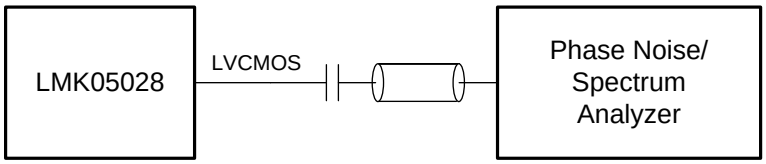


Figure 12. LVCMOS Output Phase Noise Test Configuration

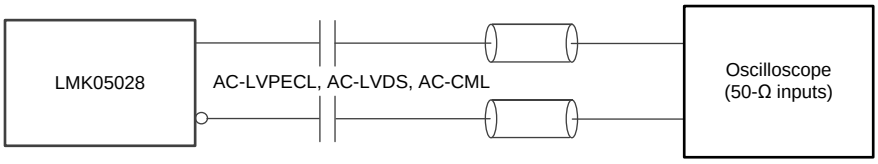


Figure 13. AC-LVPECL, AC-LVDS, AC-CML Output AC Test Configuration

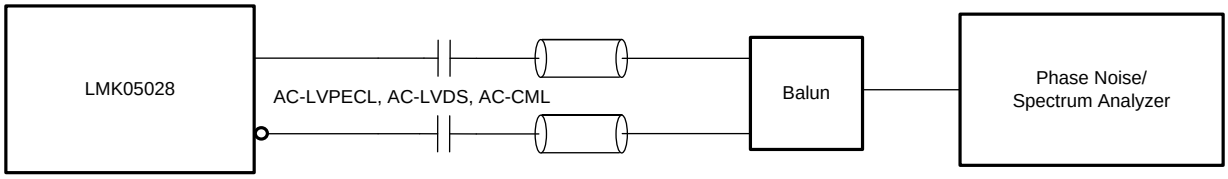


Figure 14. AC-LVPECL, AC-LVDS, AC-CML Output Phase Noise Test Configuration

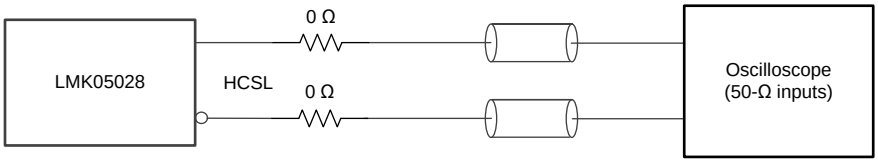


Figure 15. HCSL Output Test Configuration

Output Clock Test Configurations (continued)

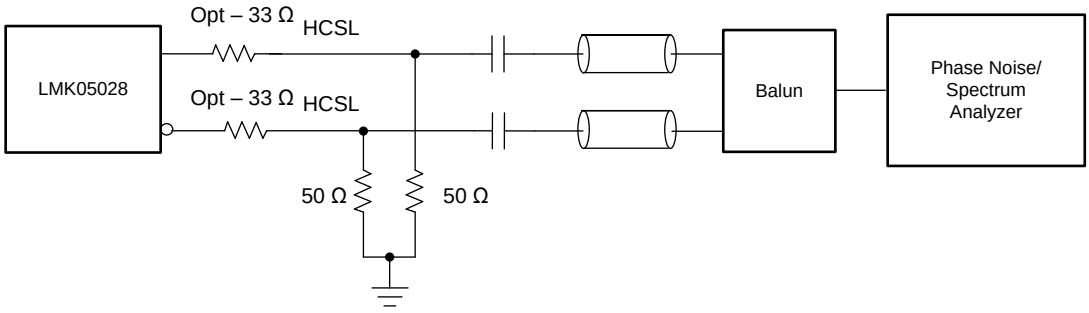
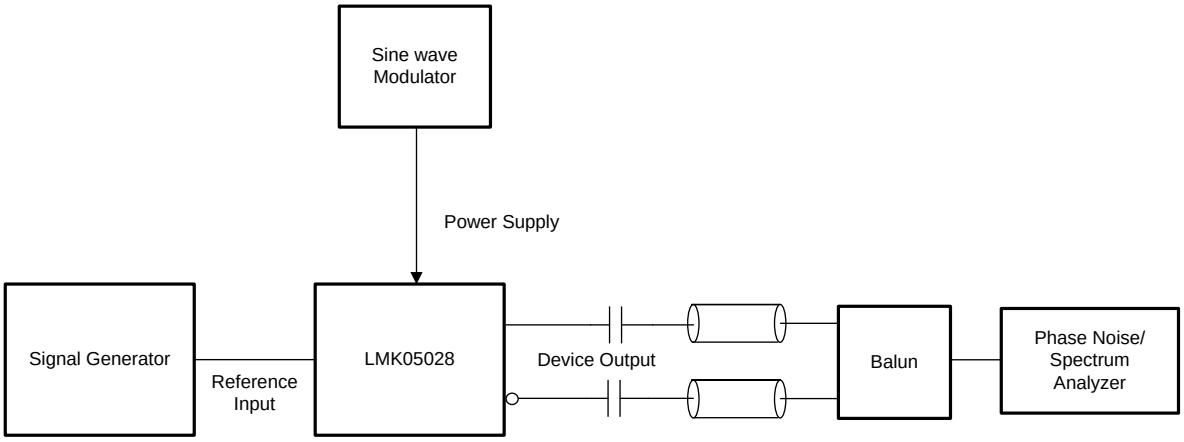


Figure 16. HCSL Output Phase Noise Test Configuration



Single-sideband spur level measured in dBc with a known noise amplitude and frequency injected onto the device power supply.

Figure 17. Power Supply Noise Rejection (PSNR) Test Configuration

9 Detailed Description

9.1 Overview

The LMK05028 is a high-performance network synchronizer clock device that provides jitter cleaning, clock generation, advanced clock monitoring, and superior hitless switching performance to meet the stringent timing requirements of communications infrastructure and industrial applications.

The LMK05028 features four reference inputs, two independent PLL channels, and eight output clocks with RMS phase jitter of 150-fs typical. The flexible PLL channels provide programmable loop bandwidths for input jitter and wander attenuation and fractional-N PLL frequency synthesis to generate any output frequency from any input frequency. Each PLL channel has three phase-locked loops comprised of two digital PLLs (DPLLs) and one analog PLL (APLL) with a low-noise integrated VCO. Each channel supports three-loop or two-loop mode configurations to optimize clock performance and solution cost for different use cases.

The reference input muxes support automatic input selection or manual input selection through software or pin control. The reference switchover event will be hitless with superior phase transient performance (50-ps typical). The reference clock input monitoring block monitors the clock inputs and will perform a switchover or holdover when a loss of reference (LOR) is detected. A LOR condition can be detected upon any violation of the threshold limits set for the input monitors, which include amplitude, frequency, missing pulse, runt pulse, and 1-PPS (pulse-per-second) detectors. The threshold limits for each input detector can be set and enabled independently per clock input. The tuning word history monitor feature allows the initial output frequency accuracy upon entry into holdover to be determined by the historical average frequency when locked, minimizing the frequency and phase disturbance during a LOR condition.

The device has eight outputs with programmable drivers, allowing up to eight differential clocks, eight LVCMOS pairs (two outputs per pair), or a combination of both. The output clocks can be selected from either PLL/VCO domain by the output muxes. A 1-PPS output can be supported on outputs 0 and 7. The output dividers have a SYNC feature to allow multiple outputs to be phase-aligned. If needed, zero delay can be enabled to achieve a deterministic phase offset between any specified PLL output clock and its selected input clock.

To support IEEE 1588 PTP slave clock or other clock steering applications, each PLL channel also supports DCO mode with <1-ppt (part per trillion) frequency resolution for precise frequency and phase adjustment through external software or pin control.

The device is fully programmable through I^2C or SPI and features custom start-up frequency configuration with the internal EEPROM, which is custom factory pre-programmable and in-system programmable. Internal LDO regulators provide excellent PSNR to reduce the cost and complexity of the power delivery network. The clock input and PLL monitoring status can be observed through the status pins and interrupt registers for full diagnostic capability.

9.1.1 ITU-T G.8262 (SyncE) Standards Compliance

The LMK05028 meets the applicable requirements of the ITU-T G.8262 (SyncE) standard. See the Application Report, *ITU-T G.8262 Compliance Test Result for the LMK05028* (SNAA315).

9.2 Functional Block Diagrams

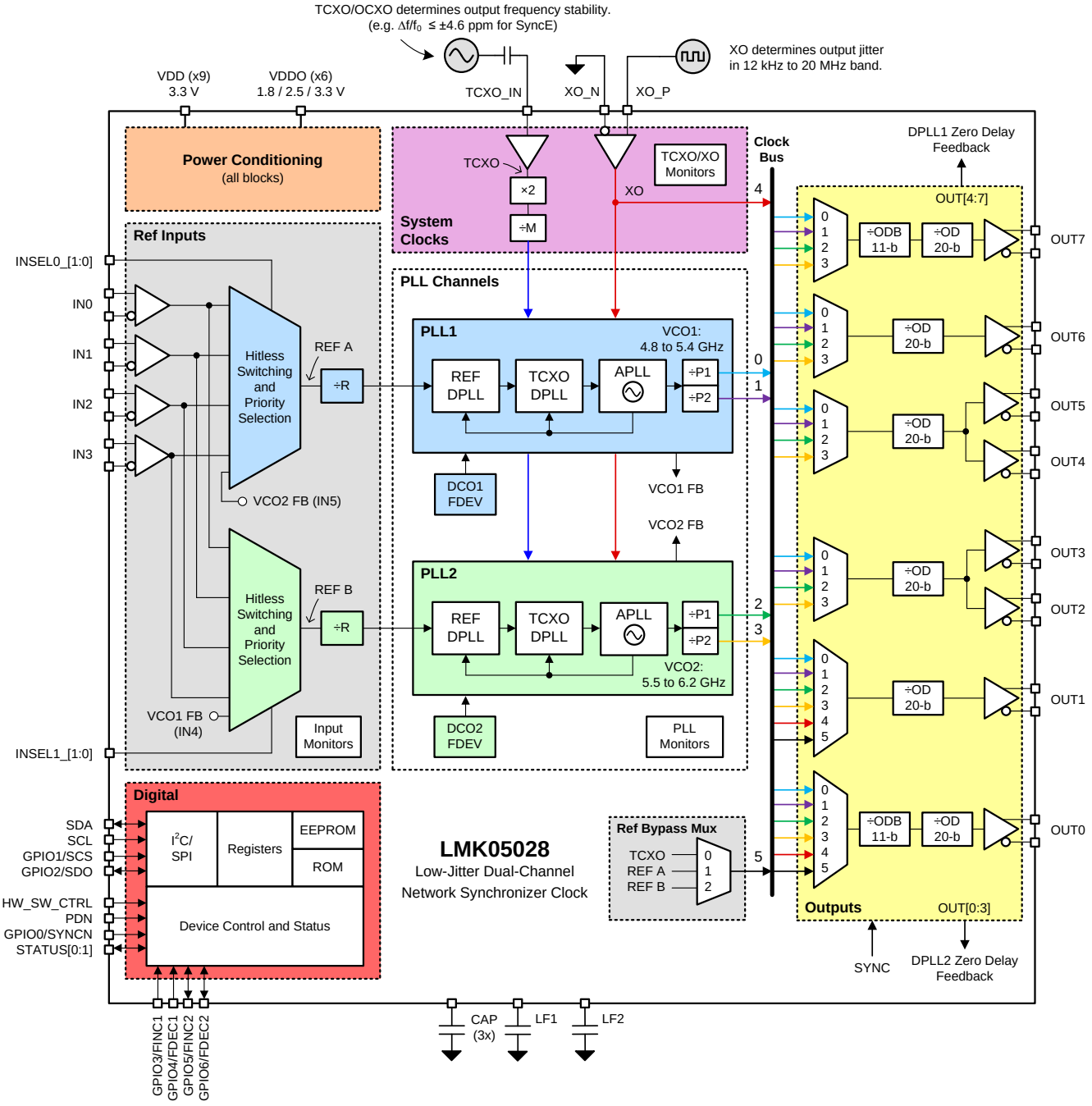
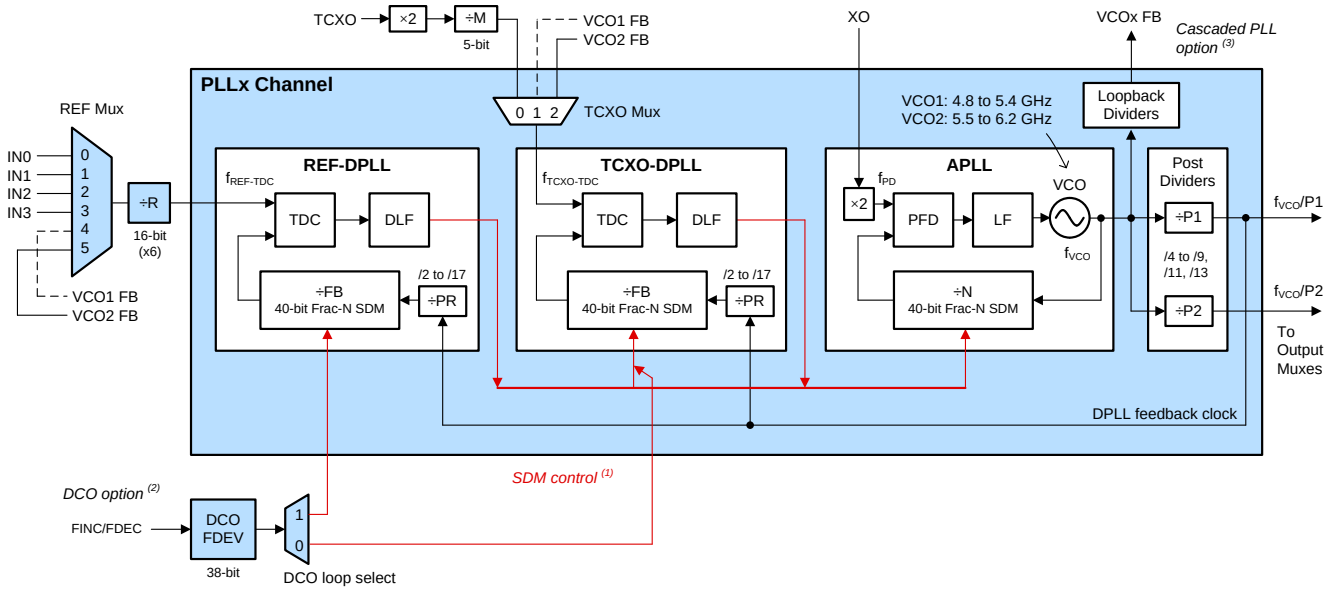


Figure 18. Top-Level Device Block Diagram

Functional Block Diagrams (continued)

9.2.1 PLL Architecture Overview

Figure 19 shows the 3-loop architecture implemented the same for both PLL channels with exception of the VCO frequency range. Each channel has three phase-locked loops with two digital PLLs (REF-DPLL and TCXO-DPLL) and one analog PLL (APLL) with integrated VCO. The REF-DPLL and TCXO-DPLL are each comprised of a time-to-digital converter (TDC), digital loop filter (DLF), feedback prescaler (PR), and 40-bit fractional feedback (FB) divider with sigma-delta-modulator (SDM or "MASH"). The APLL is comprised of a reference frequency doubler (×2), phase-frequency detector (PFD), loop filter (LF), fractional feedback (N) divider with SDM, and VCO.



(1) Fractional divider SDM control node depends on the selected PLL mode configuration.

(2) DCO frequency adjustments can be software or pin controlled.

(3) PLL cascading options: a) PLL1 VCO1 Loopback to PLL2, b) PLL2 VCO2 Loopback to PLL1.

Figure 19. PLL Architecture (One Channel)

Table 2 summarizes the PLL mode configuration options available in each channel. These modes support a wide range of use cases depending to the clock functionality and performance required in the application. Most applications will use 2-loop REF-DPLL or 3-loop mode for network synchronization clock features such as programmable loop bandwidth for jitter and wander attenuation, hitless switching, precise digital holdover, DCO frequency steering, and/or zero delay mode.

Table 2. PLL Mode Configuration Options

PLL MODE	FRACTIONAL SDM ENABLED (SDM CONTROL FROM)			DCO MODE OPTION	FREE-RUN / HOLDOVER CLOCK
	REF-DPLL	TCXO-DPLL	APLL		
1-Loop (APLL only)	–	–	Y (Free-run from XO)	–	XO
2-Loop REF-DPLL	Y (DCO option)	–	Y (REF-DPLL)	REF-DPLL SDM	XO
2-Loop TCXO-DPLL	–	Y (DCO option)	Y (TCXO-DPLL)	TCXO-DPLL SDM	TCXO
3-Loop	Y (DCO option)	Y (REF-DPLL)	Y (TCXO-DPLL)	REF-DPLL SDM	TCXO

The following sections describe the basic principle of operation for 2-loop and 3-loop modes. See PLL Operating Modes for more details on the PLL modes of operation including holdover.

9.2.2 3-Loop Mode

In 3-loop mode, the TCXO/OCXO source determines the free-run and holdover frequency stability and accuracy, and the XO source determines the output phase noise and jitter performance over the 12-kHz to 20-MHz integration band. 3-loop mode allows the use of a cost-effective, low-frequency TCXO/OCXO (such as 10 or 12.8 MHz) to support standards-compliant frequency stability and low loop bandwidth (≤10 Hz) required in synchronization applications like SyncE and SONET/SDH.

The principle of operation for 3-loop mode is as follows. After power-on reset and initialization, the APLL locks the VCO to the external XO input clock and operates in free-run mode. Once the external TCXO/OCXO input clock is detected, the TCXO-DPLL begins lock acquisition. The TCXO TDC compares the phase of the TCXO/OCXO clock and the TCXO FB divider clock (from the VCO) and generates a digital correction word corresponding to the phase error. The correction word is filtered by the TCXO DLF, and its output controls the APLL N divider SDM to pull the VCO frequency until it is locked to the TCXO/OCXO clock. After a valid reference input is selected, the REF-DPLL enters lock acquisition mode. The REF TDC compares the phase of the selected input clock and the REF FB divider clock (from the VCO) and generates a digital correction word. The correction word is filtered by the REF DLF, and its output controls the TCXO FB divider SDM which translates to a frequency offset to the TCXO TDC. This frequency correction propagates through the TCXO-DPLL which then controls the APLL N divider SDM to pull the VCO frequency until it is locked to the selected reference input clock.

If DCO mode is enabled on the REF-DPLL, a frequency deviation step value (FDEV) can be programmed and used to adjust (increment or decrement) the REF FB divider SDM, where the frequency adjustment effectively propagates through the 3 nested loops to the VCO output.

To ensure proper loop stability in 3-loop mode, the REF-DPLL has the lowest loop bandwidth ($BW_{REF\text{-}DPLL}$ ≤ 80 Hz, typical), the TCXO-DPLL has a higher loop bandwidth ($BW_{REF\text{-}DPLL}$ × 50 ≤ $BW_{TCXO\text{-}DPLL}$ ≤ 4 kHz), and the APLL has the highest bandwidth (BW_{APLL} is approximately 500 kHz typical).

When operating in 3-loop mode and all reference inputs to the REF-DPLL are lost, the PLL channel will enter holdover mode and operate similar to 2-loop TCXO-DPLL mode.

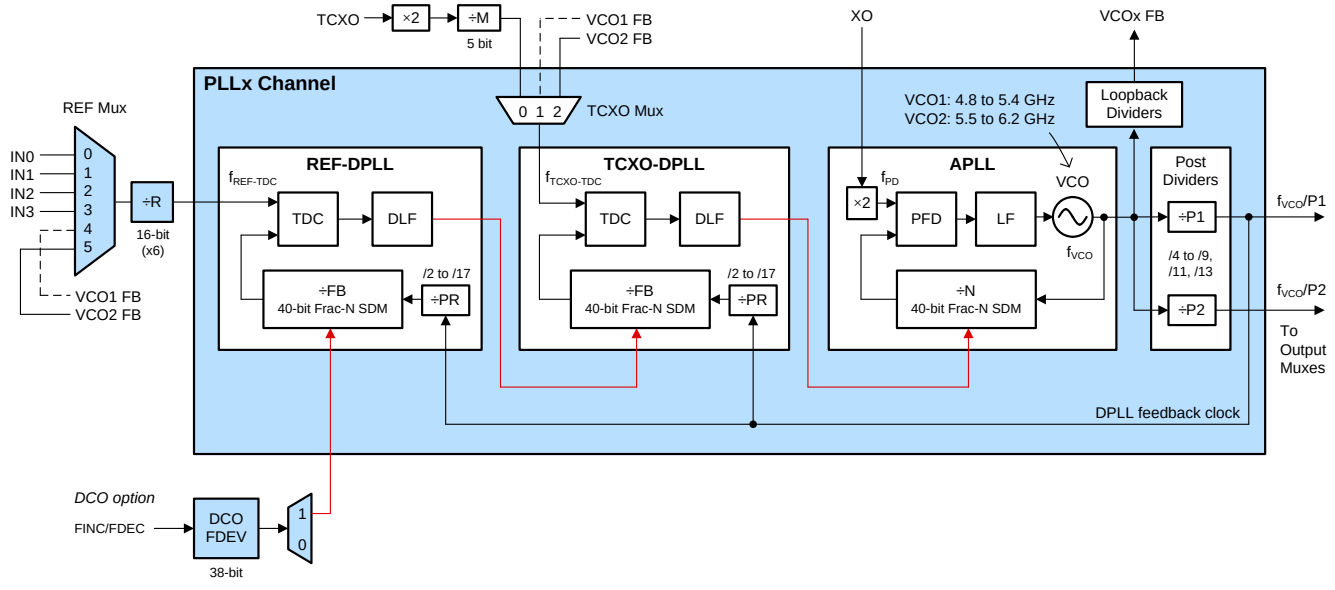
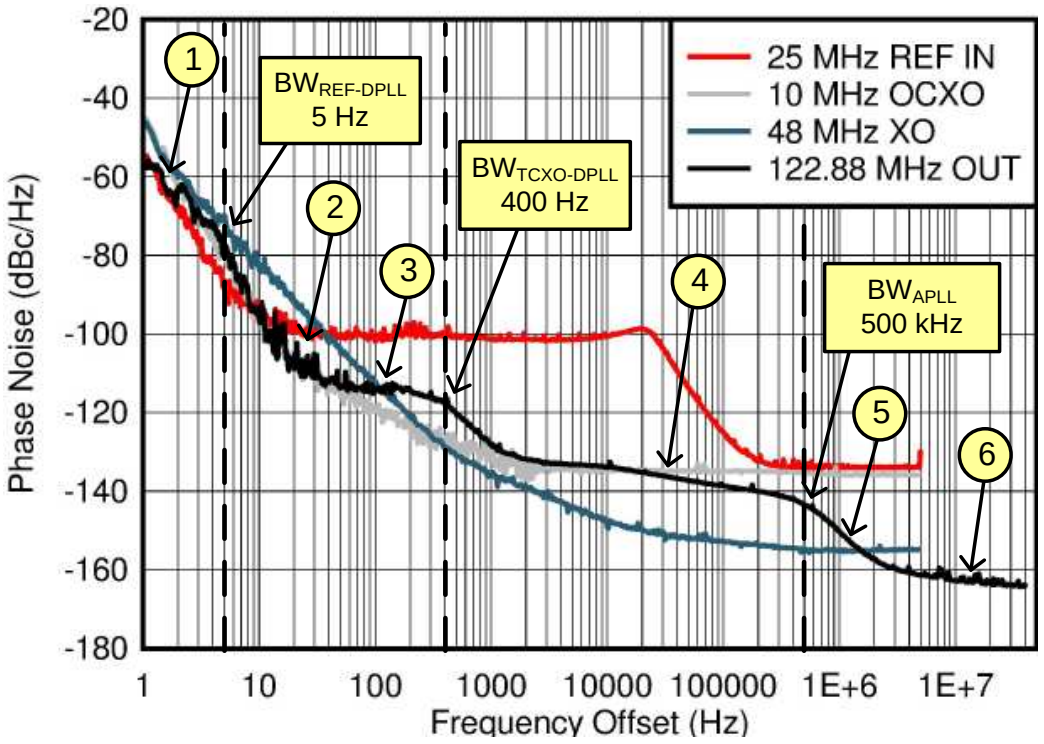


Figure 20. 3-Loop Mode with DCO Option

9.2.2.1 PLL Output Clock Phase Noise Analysis in 3-Loop Mode

The following plot shows an example PLL clock output phase noise profile in 3-loop mode. The PLL output clock phase noise at different frequency offsets are determined by different noise contributors, such as external clock input sources (REF IN, OCXO, XO) and internal noise sources (PLL, VCO), as well as the configured PLL loop bandwidths ($BW_{REF\text{-}DPLL}$, $BW_{TCXO\text{-}DPLL}$, BW_{APLL}). The phase noise profile shown for each external clock source (f_{SOURCE}) was normalized to the PLL output frequency (f_{OUT}) by adding $20\times LOG_{10}(f_{OUT} / f_{SOURCE})$ to the measured source's phase noise. The PLL output phase noise can be analyzed as follows:

1. Below $BW_{REF\text{-}DPLL}$, the REF input noise contributes to output.
2. Above $BW_{REF\text{-}DPLL}$, the REF input noise is attenuated by REF-DPLL bandwidth with up to 60-dB/decade roll-off.
3. Below $BW_{TCXO\text{-}DPLL}$, the OCXO noise and TDC noise of the TCXO-DPLL determine the output noise here. The close-in phase noise is –112 dBc/Hz at 100-Hz offset.
4. Above $BW_{TCXO\text{-}DPLL}$, the OCXO noise is attenuated. Below BW_{APLL}, the APLL noise dominates as the XO noise contribution is much lower.
5. Above BW_{APLL}, the VCO noise dominates and the XO noise is attenuated.
6. AC-LVPECL output noise floor is -163 dBc/Hz at 10-MHz offset.



Output Phase Jitter = 160-fs RMS (12 kHz to 20 MHz)

AC-LVPECL output, f_{IN} = 25 MHz, f_{TCXO} = 10 MHz (OCXO), f_{XO} = 48.0048 MHz, $f_{TCXO\text{-}TDC}$ = 20 MHz

Figure 21. 122.88-MHz Output Phase Noise (3-Loop) With Phase Noise of External Inputs

9.2.3 2-Loop REF-DPLL Mode

For applications that do not require the higher frequency stability in holdover mode and added cost of a TCXO/OCXO, 2-loop mode allows the XO input to determine the free-run and holdover frequency accuracy and also supports higher loop bandwidth.

The principle of operation for 2-loop REF-DPLL mode is similar to 3-loop mode except the TCXO-DPLL stage is bypassed. After power-on reset and initialization, the APLL locks the VCO to the external XO input clock and operates in free-run mode. After a valid reference input is selected, the REF-DPLL enters lock acquisition mode. The REF TDC compares the phase of the selected input clock and the REF FB divider clock (from the VCO) and generates a digital correction word. The correction word is filtered by the REF DLF, and its output controls the APLL N divider SDM to pull the VCO frequency until it is locked to the selected reference input clock.

If DCO mode is enabled on the REF-DPLL, a frequency deviation step value (FDEV) can be programmed and used to adjust (increment or decrement) the REF FB divider SDM, where the frequency adjustment effectively propagates through the two nested loops to the VCO output.

In 2-loop mode, the REF-DPLL loop bandwidth ($BW_{REF-DPLL}$) must be less than $f_{INx}/50$ and less than the maximum bandwidth of 4 kHz.

When operating in 2-loop mode and all reference inputs to the REF-DPLL are lost, the PLL channel will enter holdover mode and operate similar to 1-loop APLL only mode.

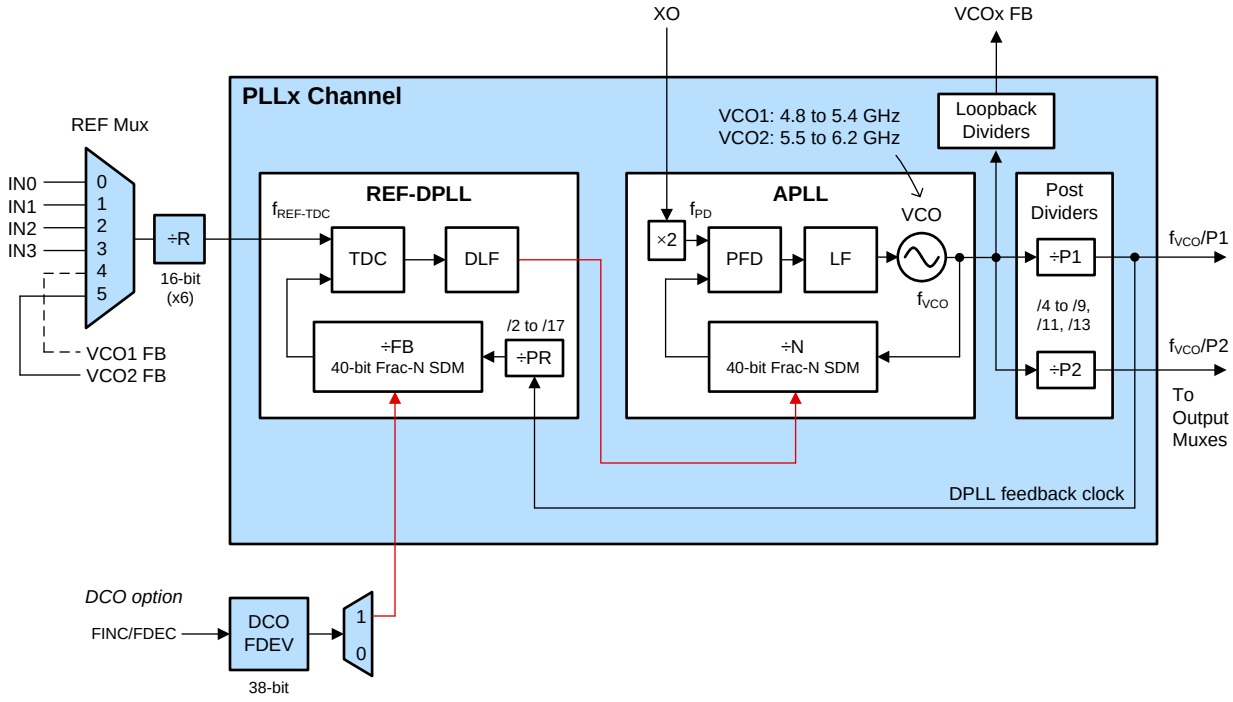


Figure 22. 2-Loop REF-DPLL Mode with DCO Option

9.2.4 2-Loop TCXO-DPLL Mode

The principle of operation for 2-loop TCXO-DPLL mode is similar to 3-loop mode except the REF-DPLL stage is bypassed. After power-on reset and initialization, the APLL locks the VCO to the external XO input clock and operates in free-run mode. Once the external TCXO/OCXO input clock is detected, the TCXO-DPLL begins lock acquisition. The TCXO TDC compares the phase of the TCXO/OCXO clock and the TCXO FB divider clock (from the VCO) and generates a digital correction word corresponding to the phase error. The correction word is filtered by the TCXO DLF, and its output controls the APLL N divider SDM to pull the VCO frequency until it is locked to the TCXO/OCXO clock.

If DCO mode is enabled on the TCXO-DPLL, a frequency deviation step value (FDEV) can be programmed and used to adjust (increment or decrement) the TCXO FB divider SDM, where the frequency adjustment effectively propagates through the two nested loops to the VCO output.

In 2-loop mode, the TCXO-DPLL loop bandwidth ($BW_{TCXO-DPLL}$) must less $f_{TCXO}/50$ and less than the maximum bandwidth of 4 kHz.

When operating in 2-loop mode and the TCXO input is lost, the PLL channel will operate similar to 1-loop APLL only mode.

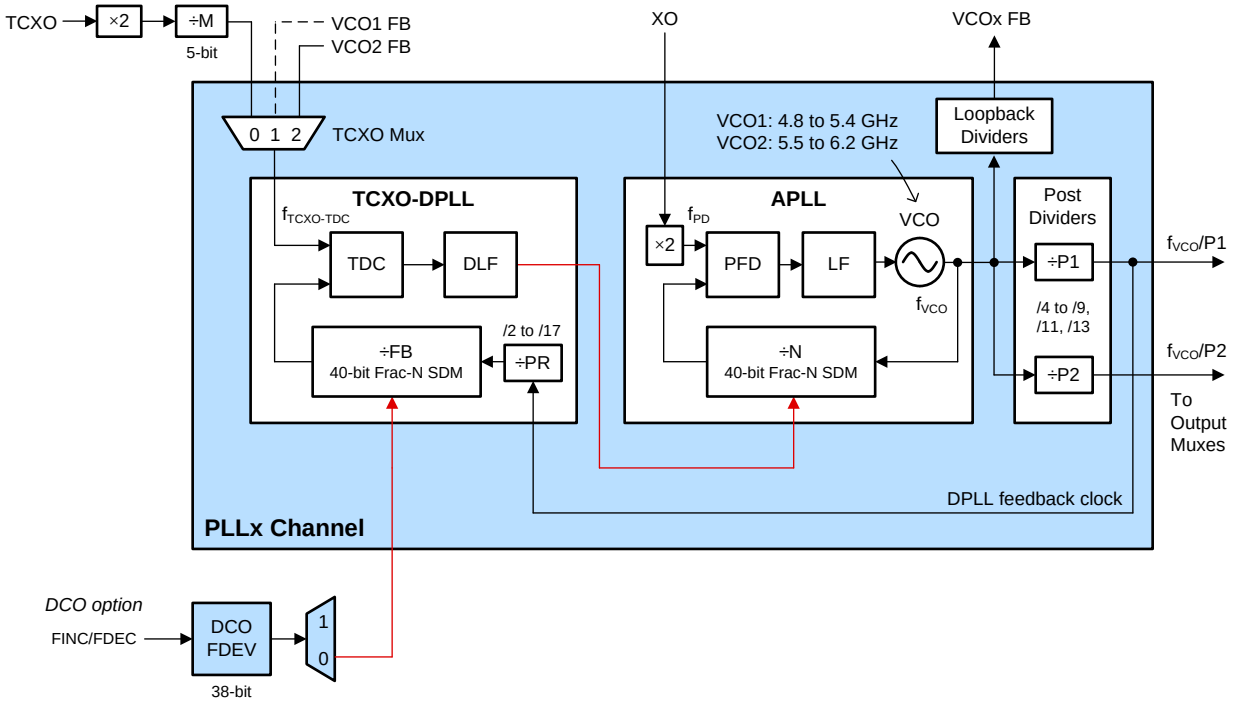


Figure 23. 2-Loop TCXO-DPLL Mode With DCO Option

9.2.5 PLL Configurations for Common Applications

Table 3. Example PLL Configurations Based on Common Application Design Parameters

MARKET SEGMENT / APPLICATION	KEY DESIGN GOALS			TYPICAL LOOP CONFIGURATION	
	HITLESS SWITCHING	BEST CLOSE-IN PHASE NOISE (100-Hz OFFSET)	WANDER ATTENUATION OR TCXO/OCXO HOLDOVER	PLL MODE	REF-DPLL BANDWIDTH
SyncE EEC Opt. 1, SDH G.813 Opt. 1	YES	–	YES	3-Loop	1 to 10 Hz
SyncE EEC Opt. 2, SONET GR-253	YES	–	YES	3-Loop	0.1 Hz
SyncE/IEEE 1588 PTP Slave	YES	–	YES	3-Loop with DCO Mode Enabled	See above for SyncE EEC Opt. 1 or 2
1-PPS Input	–	–	YES	3-Loop	0.02 Hz
Wireless/BTS	YES	YES	YES	3-Loop with DCO Mode Option	1 to 20 Hz
Test Instrumentation (for example, 10-MHz Ref. In)	Optional	YES	YES	3-Loop	1 to 40 Hz
Medical Imaging	–	YES	Optional	2-Loop TCXO	100 to 400 Hz
OTN/OTU	–	–	–	2-Loop REF	100 to 300 Hz
Broadcast (Genlock)	Optional	–	YES (TCXO)	2-Loop REF	1 to 10 Hz
Other Jitter Cleaning	Optional	–	–	2-Loop REF	10 to 100 Hz

9.3 Feature Description

The following sections describe the features and functional blocks of the LMK05028.

9.3.1 Oscillator Input (XO_P/N)

The XO input is the reference clock for the fractional-N APLLs. The combination of XO and APLL determines the jitter and phase noise performance of the output clocks. For optimal performance, the XO frequency should be at least 48 MHz and have a non-integer frequency relationship with the VCO frequencies so the APLLs operate in fractional mode. When the TCXO input is not used by either PLL channel, the XO input determines the output frequency accuracy and stability in free-run or holdover modes.

The XO input buffer has programmable input on-chip termination and AC-coupled input biasing configurations as shown in Figure 24.

The buffered XO path also drives the input monitoring blocks as well as output muxes, allowing buffered copies of the XO input on OUT0 and/or OUT1.

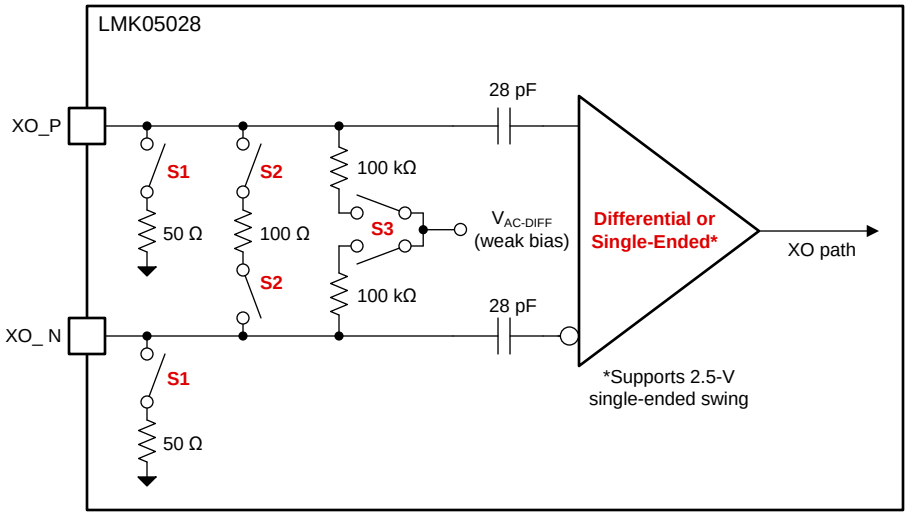


Figure 24. XO Input Buffer

Table 4 lists the typical XO input buffer configurations for common clock interface types.

Table 4. XO Input Buffer Modes

XO_DIFF_TYPE	INPUT TYPES	INTERNAL SWITCH SETTINGS	
		INTERNAL TERM. (S1, S2)(1)	INTERNAL BIAS (S3)(2)
0h	LVDS, CML, LVPECL, LVCMOS (DC-coupled)	OFF	OFF
1h	LVDS, CML, LVPECL (AC-coupled)	OFF	ON (1.3 V)
3h	LVDS, CML, LVPECL (AC-coupled, internal 100-Ω)	100 Ω	ON (1.3 V)
4h	HCSL (DC-coupled, internal 50-Ω)	50 Ω	OFF

(1) S1, S2: OFF = External termination is assumed.
(2) S3: OFF = External input bias or DC coupling is assumed.

9.3.2 TCXO/OCXO Input (TCXO_IN)

The TCXO input is the reference clock to the TCXO-DPLL loop in each PLL channel. When the PLL channel uses the TCXO-DPLL, the TCXO input source determines the close-in phase noise and wander performance (MTIE/TDEV) when the DPLL is locked, as well as the frequency accuracy and stability in free-run and holdover modes. A TCXO input with high phase noise floor should have minimal or no impact on the output jitter performance, provided the TCXO loop bandwidth is designed low enough to attenuate its noise contribution. This input can be driven from a low-frequency TCXO, OCXO, or external traceable clock that conforms to the frequency accuracy and holdover stability requirements of the application. TCXO and OCXO frequencies of 10 to 12.8 MHz are widely available and cost-effective options.

The TCXO input can accept an AC-coupled single-ended clock (sine, clipped-sine, or square wave) and has an internal weak bias of about 0.6 V. The input voltage swing should be less than 1.3 Vpp and terminated before AC-coupling to the pin. If unused, the TCXO input buffer can be powered down by register bit and the pin can be left floating.

The buffered TCXO path also drives the input monitoring blocks as well as the TCXO/Ref bypass mux to the output muxes, allowing a buffered copy of the TCXO input on OUT0 and/or OUT1.

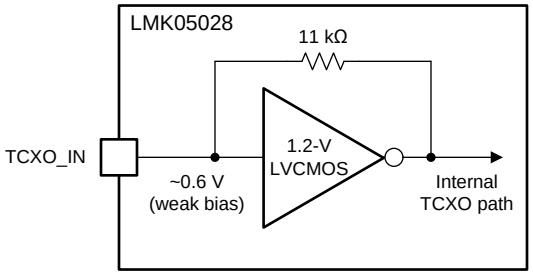


Figure 25. TCXO Input Buffer

9.3.3 Reference Inputs (INx_P/N)

The reference inputs (IN0 to IN3) can accept differential or single-ended clocks to synchronize any of the PLL channels. Each input has programmable input type, termination, and AC-coupled input biasing configurations as shown in Figure 26. Each input buffer drives the reference input mux of both DPLL blocks. The DPLL input mux can select from any of the reference inputs. Any DPLL can switch between inputs with different frequencies provided they can be divided-down to a common frequency by DPLL R dividers (DPLLy_REFx_RDIV). The reference input paths also drive the various detector blocks for reference input monitoring and validation. The selected reference of each DPLL input (before the R divider) can be routed through the TCXO/Ref bypass mux and output muxes, allowing a buffered copy of either DPLL reference input on OUT0 and/or OUT1.

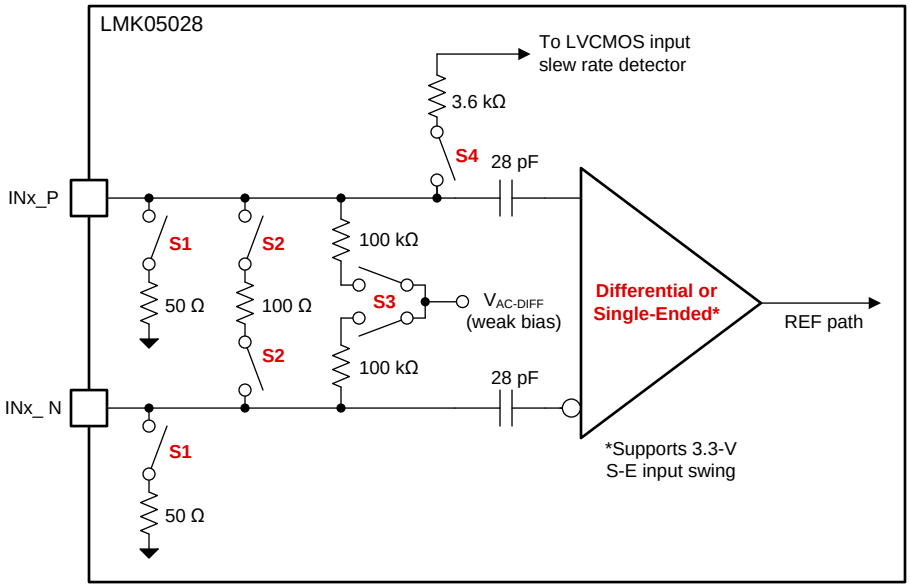


Figure 26. Reference Input Buffer

Table 5 lists the reference input buffer configurations for common clock interface types.

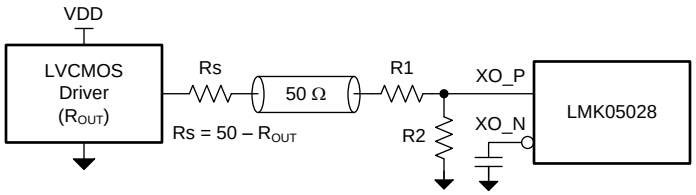
Table 5. Reference Input Buffer Modes

REFx_TYPE	INPUT TYPES	INTERNAL SWITCH SETTINGS		
		INTERNAL TERM. (S1, S2)(1)	INTERNAL BIAS (S3)(2)	LVCMOS SLEW RATE DETECT (S4)(3)
0h	LVDS, CML, LVPECL (DC-coupled)	OFF	OFF	OFF
1h	LVDS, CML, LVPECL (AC-coupled)	OFF	ON (1.3 V)	OFF
3h	LVDS, CML, LVPECL (AC-coupled, internal 100-Ω)	100 Ω	ON (1.3 V)	OFF
4h	HCSL (DC-coupled, internal 50-Ω)	50 Ω	OFF	OFF
8h	LVCMOS	OFF	OFF	ON

(1) S1, S2: OFF = External termination is assumed.
(2) S3: OFF = External input bias or DC coupling is assumed.
(3) S4: OFF = Differential input amplitude detector is used for all input types except LVCMOS.

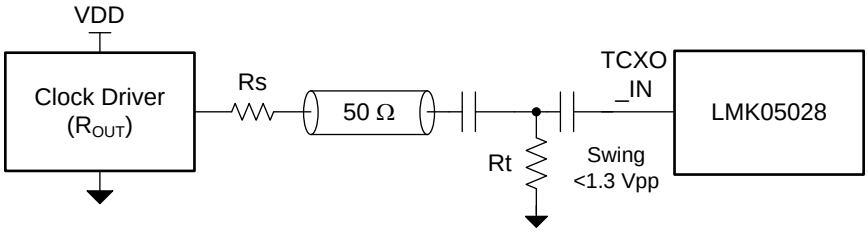
9.3.4 Clock Input Interfacing and Termination

Figure 27 through Figure 34 show the recommended input interfacing and termination circuits. Unused clock inputs can be left floating or pulled down.



VDD	R1 (Ω)	R2 (Ω)
3.3 V	125	375
2.5 V	0	open
1.8 V	0	open

Figure 27. Single-Ended LVCMOS to XO Input (XO_P)



Driver	Rs (Ω)	Rt (Ω)
3.3-V LVCMOS	100	50
2.5-V LVCMOS	68	50
1.8-V LVCMOS	33	50
(Clipped) Sinewave	0	open

Figure 28. Single-Ended LVCMOS or Sinewave to TCXO Input (TCXO_IN)

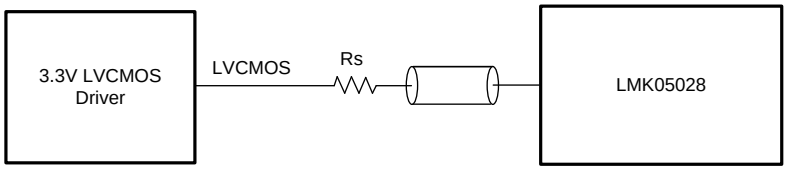


Figure 29. Single-Ended LVCMOS (1.8, 2.5, 3.3 V) to Reference (INx_P)

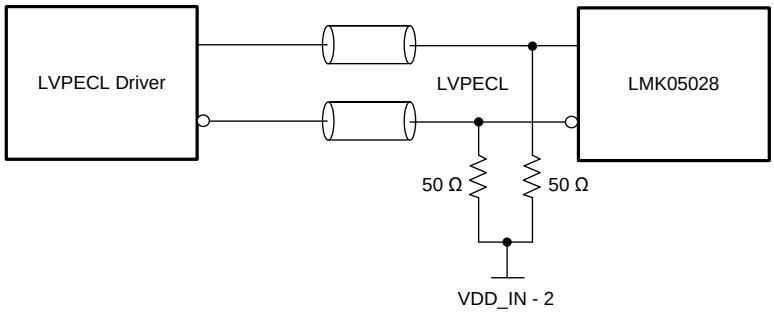


Figure 30. DC-Coupled LVPECL to Reference (INx) or XO Inputs

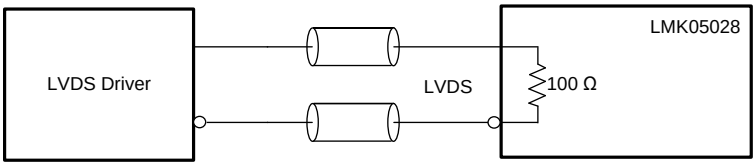


Figure 31. DC-Coupled LVDS to Reference (INx) or XO Inputs

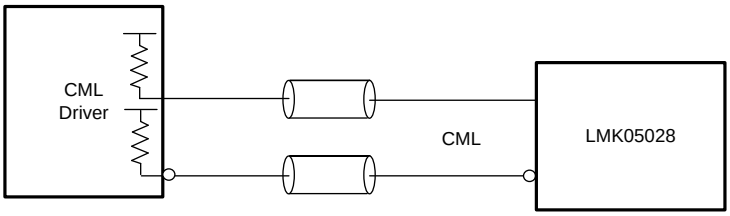


Figure 32. DC-Coupled CML (Source Terminated) to Reference (INx) or XO Inputs

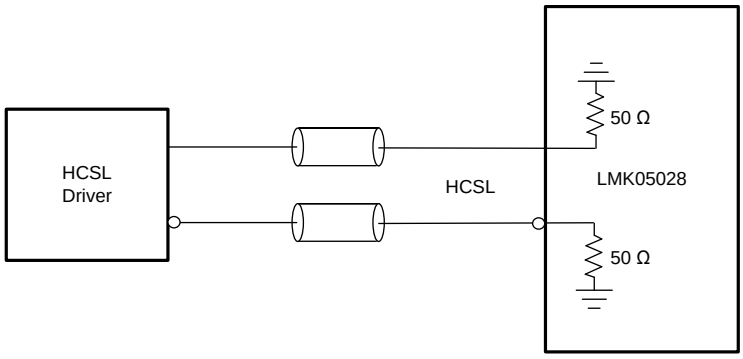


Figure 33. HCSL (Load Terminated) to Reference (INx) or XO Inputs

Driver	R_B (Ω)
LVDS	open
CML*	open
3.3-V LVPECL	150
2.5-V LVPECL	82
HCSL	50

*CML driver has 50-Ω pull-up

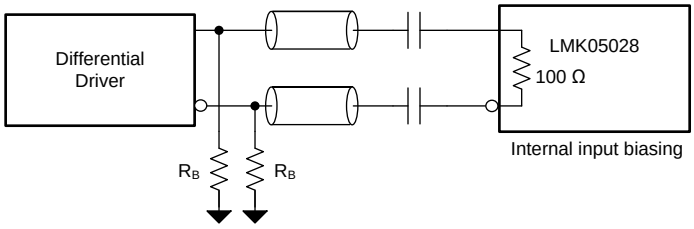


Figure 34. AC-Coupled Differential to Reference (INx) or XO Inputs

9.3.5 Reference Input Mux Selection

For each REF-DPLL block, the reference input mux selection can be done automatically using an internal state machine with a configurable input priority scheme, or manually through software register control or hardware pin control. The input mux can select from IN0 to IN3. Additionally, DPLL1 can select IN5 as an internal loopback clock divided-down from PLL2's VCO (VCO2 FB clock), and DPLL2 can select IN4 as an internal loopback clock from PLL1's VCO (VCO1 FB clock).

The priority for all inputs can be assigned for each DPLL through registers. The priority ranges from 0 to 6, where 0 means Ignored (never select) and 1 to 6 are highest (1st) to lowest (6th) priority. When two or more inputs are configured with the same priority setting, the reference input with the lowest index (INx) will be given higher priority.

The currently selected reference input for each DPLL can be read through the status pin or register.

9.3.5.1 Automatic Input Selection

There are two automatic input selection modes that can be set by a register: Auto Revertive and Auto Non-Revertive.

- *Auto Revertive:* In this mode, the DPLL automatically selects the valid input with the highest configured priority. If a clock with higher priority becomes valid, the DPLL will automatically switch over to that clock immediately.
- *Auto Non-Revertive:* In this mode, the DPLL automatically selects the highest priority input that is valid. If a higher priority input because valid, the DPLL will not switch-over until the currently selected input becomes invalid.

9.3.5.2 Manual Input Selection

There are two manual input selection modes that can be set by a register: Manual with Auto-Fallback and Manual with Auto-Holdover. In either manual mode, the input selection can be done through register control (Table 6) or hardware pin control (Table 7).

- *Manual with Auto-Fallback:* In this mode, the manually selected reference is the active reference until it becomes invalid. If the reference becomes invalid, the DPLL will automatically fallback to the highest priority input that is valid or qualified. If no prioritized inputs are valid, the DPLL will enter holdover mode (if tuning word history is valid) or free-run mode. The DPLL will exit holdover mode when the selected input becomes valid.
- *Manual with Auto-Holdover:* In this mode, the manually selected reference is the active reference until it becomes invalid. If the reference becomes invalid, the DPLL will automatically enter holdover mode (if tuning word history is valid) or free-run mode. The DPLL will exit holdover mode when the selected input becomes valid.

Table 6. Manual Input Selection by Register Bits

DPLLx_REF_MAN_REG_SEL[2:0] BITS	DPLLx_REF_MAN_SEL BIT	SELECTED INPUT
000b	0	IN0
001b	0	IN1
010b	0	IN2
011b	0	IN3

Table 6. Manual Input Selection by Register Bits (continued)

DPLLx_REF_MAN_REG_SEL[2:0] BITS	DPLLx_REF_MAN_SEL BIT	SELECTED INPUT
100b	0	VCO1 Loopback to DPLL2
101b	0	VCO2 Loopback to DPLL1

Table 7. Manual Input Selection by Hardware Pins

INSELx_[1:0] PINS	DPLLx_REF_MAN_SEL BIT	SELECTED INPUT
00b	1	IN0
01b	1	IN1
10b	1	IN2
11b	1	IN3

The reference input selection flowchart is shown in Figure 35.

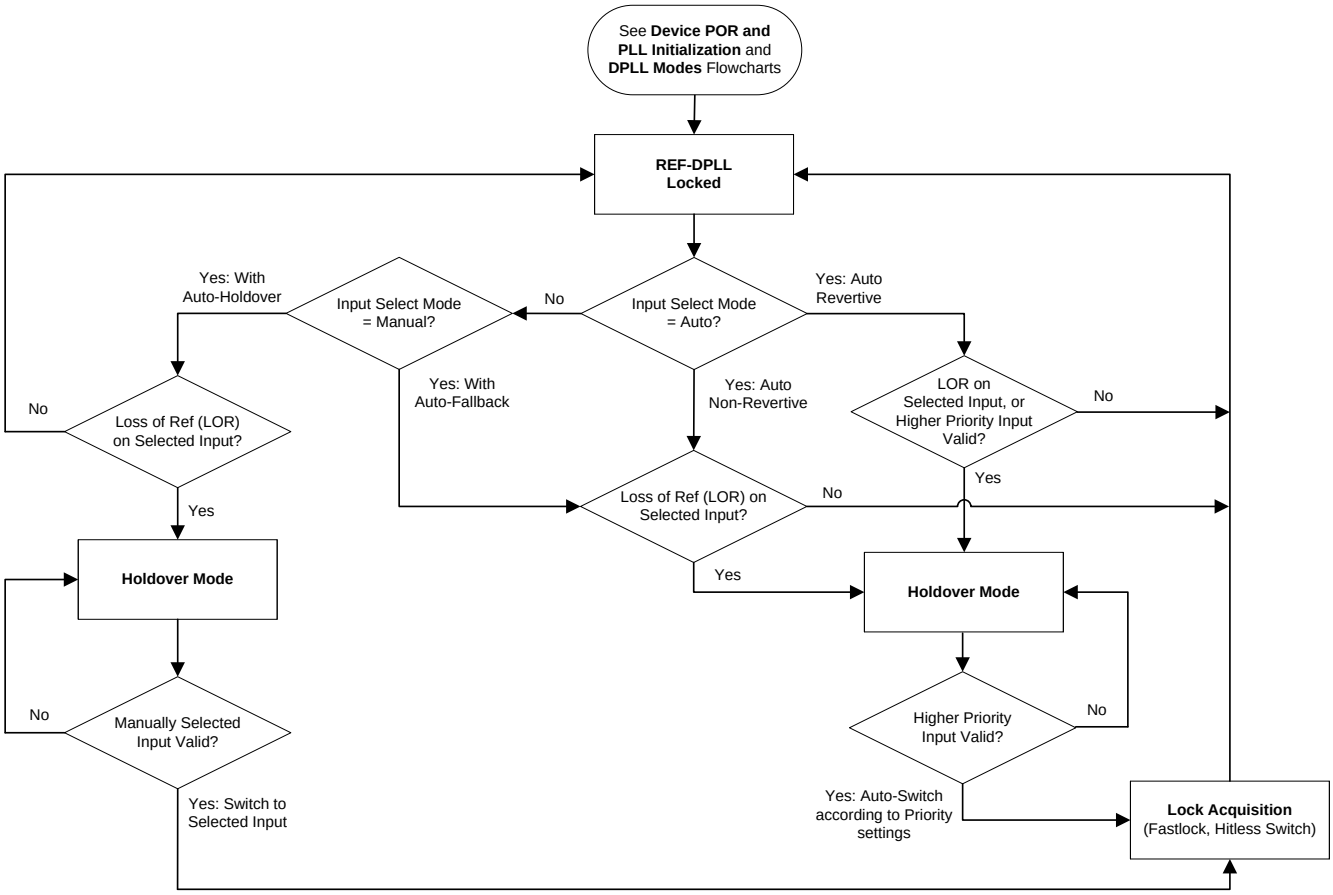


Figure 35. Reference Input Selection Flowchart

9.3.6 Hitless Switching

Each REF-DPLL supports hitless switching through a proprietary phase cancellation scheme, which can be enabled per DPLL. When hitless switching is enabled, it will prevent a phase transient (phase hit) from propagating to the outputs when the two switched inputs have a fixed phase offset and are frequency-locked. The inputs are frequency-locked when they have same exact frequency (0-ppm offset), or have frequencies that are integer-related and can each be divided to a common frequency by integers. When hitless switching is

disabled, a phase hit equal to the phase offset between the two inputs will be propagated to the output at a rate determined by the REF-DPLL fastlock bandwidth. The hitless switching specifications ($t_{HITLESS}$ and $f_{HITLESS}$) are valid for reference inputs with no wander. In the case where two inputs are switched but are not frequency-locked, the output smoothly transitions to the new frequency with reduced transient. Hitless switching is not supported for 1-PPS inputs.

9.3.7 Gapped Clock Support on Reference Inputs

Each DPLL supports locking to an input clock that has missing periods and is referred to as a gapped clock. Gapping a clock severely increases its jitter, so the device provides the high input jitter tolerance and low loop bandwidth necessary to generate a low-jitter periodic output clock. The resulting output will be a periodic non-gapped clock with an average frequency of the input with its missing cycles. The gapped clock width cannot be longer be than the reference clock period after the R divider (R_{INx} / f_{INx}). The reference input monitors should be configured to avoid any flags due to the worst-case clock gapping scenario to achieve and maintain lock. Reference switchover between two gapped clock inputs may violate the hitless switching specification if the switch occurs during a gap in either input clock.

9.3.8 Input Clock and PLL Monitoring, Status, and Interrupts

The following section describes the input clock and PLL monitoring, status, and interrupt features.

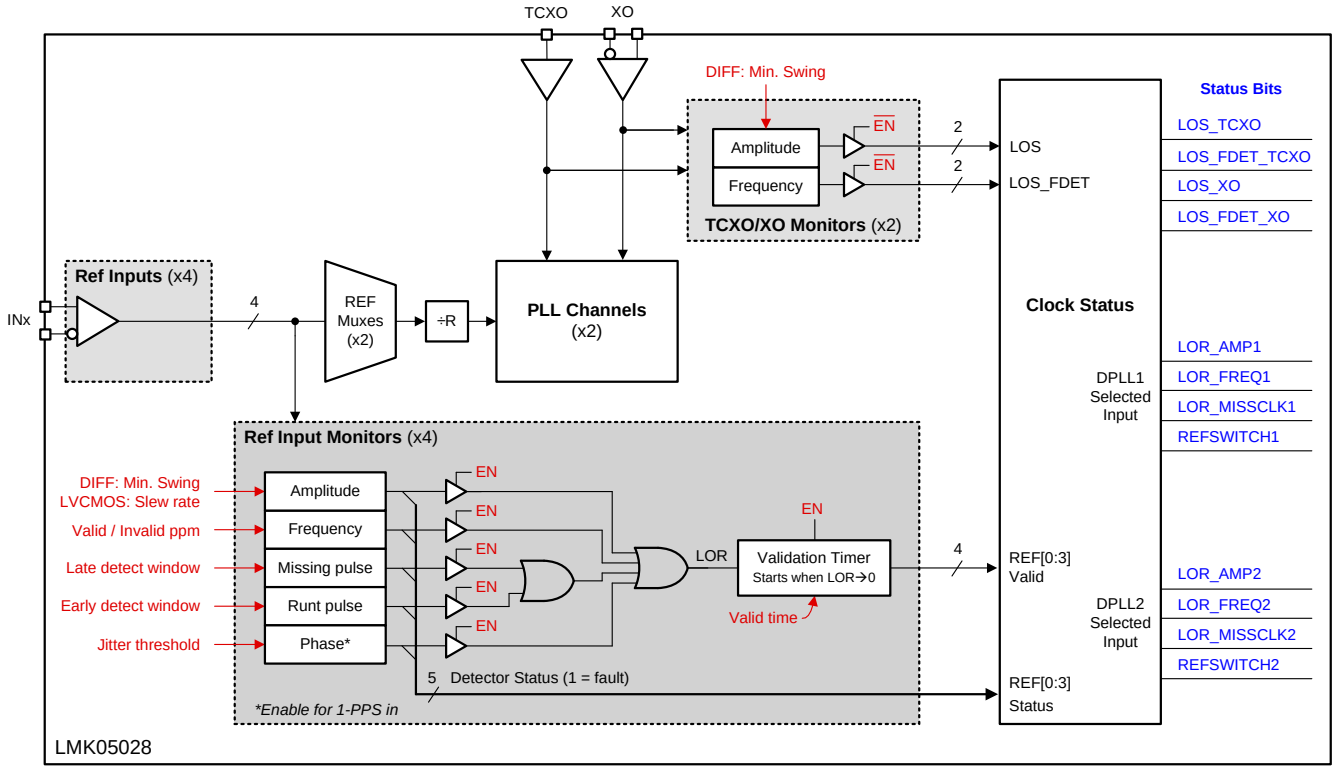


Figure 36. Clock Monitors for References, XO, and TCXO Inputs

9.3.8.1 XO Input Monitoring

The XO input has amplitude and frequency monitors to help qualify the input before it can be used to lock the APLLs.

The XO amplitude detector clears its LOS (loss-of-signal) flag when the differential input voltage swing (peak-to-peak) is greater than the minimum threshold selected by the registers (400, 600, or 800 mVpp nominal). The same threshold applies also for a single-ended LVCMOS input with the non-driven input pin pulled to ground. If the input clock does not meet the amplitude threshold, the amplitude detector will set the LOS flag and disqualify the input.

The XO frequency detector clears its LOS_FDET flag when the input frequency is detected within the range of about 10 MHz to 90 MHz. Above 90 MHz, the frequency detector should be bypassed for proper operation. The XO frequency monitor uses a RC-based detector and cannot precisely detect if the XO input clock has sufficient frequency stability to ensure successful VCO calibration during the PLL start-up when the external XO clock has a slow or delayed start-up behavior. See *Slow or Delayed XO Start-Up* for more information.

The XO monitors can be bypassed through registers, so the input will always be considered valid by the PLL control state machines. The XO's LOS status flags can be observed through the status pins and the status bits. The XO LOS signal from the status pin is the logic-OR combination of both its amplitude and frequency monitor flags.

9.3.8.2 TCXO Input Monitoring

The TCXO input has amplitude and frequency monitors to help qualify the input before it can be used to lock the TCXO-DPLLs.

The TCXO amplitude detector determines if the input meets the minimum input slew rate threshold. The input slew rate detector clears its LOS flag when the slew rate is faster than 0.2 V/ns on the clock edge selected by the registers (rising edge, falling edge, or both edges). If the input clock does not meet the slew rate threshold on the selected clock edge(s), the amplitude monitor will set the LOS flag and disqualify the input.

The TCXO frequency detector clears its LOS_FDET flag when the input frequency is detected within the range of about 10 MHz to 90 MHz. Above 90 MHz, the frequency detector should be bypassed for proper operation.

The TCXO monitors can be bypassed through registers, so the input will always considered valid by the PLL control state machines. The TCXO's LOS status flags can be observed through the status pins and the status bits. The TCXO LOS signal from the status pin is the logic-OR combination of both its amplitude and frequency monitor flags.

9.3.8.3 Reference Input Monitoring

Each DPLL reference clock input is independently monitored for input validation (qualification) before it is available for input selection by either DPLL. The reference monitoring blocks include amplitude, frequency, missing pulse, and runt pulse monitors. For a 1-PPS input, the phase valid monitor is supported and the frequency, missing pulse, and runt pulse monitors are not supported. A validation timer sets the minimum time for all enabled reference monitors to be clear of flags before an input is qualified.

The enablement and valid threshold for all reference monitors and validation timers are programmable per input. The reference monitors and validation timers are optional to enable, but critical to achieve optimal transient performance during holdover or switchover events and also to avoid selection of an unreliable or intermittent clock input. If a given detector is not enabled, it will not set a flag and will be ignored. The status flag of any enabled detector can be observed through the status pins for any reference input (selected or not selected). The status flags of the enabled detectors can also be read through the status bits for the selected input of each DPLL.

9.3.8.3.1 Reference Validation Timer

The validation timer sets the amount of time for each reference to be clear of flags from all enabled input monitors before it is qualified and valid for selection. The validation timer and enable settings are programmable.

9.3.8.3.2 Amplitude Monitor

The reference amplitude detector determines if the input meets the amplitude-related threshold depending on the input buffer configuration. For differential input mode, the amplitude detector clears its LOR_AMP flag when the differential input voltage swing (peak-to-peak) is greater than the minimum threshold selected by the registers (400, 500, or 600 mVpp nominal). For LVCMOS input mode, the input slew rate detector clears its LOR_AMP flag when its slew rate is faster than 0.2 V/ns on the clock edge selected by the registers (rising edge, falling edge, or both edges). If either the differential or LVCMOS input clock does not meet the specified thresholds, the amplitude detector will set the LOR_AMP flag and disqualify the input.

Below about 5 MHz, the differential input detector may signal a false flag; in this case, the amplitude detector should be disabled and at least one other input monitor (frequency, window detector) should be enabled to validate the input clock. The LVCMOS input detector can be used for low-frequency clocks down to 1 Hz or 1 PPS.

9.3.8.3.3 Missing Pulse Monitor (Late Detect)

The missing pulse monitor uses a window detector to validate input clock pulses that arrive within the nominal clock period plus a programmable late window threshold (T_{LATE}). When an input pulse arrives before T_{LATE}, the pulse is considered valid and the missing pulse flag will be cleared. When an input pulse does not arrive before T_{LATE} (due to a missing or late pulse), the flag will be set immediately to disqualify the input.

Typically, T_{LATE} should be set higher than the input's longest clock period (including cycle-to-cycle jitter), or higher than the gap width for a gapped clock. The missing pulse monitor can act as a coarse frequency detector with faster detection than the ppm frequency detector. The missing pulse monitor is supported for input frequencies between 2 kHz and $f_{VCO}/48$ and should be disabled when outside this range.

The missing pulse and runt pulse monitors operate from the same window detector block for each reference input. The status flags for both these monitors are combined by logic-OR gate and can be observed through status pin. The window detector flag for the selected DPLL input can also be observed through the corresponding MISSCLK status bit.

9.3.8.3.4 Runt Pulse Monitor (Early Detect)

The runt pulse monitor uses a window detector to validate input clock pulses that arrive within the nominal clock period minus a programmable early window threshold (T_{EARLY}). When an input pulse arrives after T_{EARLY}, the pulse is considered valid and the runt pulse flag will be cleared. When an early or runt input pulse arrives before T_{EARLY}, the monitor will set the flag immediately to disqualify the input.

Typically, T_{EARLY} should be set lower than the input's shortest clock period (including cycle-to-cycle jitter). The early pulse monitor can act as a coarse frequency detector with faster detection than the ppm frequency detector. The early pulse monitor is supported for input frequencies between 2 kHz and $f_{VCO}/48$ and should be disabled when outside this range.

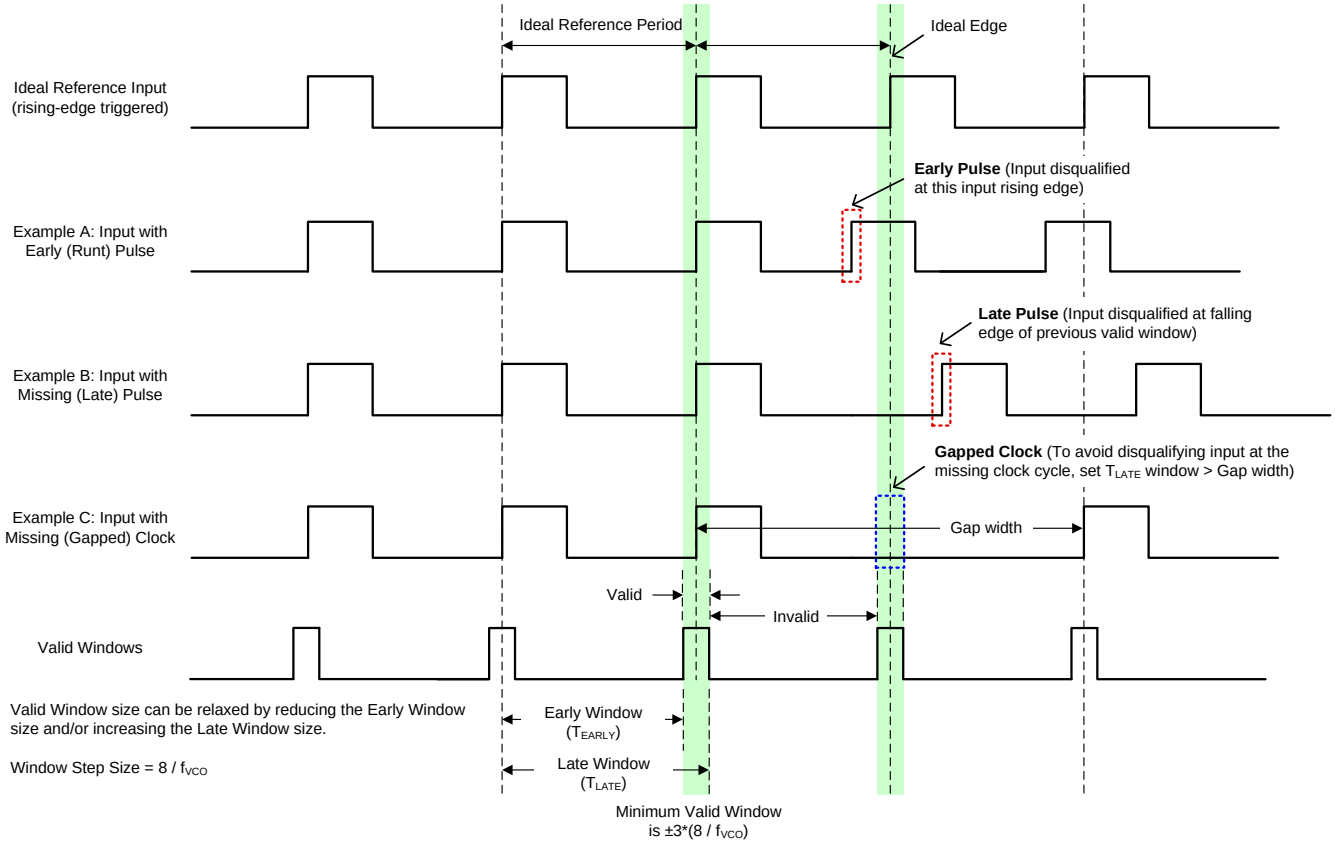


Figure 37. Early and Late Window Detector Examples

9.3.8.3.5 Frequency Monitoring

The precision frequency detector measures the frequency offset (in ppm) for all input clocks relative to a 0-ppm reference clock, which can be selected from either the XO or TCXO input. The valid and invalid ppm frequency thresholds are configurable through the registers. The monitor will clear its LOR_FREQ flag when the relative input frequency error is less than the valid ppm threshold. Otherwise, it will set the LOR_FREQ flag when the relative input frequency error is greater than the invalid ppm threshold. The ppm delta between the valid and invalid thresholds provides hysteresis to prevent the LOR_FREQ flag from toggling when the input frequency offset is crossing these thresholds.

A frequency measurement averaging factor is also used in computing the frequency detector register settings. A higher averaging factor increases the measurement delay to set or clear the flag, which allow more time for the input frequency to settle, and can also provide better measurement resolution for an input with high drift or wander. Note that higher averaging reduces the maximum frequency ppm thresholds that can be configured.

9.3.8.3.6 Phase Valid Monitor for 1-PPS Inputs

The phase valid monitor is designed specifically for 1-PPS input validation because the frequency and window detectors do not support this mode. The phase valid monitor uses a window detector to validate 1-PPS input pulses that arrive within the nominal clock period (T_{IN}) plus a programmable jitter threshold (T_{JIT}). When the input pulse arrives within the counter window (T_V), the pulse is considered valid and the phase valid flag will be cleared. When the input pulse does not arrive before T_V (due to a missing or late pulse), the flag will be set immediately to disqualify the input. T_{JIT} should be set higher than the worst-case input cycle-to-cycle jitter.

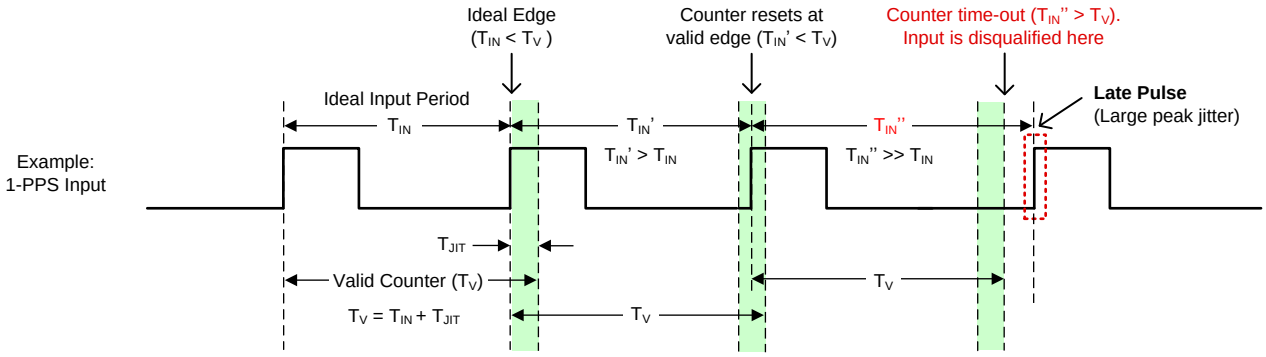


Figure 38. 1-PPS Input Window Detector Example

9.3.8.4 PLL Lock Detectors

The loss-of-lock (LOL) status is available for each APLL and DPLL. The APLLs are monitored for loss-of-frequency lock only. The REF-DPLLs are monitored for both loss-of-frequency lock (LOFL) and loss-of-phase lock (LOPL). The DPLL lock threshold and loss-of-lock threshold are programmable for both LOPF and LOFL detectors.

Each DPLL frequency lock detector will clear its LOFL flag when the DPLL's frequency error relative the selected reference input is less than the lock ppm threshold. Otherwise, it will set the LOFL flag when the DPLL's frequency error is greater than the unlock ppm threshold. The ppm delta between the lock and unlock thresholds provides hysteresis to prevent the LOFL flag from toggling when the DPLL frequency error is crossing these thresholds.

A measurement averaging factor is also used in computing the frequency lock detector register settings. A higher averaging factor increases the measurement delay to set or clear the LOFL flag. Higher averaging may be useful when locking to an input with high wander or when the DPLL is configured with a narrow loop bandwidth. Note that higher averaging reduces the maximum frequency ppm thresholds that can be configured.

Each DPLL phase lock detector will clear its LOPL flag when the DPLL's phase error is less than the phase lock threshold. Otherwise, it will set the LOPL flag when greater than the phase unlock threshold.

The APLL and DPLL lock detector flags can be observed through the status pins and the status bits.

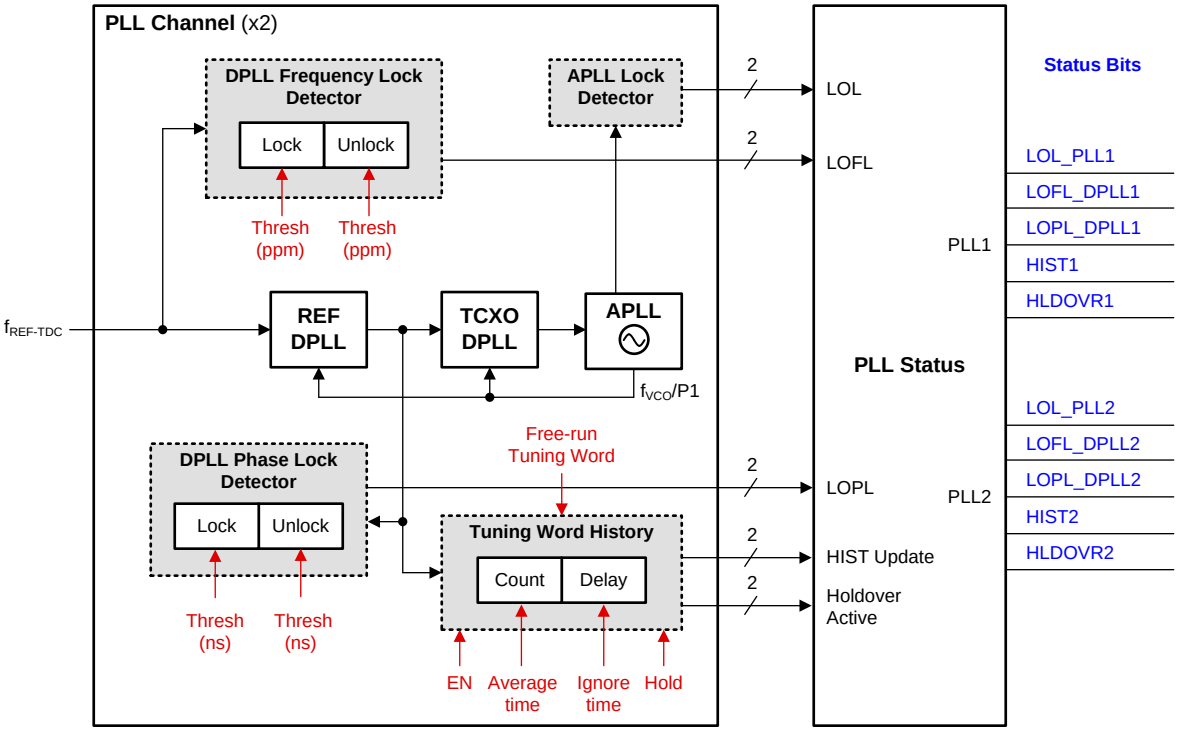


Figure 39. DPLL and APLL Lock Detectors

9.3.8.5 Tuning Word History

Each REF-DPLL domain has a tuning word history monitor block that determines the initial output frequency accuracy upon entry into holdover. The tuning word can be updated from one of three sources depending on the DPLL operating mode:

a. Locked Mode: From the output of the digital loop filter when locked
b. Holdover Mode: From the final output of the history monitor
c. Free Run Mode: From the free-run tuning word register (user defined)

When the history monitor is enabled and the DPLL is locked, it effectively averages the reference input frequency by accumulating history from the digital loop filter output during a programmable averaging time (T_{AVG}). Once the input becomes invalid, the final tuning word value is stored to determine the initial holdover frequency accuracy. Generally, a longer T_{AVG} time will produce a more accurate initial holdover frequency. The stability of the 0-ppm reference clock (XO or TCXO input) determines the long-term stability and accuracy of the holdover output frequency.

There is also a separate programmable delay timer (T_{IGN}) that can be set to ignore the history data that is corrupted just prior to entry into holdover. The history data could be corrupted if a tuning word update occurs while the input clock is failing and before it is detected by the input monitors. Both T_{AVG} and T_{IGN} times are programmable through the HISTCNT and HISTDLY register bits, respectively, and are related to the REF-TDC rate.

The tuning word history is initial cleared after a device hard reset or soft reset. The history monitor begins to accumulate history once the DPLL locks to a new reference. The previous history will be cleared when a switchover to a new reference occurs assuming the history persistence bit (HIST_HOLD) is not set. The history can be manually cleared by asserting the history soft reset bit (HIST_SW_RST). If the history persistence bit is set, the history monitor will not clear the previous history value during reference switchover, holdover exit, or history soft reset. Whenever the tuning word is cleared, the history monitor waits for the first T_{AVG} timer to expire before storing the first tuning word value.

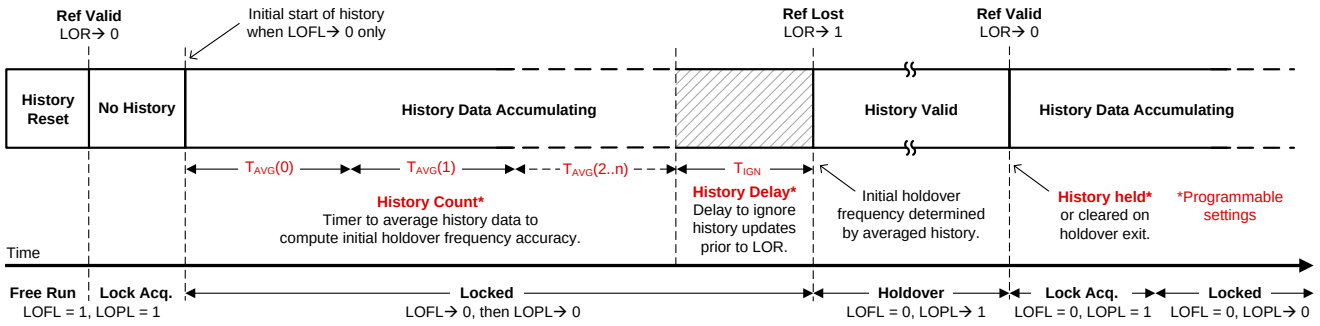


Figure 40. Tuning Word History Windows

If the T_{AVG} period is set very long (minutes or hours) to obtain a more precise historical average frequency, it is possible for a switchover or holdover event to occur before the first tuning word is stored and available for use. To overcome this, there is an intermediate history update option (HIST_INTMD). If the history is reset, then the intermediate average can be updated at intervals of $T_{AVG}/2^K$, where K = HIST_INTMD to 0, *during the first T_{AVG} period only*. If HIST_INTMD = 0, there is no intermediate update and the first average is stored after the first T_{AVG} period. However, if HIST_INTMD = 4, then four intermediate averages are taken at $T_{AVG}/16$, $T_{AVG}/8$, $T_{AVG}/4$, and $T_{AVG}/2$, as well as at T_{AVG}. After the first T_{AVG} period, all subsequent history updates occur at the T_{AVG} period.

When no tuning word history exists, the free-run tuning word value (TUNING_FREE_RUN) determines the initial holdover output frequency accuracy.

9.3.8.6 Status Outputs

STATUS[1:0] and GPIO[6:5] pins can be configured to output various status signals and interrupt flag for device diagnostic and debug purposes. The status signal, output driver type, and output polarity settings are programmable. The status output signals available at these pins for each device block monitored are listed in Equation 10. When the status signal is asserted, the status output will be active high (assuming the status polarity is not set to active low).

Table 8. Status Pin Signals Available per Device Block

DEVICE BLOCK MONITORED	STATUS SIGNAL (ACTIVE HIGH)
XO	XO Input Loss of Signal (LOS)
TCXO	TCXO Input Loss of Signal (LOS)
APLL1, APLL2	APLLx Lock Detected ($\overline{\text{LOL}}$)
	PLLx VCO Calibration Active
	APLLx N Divider, div-by-2
EEPROM	EEPROM Active
All Inputs and PLLs	Interrupt (INTR)
REF0 to REF3 (IN0 to IN3)	REFx Monitor Divider Output, div-by-2
	REFx Amplitude Monitor Fault
	REFx Frequency Monitor Fault
	REFx Missing or Early Pulse Monitor Fault
	REFx Validation Timer Active
	REFx Phase Validation Monitor Fault
DPLL1, DPLL2	DPLLx R Divider, div-by-2
	DPLLx REF N Divider, div-by-2
	DPLL TCXO M Divider, div-by-2
	DPLLx TCXO N Divider, div-by-2
	DPLLx REFn Selected
	DPLLx Holdover Active
	DPLLx Reference Switchover Event
	DPLLx Tuning History Update
	DPLLx Loss of Lock (LOFL)

9.3.8.7 Interrupt

Any of the four status pins can be configured as a device interrupt output pin. The interrupt configuration is set through registers. When the interrupt is enabled, the interrupt flag can be triggered from any combination of interrupt status indicators, including LOS for the XO, TCXO, and DPLL-selected inputs, LOL for each DPLL and APLL, and holdover and switchover events for each DPLL. Any status indicator can be masked so it will not trigger the interrupt pin. Any unmasked status indicator can have its polarity inverted before it is combined at the interrupt AND/$\overline{\text{OR}}$ gate and output to the status pin.

When the interrupt output is enabled and an interrupt flag is asserted by one or more fault conditions, the host device can read the sticky status registers to identify which flags were set, resolve any fault conditions in the system, and clear the flag by writing 0 to clear the sticky bits that were set.

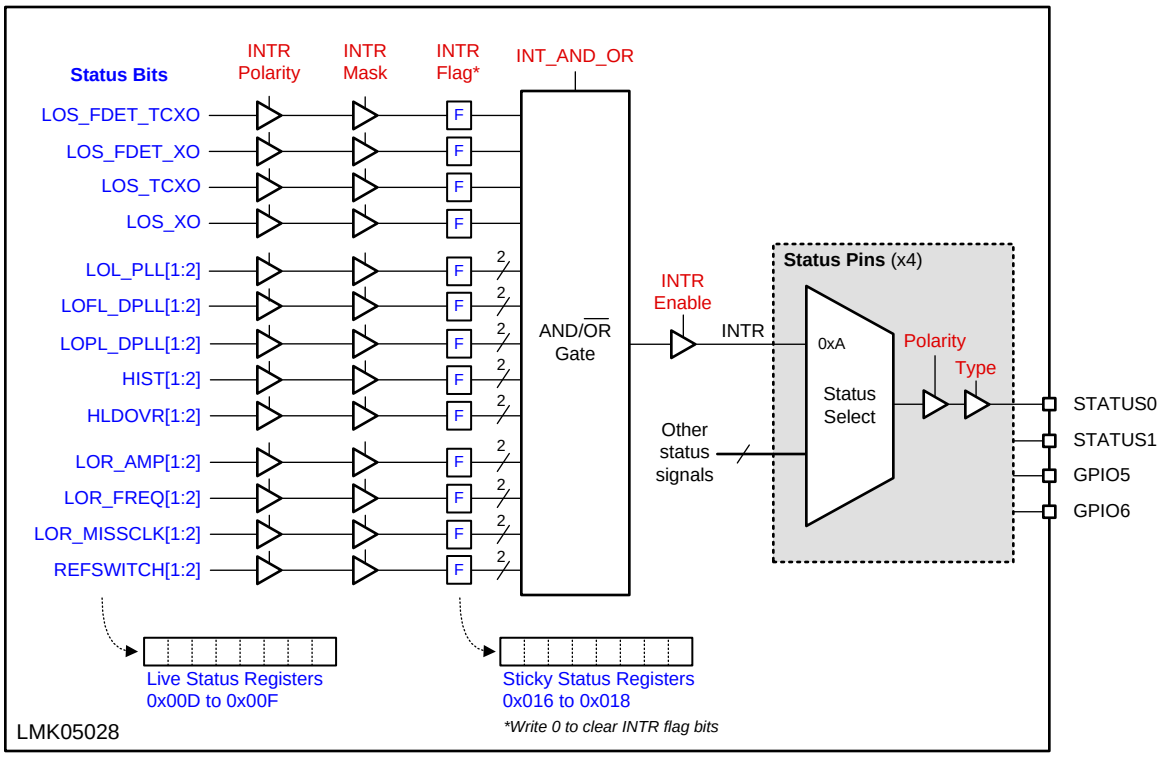


Figure 41. Status and Interrupt

9.3.9 PLL Channels

Figure 42 shows the 3-loop architecture implemented the same for both PLL channels with exception of the VCO frequency range. Each PLL channel can be configured independently in the different PLL modes described in *PLL Architecture Overview*.

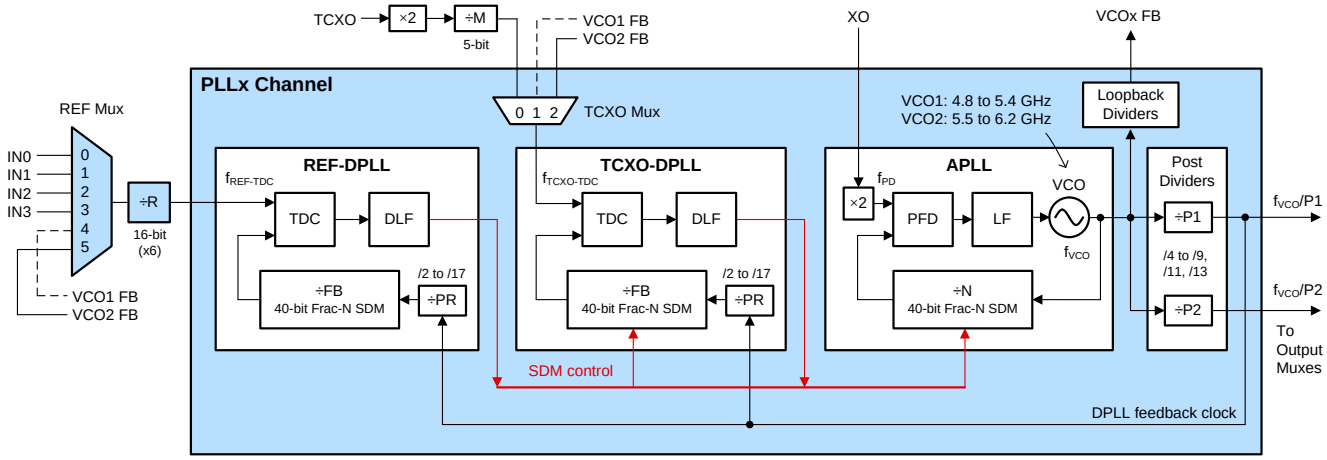


Figure 42. PLL Architecture (One Channel)

9.3.9.1 PLL Frequency Relationships

The following equations provide the PLL frequency relationships required to achieve closed-loop operation according to the selected PLL mode. The TICS Pro programming software can be used to generate valid divider settings based on the desired frequency plan configuration and PLL mode. The equations are applicable to both PLL channels.

- For 1-loop APLL mode, the condition in Equation 1 must be met.
- For 3-loop mode, the conditions in Equation 1, Equation 2, Equation 3, and Equation 4 must be met.
- For 2-loop mode (REF-DPLL), the conditions in Equation 1, Equation 3, and Equation 4 must be met.
- For 2-loop mode (TCXO-DPLL), the conditions in Equation 1 and Equation 2 must be met.

Equation 1 relates to the APLL:

$$f_{VCO} = f_{XO} \times D_{XO} \times (INT_{APLL} + NUM_{APLL} / DEN_{APLL}) \quad (1)$$

where

- f_{VCO}: VCO frequency
- f_{XO}: XO input frequency
- D_{XO}: APLL XO doubler (1 = disabled, 2 = enabled)
- INT_{APLL}: APLL N divider integer value (9 bits, 1 to 2^9-1)
- NUM_{APLL}: APLL N divider numerator value (40 bits, 0 to 2^{40}-1)
- DEN_{APLL}: APLL N divider denominator value (fixed, 2^{40})

Equation 2 relates to the TCXO-DPLL:

$$f_{VCO} = (f_{TCXO} \times D_{TCXO} / M_{TCXO}) \times P1_{PLL} \times PR_{TCXO} \times (INT_{TCXO} + NUM_{TCXO} / DEN_{TCXO}) \quad (2)$$

where

- f_{TCXO}: TCXO/OCXO input frequency
- D_{TCXO}: TCXO input doubler (1 = disabled, 2 = enabled)
- M_{TCXO}: TCXO input divide value (5 bits, 1 to 32)
- $P1_{PLL}$: PLL primary post-divider value (4 to 9, 11, 13)
- PR_{TCXO}: TCXO-DPLL FB prescaler divide value (2 to 17)
- INT_{TCXO}: TCXO-DPLL FB divider integer value (30 bits, 1 to 2^{30}-1)
- NUM_{TCXO}: TCXO-DPLL FB divider numerator value (40 bits, 0 to 2^{40}-1)
- DEN_{TCXO}: TCXO-DPLL FB divider denominator value (fixed, 2^{40})

Equation 3 relates to the REF-DPLL:

$$f_{VCO} = (f_{INx} / R_{INx}) \times P1_{PLL} \times PR_{REF} \times (INT_{REF} + NUM_{REF} / DEN_{REF}) \quad (3)$$

where

- f_{INx}: Reference input frequency (x = 0 to 3) or VCO loopback frequency (x = 4 or 5)
- R_{INx}: Reference input divide value (16 bits, 1 to 2^{16}-1) (x = 0 to 5)
- PR_{REF}: REF-DPLL FB prescaler divide value (2 to 17)
- INT_{REF}: REF-DPLL FB divider integer value (30 bits, 1 to 2^{30}-1)
- NUM_{REF}: REF-DPLL FB divider numerator value (40 bits, 0 to 2^{40}-1)
- DEN_{REF}: REF-DPLL FB divider denominator value (40 bits, 1 to 2^{40})

Equation 4 relates to any reference inputs assigned to a DPLL reference mux to achieve a constant REF-TDC rate required for proper input switchover.

$$f_{REF\text{-}TDC} = f_{IN0}/R_{IN0} = f_{IN1}/R_{IN1} = f_{IN2}/R_{IN2} = f_{IN3}/R_{IN3} \quad (4)$$

Equation 5, Equation 6, Equation 7, Equation 8, and Equation 9 relate to the output frequency according to the output channel mux selection (CHxMUX).

$$f_{CHxMUX} = f_{VCOy} / Pn_{PLLy} \text{ when PLLy post-divider is selected} \quad (5)$$

$$f_{CHxMUX} = f_{XO} \text{ when XO is selected (OUT0 or OUT1)} \quad (6)$$

$$f_{CHxMUX} = f_{TCXO/REF} \text{ when TCXO or REF is selected (OUT0 or OUT1)} \quad (7)$$

$$f_{OUTx} = f_{CHxMUX} / OD_{OUTx} \text{ (OUT1 to OUT6)} \quad (8)$$

$$f_{OUTx} = f_{CHxMUX} / (DIVA_{OUTx} \times DIVB_{OUTx}) \text{ (OUT0 or OUT7 only)}$$

where

- f_{CHxMUX}: Output channel mux frequency (from PLL post-divider, XO, or TCXO/Ref Bypass mux)
- $f_{TCXO/REF}$: TCXO, DPLL1 Ref, or DPLL2 Ref input frequency (selected by TCXO/Ref Bypass mux)
- f_{OUTx}: Output clock frequency (x = 0 to 7)
- Pn_{PLLy}: PLLy P1 (primary) or P2 (secondary) post-divider value (4 to 9, 11, 13)
- OD_{OUTx}: Output divide value (20 bits, 1 to 2^{20}-1)
- ODB_{OUTx}: Output MSB divide value for OUT0 or OUT7 (11 bits, 1 to 2^{11}-1) (9)

9.3.9.2 Analog PLL (APLL)

The APLL has a 40-bit fractional-N divider to support high-resolution frequency synthesis, wide output frequency range, very low phase noise and jitter, and the ability to tune its VCO frequency through sigma-delta modulator (SDM) control.

The APLL XO doubler doubles the XO input frequency into the phase frequency detector (PFD) input. The APLL multiplies the PFD frequency by the total N divider value to generate the VCO clock. The desired VCO output to PFD input frequency ratio is the total value of N (INT + NUM/DEN) applied to the SDM to tune the VCO frequency.

In free-run mode, the APLL uses a low-jitter XO input as a initial reference clock to lock the internal voltage controlled oscillator (VCO). The PFD compares the fractional-N divided clock with the XO doubler frequency and generates a control signal. The control signal is filtered by the APLL loop filter to generate the VCO's control voltage that sets its output frequency. The SDM modulates the N divider ratio to get the desired fractional ratio between the PFD input and the VCO output.

In 2-loop or 3-loop mode, the APLL's SDM is controlled by one of the DPLL loops to pull the VCO frequency into lock with the DPLL reference input.

9.3.9.3 APLL XO Doubler

The APLL has a XO doubler that can be enabled to double the PFD frequency up to 200 MHz. The doubler adds minimal noise and is useful for raising the PFD frequency for better phase noise and jitter and also to avoid spurs. When the PFD frequency is increased, the flat portion of the APLL phase noise improves.

9.3.9.4 APLL Phase Frequency Detector (PFD) and Charge Pump

The APLL PFD frequency can operate from 10 MHz to 200 MHz, but the APLL performance is optimized for frequencies of 96 MHz or higher. The PLL has programmable charge pump settings of 1.6, 3.2, 4.8, or 6.4 mA.

9.3.9.5 APLL Loop Filter

The APLL supports programmable loop bandwidth from 100 kHz and 1 MHz. The loop filter components can be programmed to optimize the APLL bandwidth depending on the XO frequency and phase noise without changing any external components. The LF1 and LF2 pins each require an external C2 capacitor to ground, typically 0.1-µF. Figure 43 shows the APLL loop filter structure between the PFD/charge pump output and VCO control input.

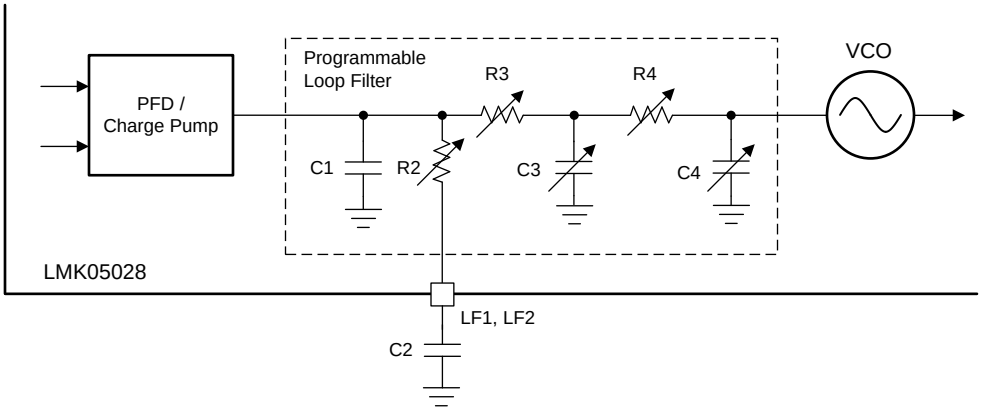


Figure 43. Loop Filter Structure of Each APLL

9.3.9.6 APLL Voltage Controlled Oscillator (VCO)

Each PLL contains fully-integrated LC-based oscillators with very low phase noise. The VCO takes the voltage from the loop filter and converts this into a frequency. The tuning range of VCO1 is 4.8 to 5.4 GHz, and the tuning range of VCO2 is 5.5 to 6.2 GHz. The two VCO frequency ranges are spaced apart to cover a wide range of frequency configurations and to help minimize cross-coupling between the two PLL domains.

9.3.9.6.1 VCO Calibration

Each PLL's VCO must be calibrated to ensure that the PLL can achieve lock and deliver optimal phase noise performance. Fundamentally, the VCO calibration establishes an optimal operating point within the tuning range of the VCO. The VCO calibration is executed automatically during initial PLL start-up after device power-on, hard reset, or soft reset once the XO input is detected by its input monitor. To ensure proper VCO calibration, it is critical for the XO clock to be stable in amplitude and frequency prior to the start of VCO calibration; otherwise, the VCO calibration can fail and prevent start-up of the PLL and its output clocks. Prior to VCO calibration and APLL lock, the output drivers are typically held in the mute state (configurable per output) to prevent spurious output clocks.

To trigger VCO calibration for one PLL channel without affecting the other channel, this can be achieved through host programming by either entering/exiting PLL power-down (PLLx_PDN register bit) or by asserting a PLL soft-reset (SWRxPLL register bit).

9.3.9.7 APLL VCO Post-Dividers (P1, P2)

The APLL has a primary (P1) and secondary (P2) VCO post-divider for flexible clock frequency planning. All post-divider supports divide by 4 to 9, 11, or 13. The post-divider clocks for both PLLs are distributed to all output channel muxes for selection. The primary (P1) post-divider output is also fed back to the FB divider paths of the REF-DPLL and TCXO-DPLL to close the loops.

After the P1 divider and DPLL fractional FB divider values have been determined for closed-loop operation, the P1 divider value should not be modified dynamically because it would affect the FB divider clock frequency to the TDC of the DPLL. If the P1 divider must be changed, it is necessary to re-compute the DPLL FB divider values. Also, changing any PLL post-divider value requires a PLL soft-reset (or device soft-reset) to reset the divider for proper operation.

9.3.9.8 APLL Fractional N Divider (N) With SDM

The APLL fractional N divider includes a 9-b integer portion (INT), 40-b numerator portion (NUM), a fixed 40-b denominator portion (DEN), and sigma-delta modulator. The INT and NUM are programmable, while the denominator is fixed to 2^{40} for highest frequency resolution (step size) on the output. The total N divider value is: N = INT + NUM / DEN.

9.3.9.9 REF-DPLL Reference Divider (R)

The reference clock input paths to each REF-DPLL features a 16-b reference divider (R) for each clock input (IN0 to IN3). The output of each R divider sets the frequencies to the reference input mux and the TDC rate of the REF-DPLL. There are also two additional R dividers for the internal VCO loopback clocks (IN4 and IN5) that could be used in cascaded PLL configurations. IN4 refers to the VCO1 loopback clock to DPLL2 reference input, and IN5 refers to the VCO2 loopback clock to DPLL1 reference input. To support hitless switching between inputs with different frequencies, the R divider can be used to divide the clocks to a single common frequency to the REF-DPLL TDC input.

9.3.9.10 TCXO/OCXO Input Doubler and M Divider

The TCXO/OCXO input features a frequency doubler followed by a 5-b M divider. The M divider output is sent to the TCXO mux of both TCXO-DPLLs.

9.3.9.11 TCXO Mux

Each PLL channel has a TCXO mux to select the TCXO-DPLL input from either the TCXO M divider clock, or the VCO loopback clock from the opposite PLL channel when PLL cascading is used. When the TCXO M divider is selected, the M Divider frequency sets the TCXO-TDC rate. When the VCO loopback clock is selected, the VCO loopback divider frequency from the opposite PLL sets the TCXO-TDC rate.

9.3.9.12 REF-DPLL and TCXO-DPLL Time-to-Digital Converter (TDC)

The TDCs for the REF-DPLL and TCXO-DPLL operate up 30 MHz. The TDC resolution is fine enough to achieve in-band phase noise of –112 dBc/Hz at 100-Hz offset for a 122.88-MHz output.

When the REF mux selects a reference input clock, the REF-DPLL TDC rate is:

$$f_{REF\text{-}TDC} = f_{INx} / R_{INx} \quad (10)$$

When the REF mux selects the VCO loopback clock, the REF-DPLL TDC rate is:

$$f_{REF\text{-}TDC} = f_{VCOa} / (48 \times DIV_{DPLLa\_CLK\_FB}) / R_{INx} \quad (11)$$

When the TCXO mux selects the M divider clock, the TCXO-DPLL TDC rate is:

$$f_{TCXO\text{-}TDC} = f_{TCXO} \times D_{TCXO} / M_{TCXO} \quad (12)$$

When the TCXO mux selects the VCO loopback clock, the TCXO-DPLL TDC rate is:

$$f_{TCXO\text{-}TDC} = f_{VCOa} / (48 \times DIV_{DPLLa\_CLK\_FB})$$

where

- f_{VCOa}: VCO frequency fed back from the first PLL channel (PLLa) in a cascaded configuration
- $DIV_{DPLLy\_CLK\_FB}$: VCO loopback divide value (3 to 32) from PLLa (13)

9.3.9.13 REF-DPLL and TCXO-DPLL Loop Filter

Each REF-DPLL and TCXO-DPLL supports programmable loop bandwidth from 10 mHz to 4 kHz and can achieve jitter peaking below 0.1 dB (typical). The low-pass jitter transfer characteristic of each DPLL attenuates its reference input noise with up to 60-dB/decade roll-off above the loop bandwidth.

In 3-loop mode, the REF-DPLL loop filter output modulates the TCXO-DPLL's SDM, and the TCXO-DPLL loop filter output correspondingly modulates the APLL's SDM to steer the APLL VCO into lock with the selected REF-DPLL input.

In 2-loop REF-DPLL mode, the TCXO-DPLL is not used and the REF-DPLL loop filter output controls the APLL's SDM to steer the VCO frequency into lock with the selected REF-DPLL input.

In 2-loop TCXO-DPLL mode, the REF-DPLL is not used and the TCXO-DPLL loop filter output controls the APLL's SDM to steer the VCO frequency into lock with the TCXO input.

9.3.9.14 REF-DPLL and TCXO-DPLL Feedback Dividers

The feedback path of each REF-DPLL and TCXO-DPLL has a feedback prescaler (PR) followed by a fractional FB divider. The prescaler divides the PLL primary post-divider (P1) clock by a programmable value from 2 to 17, which then clocks the FB divider. The FB divider of each REF-DPLL and TCXO-DPLL includes a 30-b integer portion (INT), 40-b numerator portion (NUM), and 40-b denominator portion (DEN). The total FB divider value is: FB = INT + NUM / DEN. All DPLL feedback dividers are programmable, except for the DEN_{TCXO} (fixed, 2^{40}). The FB divider clock must match the TDC rate determined by the TDC input path of the respective DPLL.

The REF-DPLL TDC rate is:

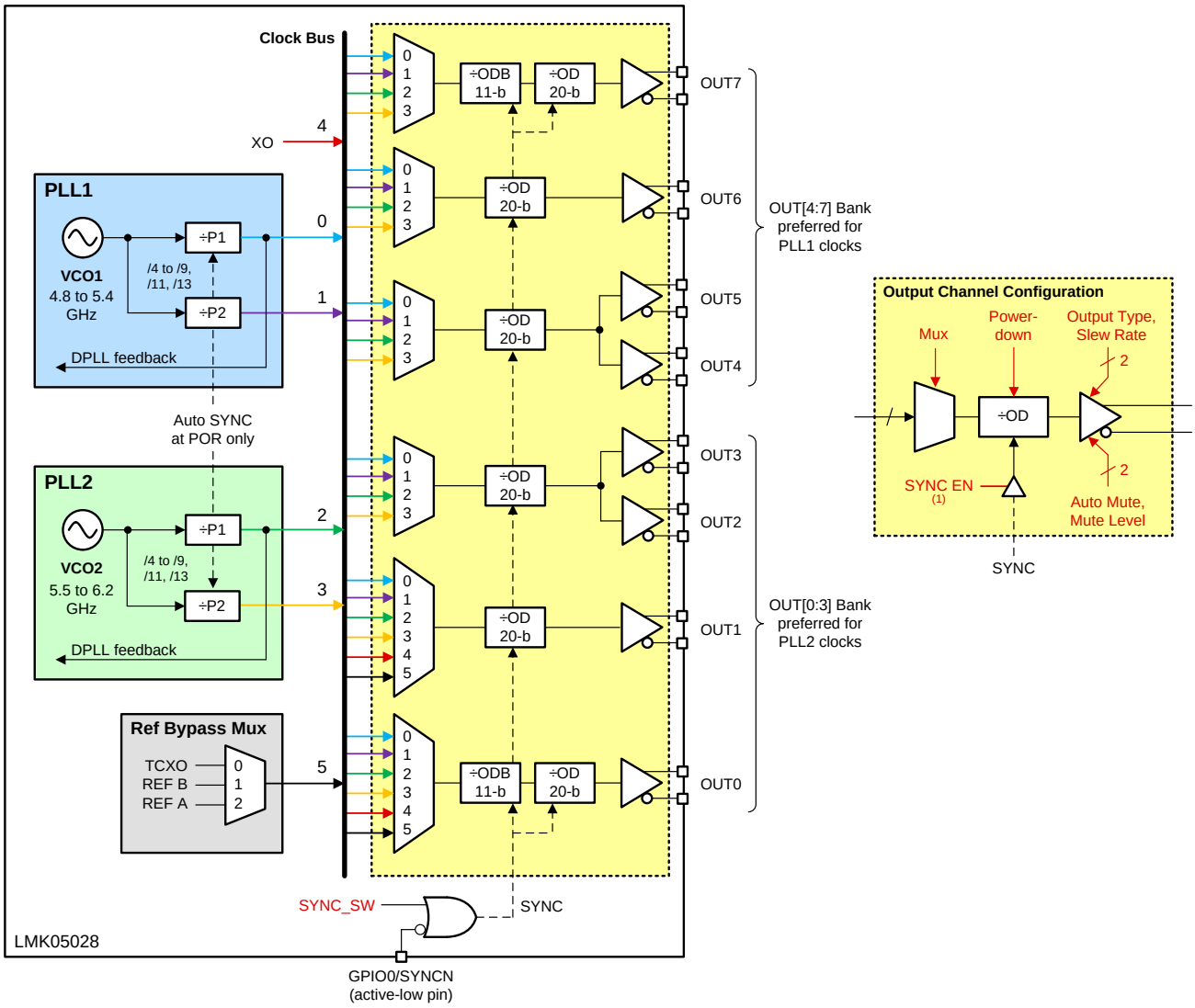
$$f_{REF\text{-}TDC} = f_{VCO} / (P1_{PLL} \times PR_{REF} \times FB_{REF}) \quad (14)$$

The TCXO-DPLL TDC rate is:

$$f_{TCXO\text{-}TDC} = f_{VCO} / (P1_{PLL} \times PR_{TCXO} \times FB_{TCXO}) \quad (15)$$

9.3.10 Output Clock Distribution

The output clock distribution blocks shown in Figure 44 includes six output muxes, a TCXO/Ref Bypass mux, six output dividers, and eight programmable output drivers. The output dividers support output synchronization (SYNC) to allow phase synchronization between two or more output channels. Also, each output bank (OUT[0:3] and OUT[4:7]) has separate a zero-delay feedback path to support the zero-delay mode option available on each DPLL channel.



(1) SYNC Enable logic: SYNC EN = ((CH[z]_SYNCEN) && (PLL[x]_[y]_CH[zz]_SYNC_BANK)) where [x]: PLL = 1 or 2, [y]: Post-Div = PRI or SEC (÷P1 or P2), [z]: CH = 0, 1, 23, 45, 6, or 7, and [zz]: Bank = 03 or 47.

Figure 44. Output Clock Distribution

9.3.11 Output Channel Muxes

Each of the six output channels has as output mux. Each output mux for OUT2 through OUT7 can individually select between the PLL1 and PLL2 post-divider clocks. Each output mux for OUT0 and OUT1 can individually select between the PLL1 and PLL2 post-divider clocks, the XO clock, or one of the clocks from the TCXO/Ref Bypass Mux.

9.3.11.1 TCXO/Ref Bypass Mux

The TCXO/Ref bypass mux can select between the TCXO clock, the selected DPLL1 input (REF A), or the selected DPLL2 input (REF B). The bypass clocks are primarily intended for diagnostic purposes and not optimized for lowest phase noise or jitter.

9.3.12 Output Dividers

Each of the six output channels has an output divider after the output mux. OUT2 and OUT3 share an output divider, as do OUT4 and OUT5. OUT0, OUT1, OUT6, and OUT7 have their own output dividers. The output divider is used to generate the final output clock frequency from the source selected by the output mux.

OUT1 to OUT6 channels have 20-bit dividers that can support output frequencies from 2 kHz to 750 MHz (or up to the maximum f_{OUT} frequency for the configured output driver type). It is possible to configure the PLL post-divider and output divider to achieve higher clock frequencies, but the driver's output swing may fall out of specification depending on the output type).

OUT0 and OUT7 channels each have cascaded 11-bit (MSB) and 20-bit (LSB) output dividers to support output frequencies from 1 Hz (1 PPS) to 750 MHz. In this case, the total output divide value is the product of the MSB and LSB output divider values.

Each output divider is powered from the same VDDO_x supply used for the clock output drivers. The output divider can be powered down if not used to reduce power. Each output divider is automatically powered down when its output driver is powered down, or when both output drivers are powered down for OUT[2:3] or OUT[4:5].

9.3.13 Clock Outputs (OUTx_P/N)

Each clock output can be individually configured as a differential driver (AC-LVDS/CML/LVPECL), HCSL driver, or LVCMOS driver (1.8 V or 2.5 V). Otherwise, it can be powered down if not used. OUT2 and OUT3 share an output supply, as do OUT4 and OUT5. OUT0, OUT1, OUT6, and OUT7 have their own output supplies. Each output supply can be separately powered by 1.8 V, 2.5 V, or 3.3 V for a differential or HCSL output, or 1.8 V or 2.5 V for an LVCMOS output. Each output channel has its own internal LDO regulator to provide excellent power supply noise rejection (PSNR) and minimize supply-noise induced jitter and spurs. The output clock specifications (for example, output swing, phase noise, jitter, and so forth) for differential and HCSL drivers are not sensitive to the VDDO_x voltage because these driver modes are powered through the channel's internal LDO regulator. When an output channel is left unpowered, the channel does not generate any clocks and will not interfere with other output channels that are powered-on.

Table 9. Output Driver Modes

OUT_x_TYPE	OUTPUT TYPE
00h	Disabled
10h	AC-LVDS
14h	AC-CML
18h	AC-LVPECL
2Ch	HCSL (External 50-Ω to GND)
2Dh	HCSL (Internal 50-Ω to GND)
30h	LVCMOS (HiZ / HiZ)
32h	LVCMOS (HiZ / –)
33h	LVCMOS (HiZ / +)
35h	LVCMOS (Low / Low)
38h	LVCMOS (– / HiZ)
3Ah	LVCMOS (– / –)
3Bh	LVCMOS (– / +)
3Ch	LVCMOS (+ / HiZ)
3Eh	LVCMOS (+ / –)
3Fh	LVCMOS (+ / +)

9.3.13.1 AC-Differential Output (AC-DIFF)

The differential output driver uses a switched-current mode type shown in Figure 45. A programmable tail current of 4, 6, or 8 mA (nominal) is used to achieve V_{OD} swing compatible with AC-coupled LVDS, CML, or LVPECL receivers, respectively, across a 100-Ω differential termination. The differential output driver is ground-referenced (similar to a HCSL driver), meaning the differential output has a low common-mode voltage (V_{OS}).

The differential driver is internally biased and does not need any external pullup or pulldown resistors, unlike conventional CML or LVPECL drivers. The differential output should be interfaced through external AC-coupling to a differential receiver with proper input termination and biasing.

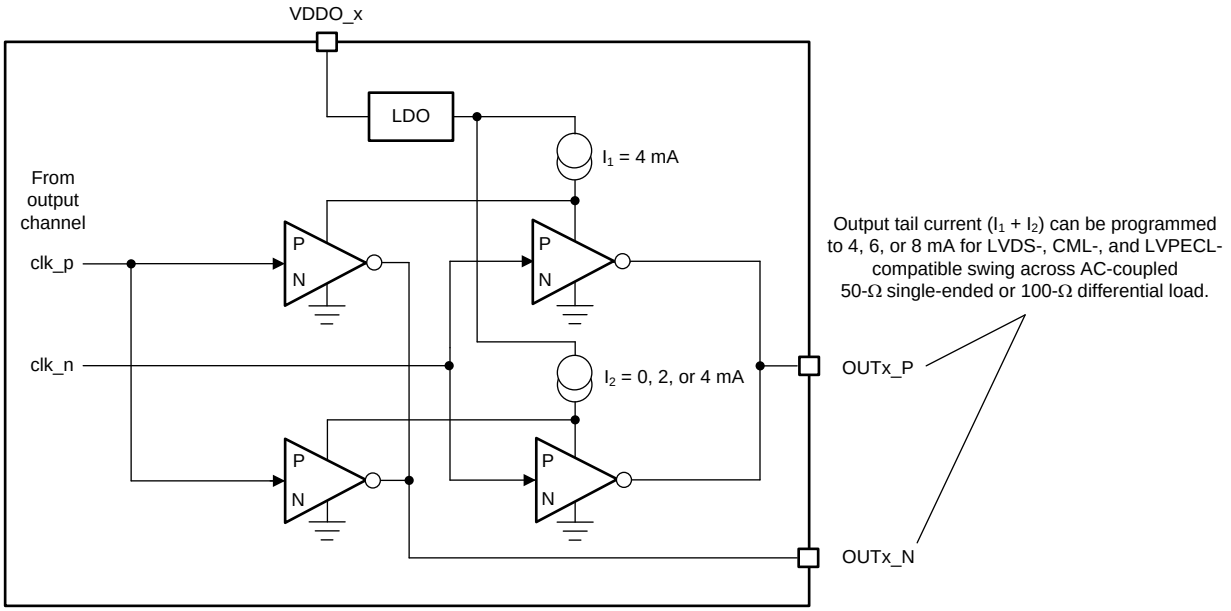


Figure 45. AC-LVDS/CML/LVPECL Output Driver Structure

9.3.13.2 HCSL Output

The HCSL output driver is an open-drain type, which should be DC-coupled to an HCSL receiver. The HCSL output has programmable, internal 50-Ω to ground (on P and N) for source termination, which can be enabled when the receiver does not provide input (load) termination. If the internal termination is disabled, external 50-Ω termination to ground (on P and N) is required at either the driver side (source terminated) or receiver side (load terminated).

9.3.13.3 LVCMOS Output (1.8 V, 2.5 V)

The LVCMOS driver has two outputs per pair. Each output on P and N can be configured for normal polarity, inverted polarity, or disabled as HiZ or static low level. The LVCMOS output high level (V_{OH}) is determined by the VDDO_x voltage of 1.8 V or 2.5 V for rail-to-rail LVCMOS output voltage swing. If a VDDO_x voltage of 3.3 V is applied, the V_{OH} level not will not swing to the VDDO_x rail due to the dropout voltage of the channel's internal LDO regulator.

Because an LVCMOS output clock is a high-swing and unbalanced signal, it can be a strong aggressor and couple noise onto other jitter-sensitive differential output clocks. If an LVCMOS clock is required from an output pair, configure the pair with both outputs enabled but with opposite polarity (+/– or –/+) and leave the unused output floating with no trace connected.

9.3.13.4 Output Auto-Mute During LOL or LOS

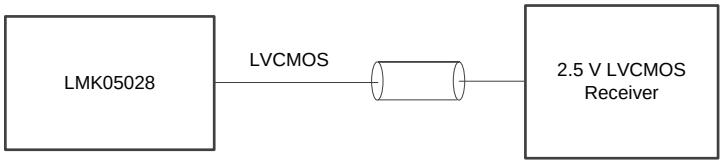
Each output driver can automatically mute or squelch its clock when the selected output mux clock source is invalid, as configured by its CH_x_MUTE bit. If the selected clock source is derived from a PLL post-divider output, the source can be invalid based on the LOL status of each PLL by configuring the APLL and DPLL mute control bits (MUTE_APLLx_LOCK, MUTE_DPLLx_LOCK, MUTE_DPLLx_TCXO). If the selected source is a bypass clock (XO or TCXO), the source is invalid when a LOS is detected on the input. The mute level can be configured per output channel by its CHx_MUTE_LVL bits, where the mute level depends on the configured output driver type (Differential/HCSL or LVCMOS). The mute level for a differential or HCSL driver can be set to output common mode, differential high, or differential low levels. The mute level for a LVCMOS driver pair can be set to output low level for each of its outputs (P and N) independently. When auto-mute is disabled or bypassed (CH_x_MUTE = CHx_MUTE_LVL = 0), the output clock can have incorrect frequency or be unstable before and during the VCO calibration if derived from a PLL. For this reason, the mute bypass mode should only be used for diagnostic or debug purposes.

9.3.14 Glitchless Output Clock Start-Up

When output auto-mute is enabled, any output derived from a PLL will start up in synchronous fashion without clock glitches when PLL lock is achieved after any the following events: device power-on, exiting hard reset (PDN pin), exiting soft reset (RESET_SW bit), or exiting PLL reset (PLLx_PDN bit). The output clock will also start up without glitches after any of the following events: VDDO_x is ramped (even when delayed after the device initialization), exiting channel soft reset (CHxPWDN bit), or deassertion of output SYNC (assuming SYNC_MUTE bit is set).

9.3.15 Clock Output Interfacing and Termination

Figure 46 to Figure 50 show the recommended output interfacing and termination circuits. Unused clock outputs can be left floating and powered down by programming.



Same applies for 1.8-V LVCMOS output to 1.8-V LVCMOS receiver.

Figure 46. 2.5-V LVCMOS Output to 2.5-V LVCMOS Receiver

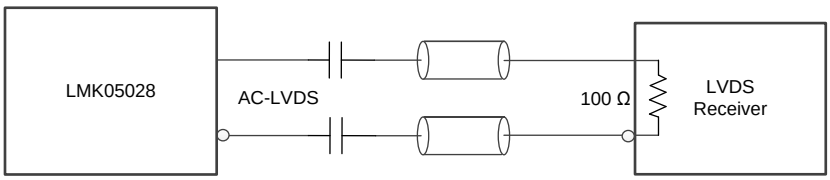


Figure 47. AC-LVDS Output to LVDS Receiver With Internal Termination/Biasing

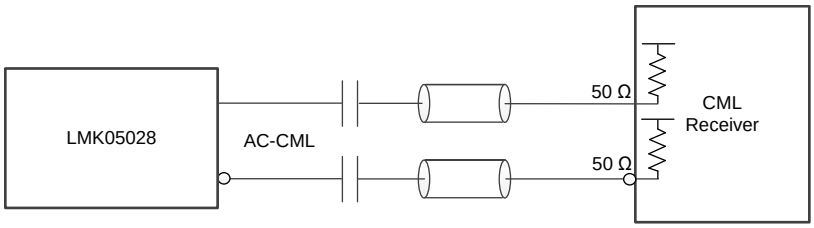


Figure 48. AC-CML Output to CML Receiver With Internal Termination/Biasing

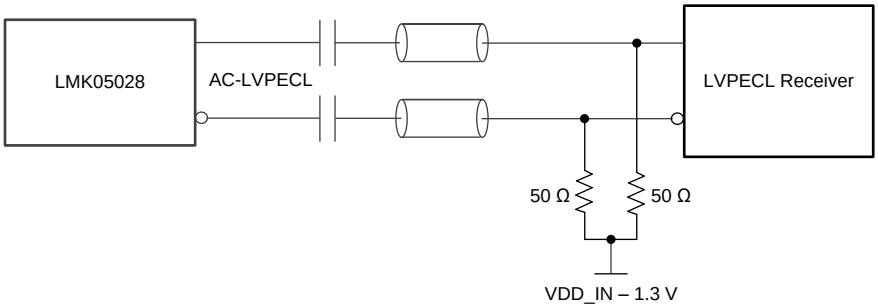
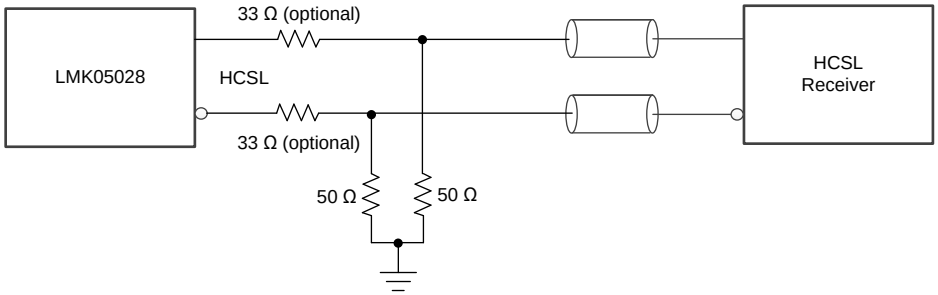


Figure 49. AC-LVPECL Output to LVPECL Receiver With External Termination/Biasing



If HCSL Internal Termination (50-Ω to GND) is enabled, replace 33-Ω with 0-Ω and remove 50-Ω external resistors.

Figure 50. HCSL Output to HCSL Receiver With External Source Termination

9.3.16 Output Synchronization (SYNC)

Output SYNC can be used to align two or more output clocks to be phase-aligned at a common rising edge by allowing the output dividers to exit reset on the same PLL post-divider clock cycle. Any output dividers selecting the same PLL post-divider can be synchronized together as a *SYNC group* by triggering a SYNC event through the hardware pin or software bit.

The following requirements must be met establish a SYNC group for two or more output channels:

- Output dividers have their respective sync enabled (CHx_SYNCEN bit = 1).
- Output dividers have their output mux selecting the same PLL primary post-divider (for example, PLL1 P1 or PRI, PLL1 P2 or SEC).
- The PLL post-divider (PRI and/or SEC) must have the applicable sync bank bit(s) enabled for the output divider bank(s). Examples:
  - PLL1_PRI_CH47_SYNC_BANK should be set when output dividers in OUT[4:7] bank will be synced to PLL1 P1 (PRI).
  - PLL1_SEC_CH03_SYNC_BANK should be set when output dividers in OUT[0:3] bank will be synced to PLL1 P1 (SEC).

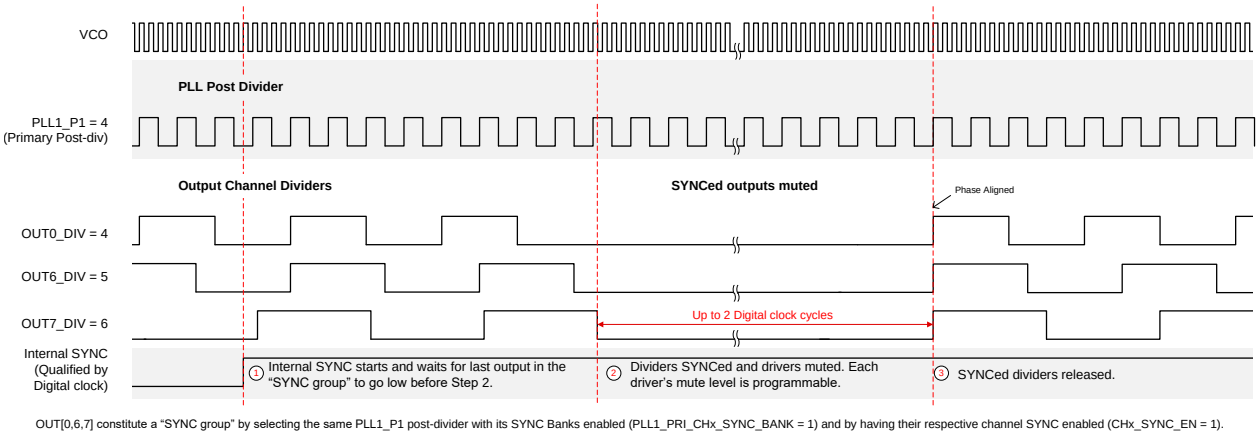
A SYNC event can be asserted by the hardware GPIO0/SYNCN pin (active low) or the SYNC_SW register bit (active high). When SYNC is asserted, the SYNC-enabled dividers held are reset and clock outputs are muted. The divider reset and output muting is done synchronously, allowing the outputs to finish their final clock cycle (to avoid a short clock period) before the actual SYNC event. When SYNC is deasserted, the outputs will start with their initial clock phases synchronized or aligned. SYNC can also be used to mute any SYNC-enabled outputs to prevent output clocks from being distributed to down-stream devices until they are configured and ready to accept the incoming clock. The SYNC signal is internally qualified or sampled by the internal digital system clock that runs at 10 MHz nominal. The negative pulse applied to the SYNCN input pin should be greater than 200 ns to be captured by the internal digital system clock. SYNC deassertion can take two cycles of the digital clock before the outputs are released.

Output channels with their sync disabled (CHx_SYNCEN bit = 0) will not be affected by a SYNC event and will continue normal output operation as configured. Also, VCO and PLL post-divider clocks do not stop running during the SYNC so they can continue to source any output channels that do not require synchronization. Output dividers with divide-by-1 (divider bypass mode) are not gated during the SYNC event. Also, SYNC should be disabled and is not supported when the output mux is selecting the XO, TCXO, or DPLL reference clocks.

Table 10. Output Synchronization

GPIO0 PIN	SYNC_SW BIT	OUTPUT DIVIDER AND DRIVER STATE
0	1	Output driver(s) muted and output divider(s) reset
0→1	1→0	Outputs in a SYNC group are unmuted with their initial clock phases aligned
1	0	Normal output driver/divider operation as configured

Figure 51 shows an example of the SYNC timing example for a SYNC group. The SYNC group is comprised of OUT0, OUT6, and OUT7 dividers, which are sourced by the PLL1 P1 (primary) post-divider. Notice that the output divider reset and output mute is applied synchronously by waiting until the last output clock in the group goes low (OUT7).



(1) The VCO clock and PLL post-divider clock do not stop running during the SYNC.

Figure 51. Output SYNC Group Timing Example

9.3.17 Zero-Delay Mode (ZDM) Configuration

Zero-delay mode can be enabled to achieve zero phase delay between the selected reference input clock and the output clocks of a DPLL. As shown in Figure 52 and Figure 53, DPLL1 supports zero-delay for OUT4/5, OUT6, and OUT7, while DPLL2 supports zero-delay for OUT0, OUT1, and OUT2/3. Any output that requires the zero-delay feature should be derived from the PLL's P1 (primary) post-divider and have zero-delay enabled (DPLLx_ZDM_EN bit = 1). Then, one of the outputs per DPLL can be selected as the primary zero-delay output (by O_CHx_y_ZERODLY_EN bit). Other outputs that need zero-delay can be synchronized with the primary zero-delay output by comprising a SYNC group (see *Output Synchronization (SYNC)*). ZDM and DCO mode should not be enabled at the same time within a PLL channel.

When the DPLL is acquiring lock to the reference input, the initial phase lock is governed by the DPLL fastlock bandwidth. Once phase lock is detected, the final output phase alignment with the input reference is governed by the normal DPLL loop bandwidth. The same phase lock and alignment process also occurs when exiting holdover or after a switchover event.

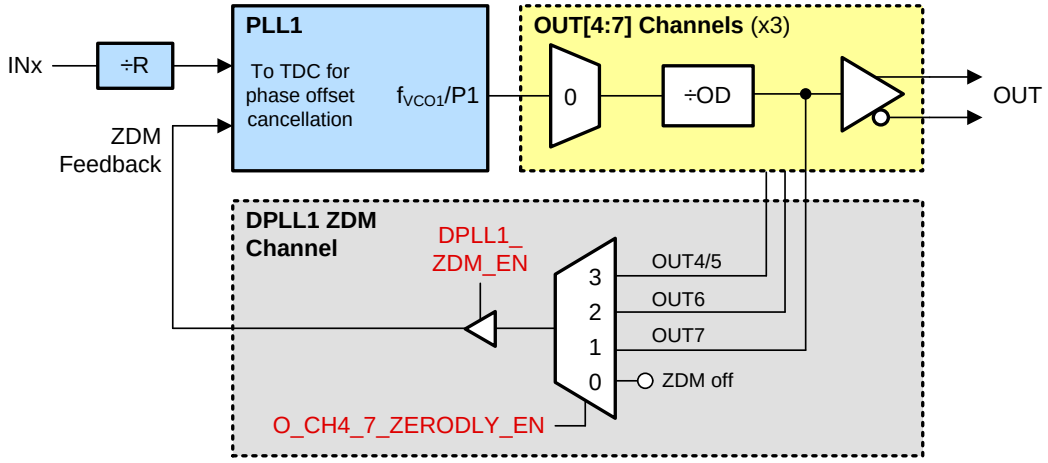


Figure 52. DPLL1 ZDM Configuration for OUT4 to OUT7

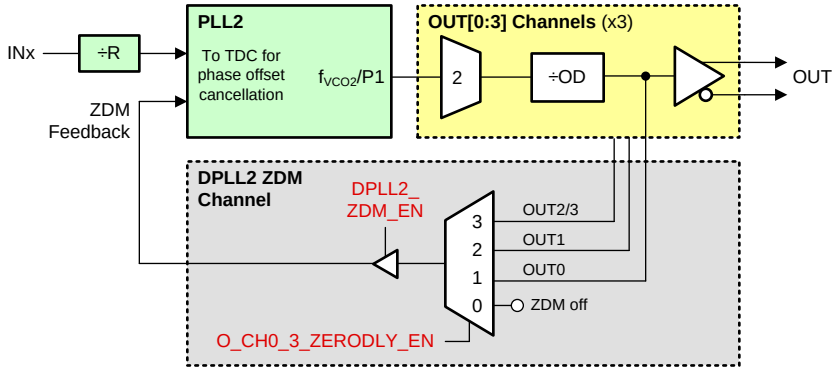


Figure 53. DPLL2 ZDM Configuration for OUT0 to OUT3

9.3.18 PLL Cascading With Internal VCO Loopback

PLL cascading can be used when the second PLL (either PLL1 or PLL2) must be precisely locked to the frequency of the first PLL. The internal VCO loopback configuration options are implemented identically on both PLL channels, allowing PLL2 to be cascaded after PLL1 or vice versa. The internal VCO loopback clock from the first PLL can drive the REF-DPLL input path or the TCXO-DPLL input path if the TCXO loopback enable control is set. The second PLL can have reference validation enabled to qualify the VCO loopback clock from the first PLL stage to ensure that the second PLL stage has a stable and valid clock input from the first PLL stage before it acquires lock. The VCO loopback clock can be validated based on when the first PLL stage achieves frequency lock and/or phase lock on the REF-DPLL or frequency lock on the TCXO-DPLL. Once the VCO loopback clock is validated based on the enabled criteria, then the second PLL stage can begin to acquire lock. The VCO loopback dividers, loopback mux, and loopback reference validation options are programmable.

In the example shown in Figure 54, PLL2 is cascaded and locked to PLL1's internal VCO1 loopback clock through the two loopback dividers (fixed and programmable) and TCXO loopback muxes. PLL2 operates with a wide loop bandwidth to precisely track the DCO frequency adjustments applied to PLL1. This effectively applies DCO adjustments to both clock domains simultaneously, which would not be possible if both loops were operating in parallel (not cascaded) with separate DCO controls.

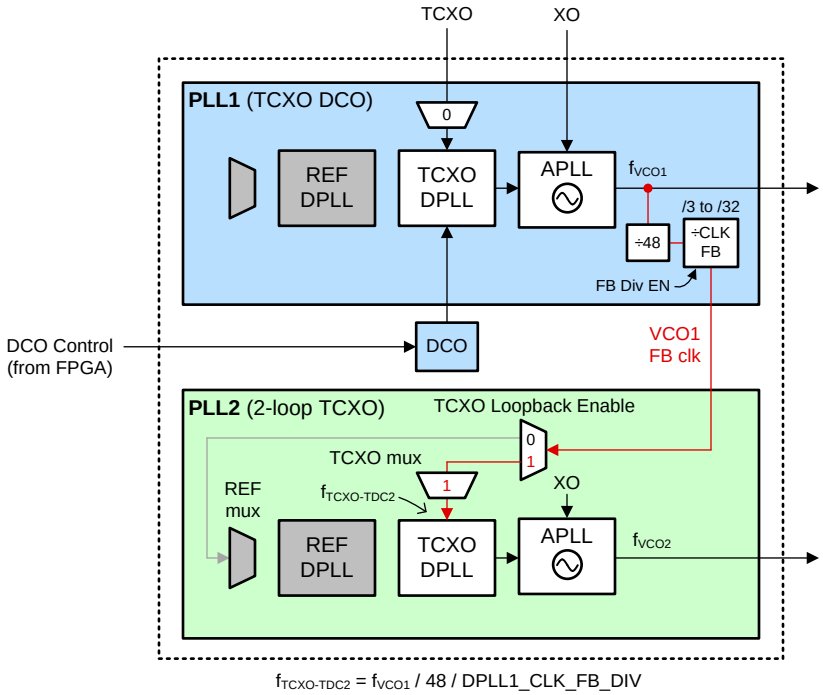


Figure 54. PLL Cascading Example With DCO Frequency Steering

9.4 Device Functional Modes

9.4.1 Device Start-Up Modes

The LMK05028 can start up in one of three device modes depending on the 3-level input level sampled on the HW_SW_CTRL pin during power-on reset (POR):

- **HW_SW_CTRL = 0:** EEPROM + I^{2}C Mode (Soft pin mode)
- **HW_SW_CTRL = V_{IM} / Float:** EEPROM + SPI Mode (Soft pin mode)
- **HW_SW_CTRL = 1:** ROM + I^{2}C Mode (Hard pin mode)

Device Functional Modes (continued)

The device start-up mode determines:

- The memory bank (EEPROM or ROM) used to initialize the register settings that sets the frequency configuration.
- The serial interface (I^2C or SPI) used for register access.
- The logic pin functionality for device control and status.

After start-up, the I^2C or SPI interface is enabled for register access to monitor the device status and control (or reconfigure) the device if needed. The register map configurations are the same for I^2C and SPI.

Table 1 summarizes the device start-up mode and corresponding logic pin functionality.

Figure 55 shows the device power-on reset configuration sequence.

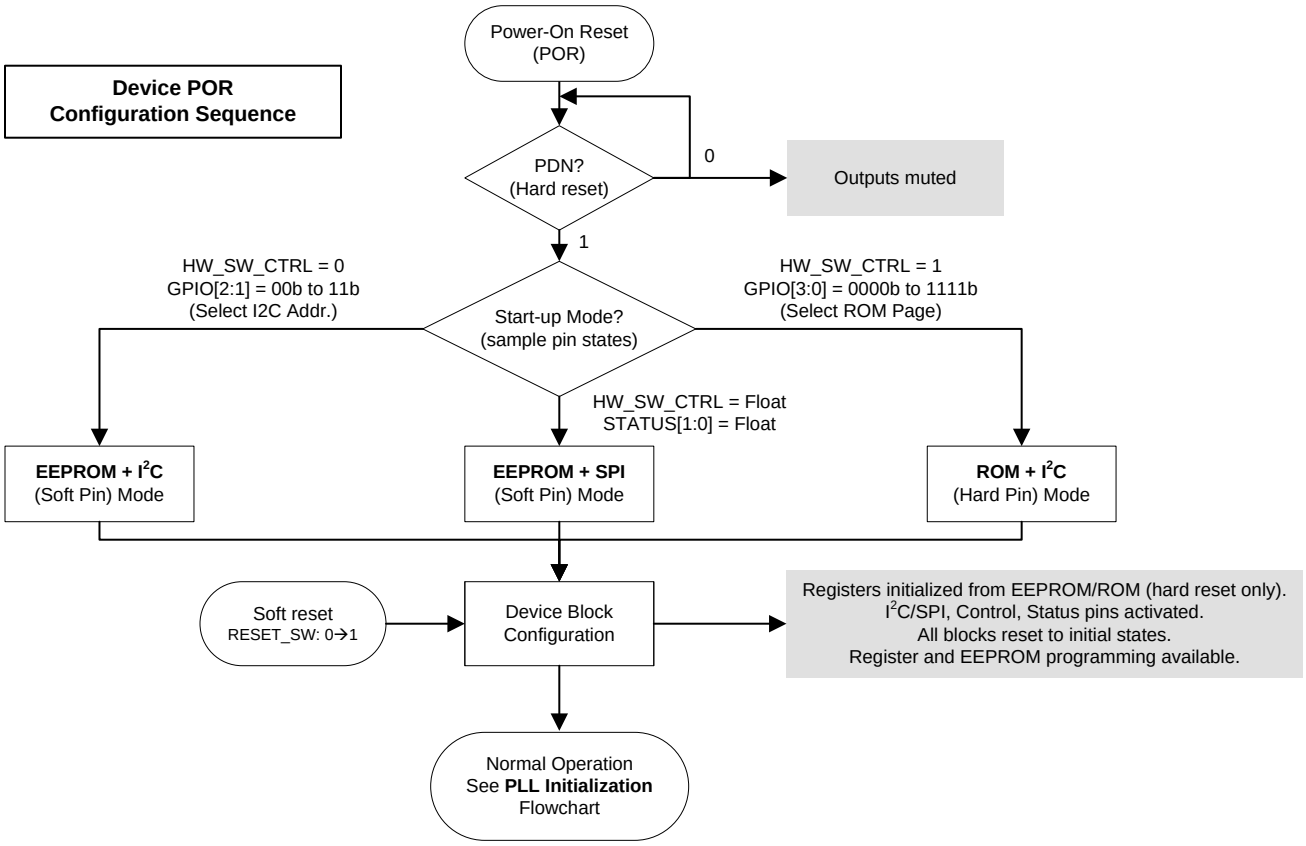


Figure 55. Device POR Configuration Sequence

9.4.1.1 EEPROM Mode

In EEPROM mode, the device's frequency configuration is loaded to the registers from the non-volatile EEPROM. A single user-defined register page can be programmed to the EEPROM to generate a custom frequency configuration on start-up. The EEPROM image can be pre-programmed at factory test or programmed in-system through the serial interface. The EEPROM supports up to 100 programming cycles to facilitate clock reconfiguration for system-level prototyping, debug, and optimization.

The EEPROM image can store a single register page or frequency configuration. A factory pre-programmed device with custom EEPROM image would be assigned by TI with a unique orderable part number (OPN).

Device Functional Modes (continued)

TI suggests using EEPROM mode when any of the following is required:

- A single custom start-up frequency configuration is needed from a single OPN.
- A host device is available to program the registers and EEPROM (if desired) with a new configuration after power-up through I^2C or SPI.
- SPI protocol is required for register access because SPI is not supported in ROM mode.

9.4.1.2 ROM Mode

In ROM mode, the device's frequency configuration is loaded to the registers from one of 16 register pages in ROM selected by the GPIO[3:0] control pins. All register pages in the ROM image are factory-set in hardware (mask ROM) and not software programmable. Only the I^2C interface is available after start-up in ROM mode.

A benefit of ROM over EEPROM is a custom ROM image can support up to 16 different pin-selectable frequency configurations from a single OPN. A factory preset device with custom ROM image would be assigned by TI with a unique OPN.

9.4.2 PLL Operating Modes

Both PLL channels have identical functionality and modes of operation, but each are configured and operate independently. The operating mode for both channels can be different at any time. The following sections describe the PLL modes of operation shown in Figure 56.

Device Functional Modes (continued)

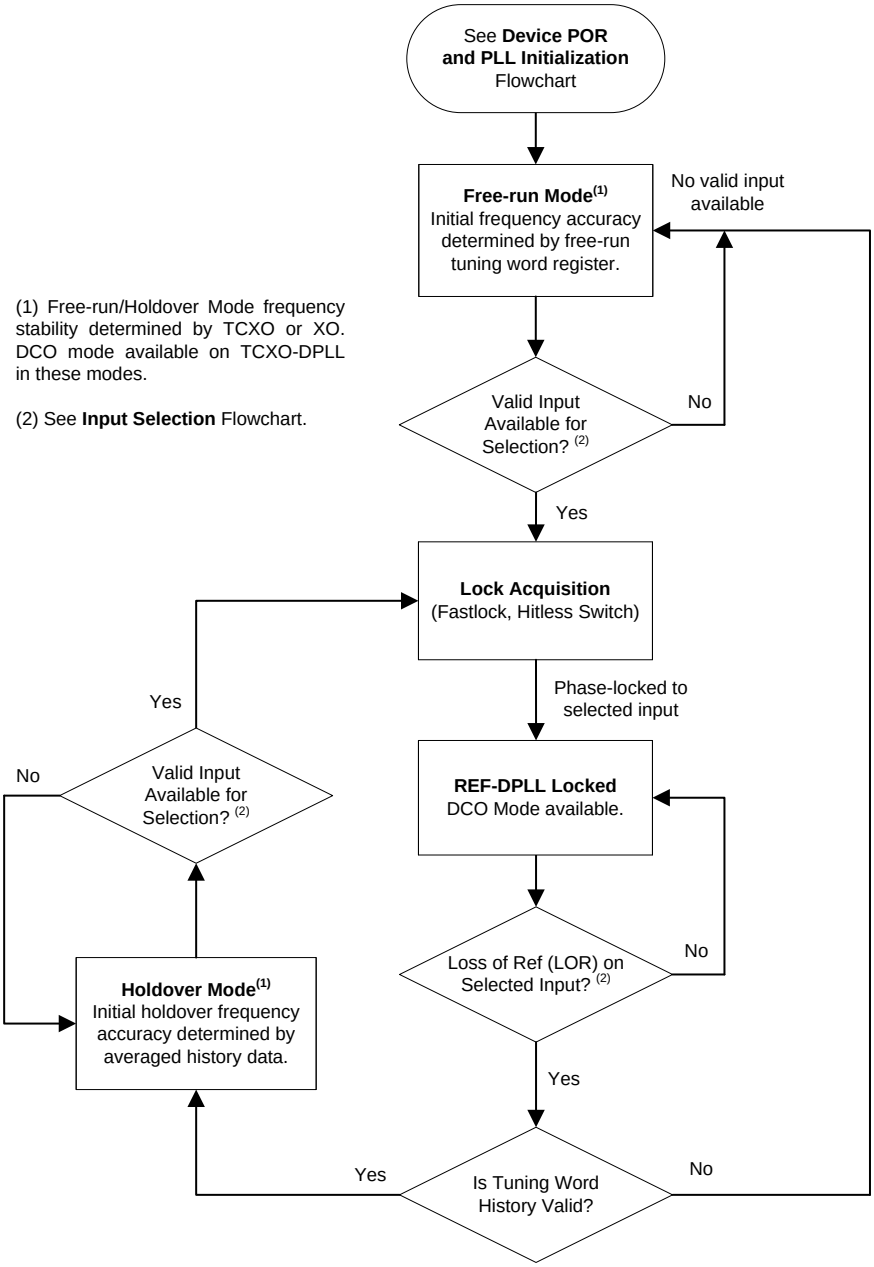


Figure 56. PLL Operating Mode

Device Functional Modes (continued)

9.4.2.1 Free-Run Mode

After device POR configuration and initialization, the APLL will automatically lock to the XO clock once it is detected by its input monitor. The output clock frequency accuracy and stability in free-run mode are equal to that of the XO input. If the TCXO input is used, the TCXO-DPLL will lock to the TCXO/OCXO clock once it is detected by its input monitor, and the output clock frequency accuracy and stability in free-run mode are equal to that of the TCXO/OCXO input. The reference inputs remain invalid (unqualified) during free-run mode.

9.4.2.2 Lock Acquisition

The PLL channel constantly monitors its assigned reference inputs for a valid input clock. When at least one valid input clock is detected, the PLL will exit free-run mode or holdover mode and initiate lock acquisition through the REF-DPLL. The device supports the Fastlock feature where the REF-DPLL temporarily engages a wider loop bandwidth to reduce the lock time. Once lock acquisition is done, the loop bandwidth is set to its normal configured loop bandwidth setting ($BW_{REF\text{-}DPLL}$).

9.4.2.3 Locked Mode

Once locked, the PLL output clocks will be frequency and phase locked to its selected DPLL input clock. While the DPLL is locked, the output clocks will not be affected by frequency drift on the XO or TCXO inputs. The REF-DPLL has a programmable frequency lock detector and phase lock detectors to indicate loss of frequency lock (LOFL) and loss of phase lock (LOPL) status flags, which can be observed through the status pins or status bits. Once frequency lock is detected (LOFL → 0), the tuning word history monitor (if enabled) will begin to accumulate history data that is used to determine the initial output frequency accuracy upon entry into holdover mode.

9.4.2.4 Holdover Mode

When a loss of reference (LOR) condition is detected and no valid input is available, the PLL will enter holdover mode. If the tuning word history is valid, the initial output frequency accuracy upon entry into holdover will be pulled to the computed average frequency accuracy just prior to the loss of reference. If no history exists, the holdover frequency accuracy will be determined by the free-run tuning word register (user programmable). The initial holdover frequency accuracy depends on the DPLL loop bandwidth and the elapsed time used for historical averaging. In general, the longer the historical average time, the more accurate the initial holdover frequency assuming the 0-ppm reference clock is drift-free. The stability of the 0-ppm reference clock (either XO or TCXO input) determines the long-term stability and accuracy of the holdover output frequency. Upon entry into holdover, the LOPL flag will be asserted (LOPL → 1); however, the LOFL flag will not be asserted as long as the holdover frequency accuracy does not drift beyond of the programmed loss-of-frequency-lock threshold. When a valid input becomes available for selection, the PLL will exit holdover mode and automatically phase lock with the new input clock without any output glitches.

Device Functional Modes (continued)

9.4.3 PLL Start-Up Sequence

Figure 57 shows the general sequence for PLL start-up after device configuration. This sequence is also applicable after a device soft-reset or individual PLL soft-reset. To ensure proper VCO calibration, it is critical for the external XO clock to be stable in amplitude and frequency prior to the start of VCO calibration; otherwise, the VCO calibration can fail and prevent start-up of the PLL and its output clocks.

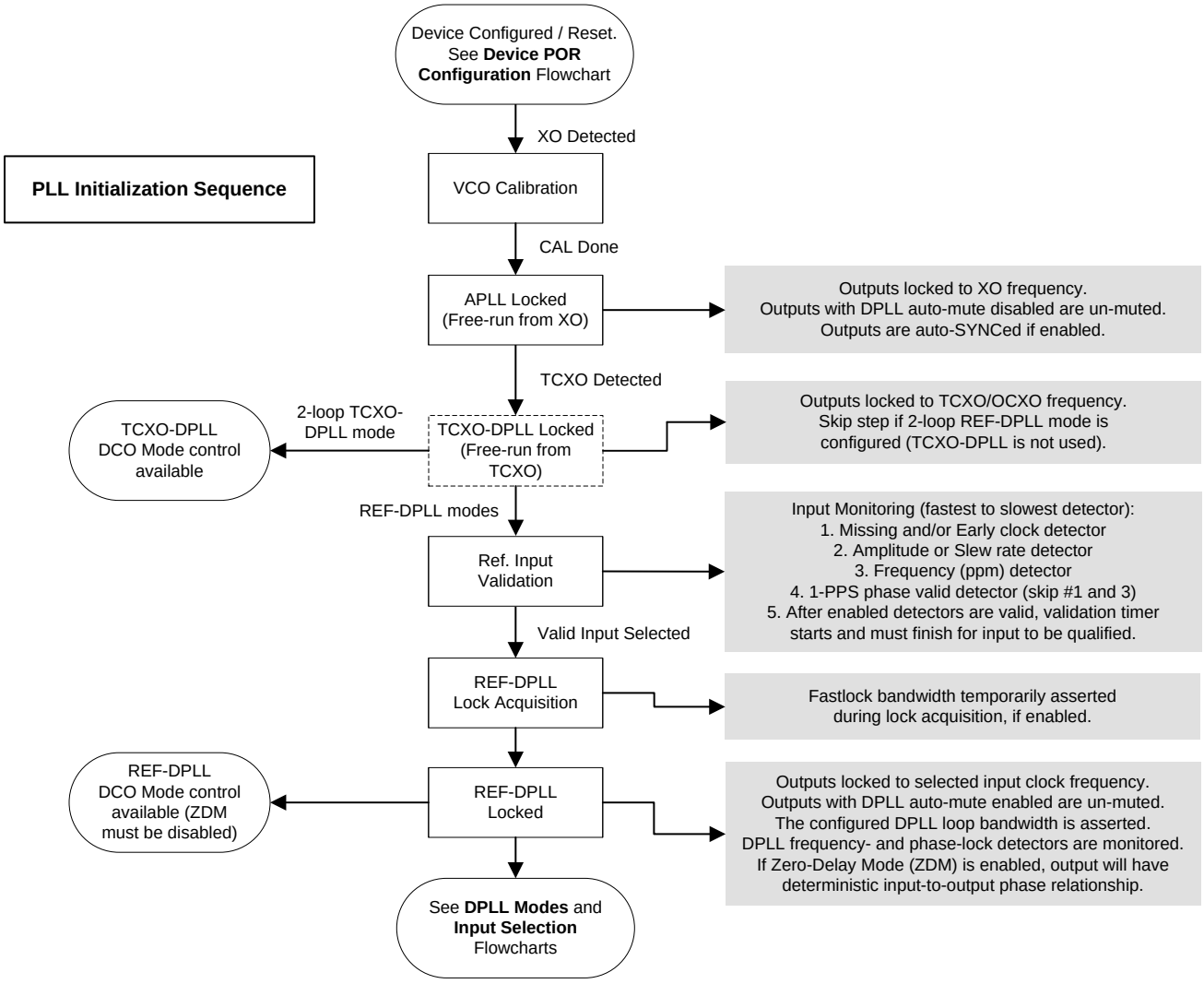


Figure 57. PLL Start-Up Sequence

Device Functional Modes (continued)

9.4.4 Digitally-Controlled Oscillator (DCO) Mode

To support IEEE 1588 slave clock and other clock steering applications, each PLL channel supports DCO mode to allow precise output clock frequency adjustment of less than 1 ppt/step. DCO mode can be enabled on either REF-DPLL or TCXO-DPLL loop when operating in locked mode.

The DCO frequency step size can be programmed through the frequency deviation or FDEV register (DPLLy_FDEV bits). The FDEV step value is an offset added to or subtracted from the current numerator value of the DPLL's fractional FB divider SDM that determines the DCO frequency offset at the VCO output.

The DCO frequency increment (FINC) or frequency decrement (FDEC) updates can be controlled through software control or pin control. DCO updates through software control are always available through I^2C or SPI by writing to the DPLLy_FDEV_REG_UPDATE register bit. Writing a 0 will increment the DCO frequency by the programmed step size, while writing a 1 will decrement it.

The pin control paths to each DCO block must be enabled through registers. Once enabled, a positive pulse on the GPIO3/FINC1 or GPIO4/FDEC1 pin will apply a corresponding DCO update to DPLL1. Similarly, a positive pulse on the GPIO5/FINC2 or GPIO6/FDEC2 pin will apply a corresponding DCO update to DPLL2. The minimum positive pulse width applied to the FINC or FDEC pins should be greater than 100 ns to be captured by the internal sampling clock. The DCO update rate should limited to less than 1 MHz when using pin control.

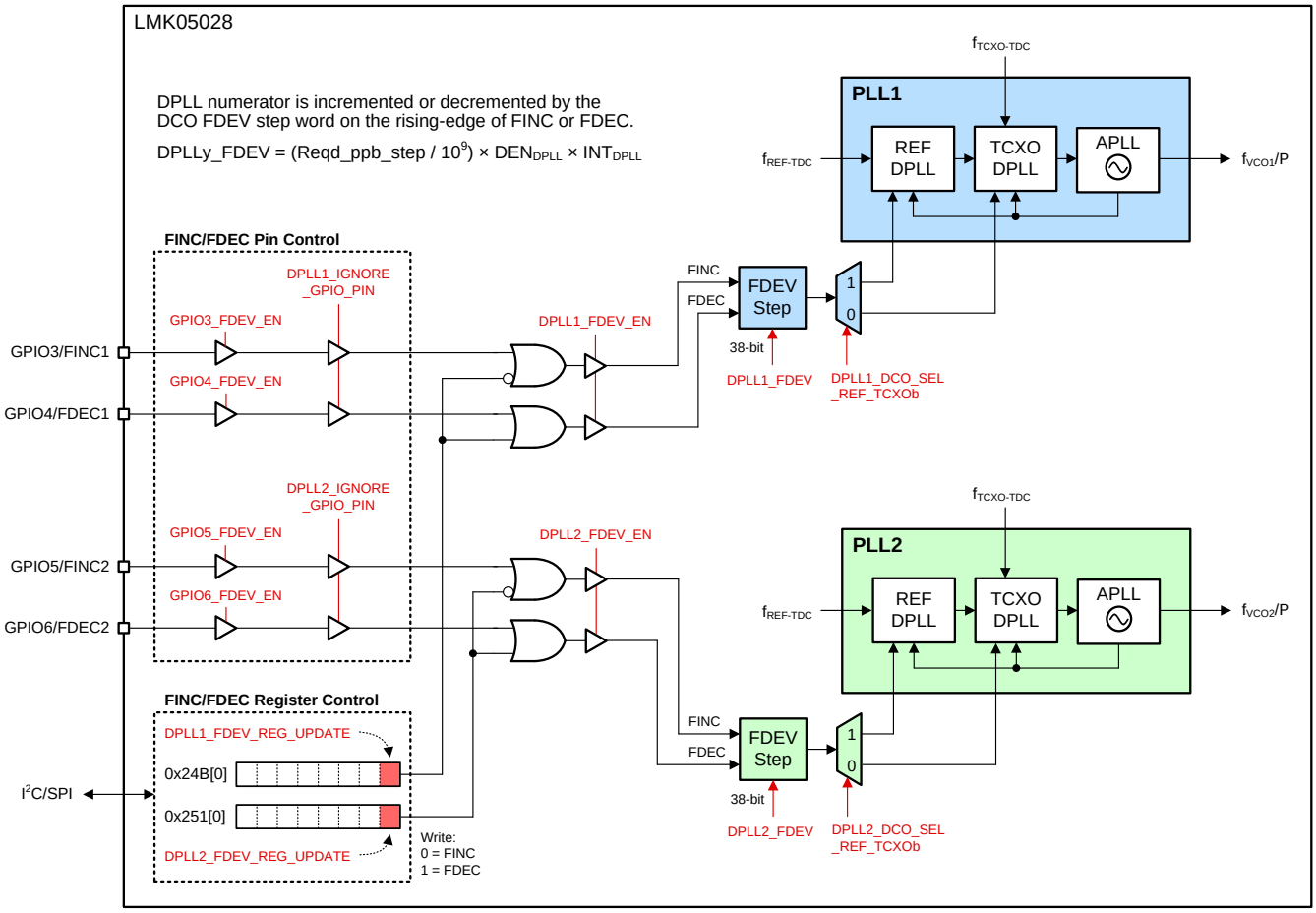


Figure 58. DCO Mode Control Options

Device Functional Modes (continued)

9.4.4.1 DCO Frequency Step Size

Equation 16 shows the formula to compute the DPLLy_FDEV register value required to meet the specified DCO frequency step size in ppb (part-per-billion) when DCO mode is enabled for the REF-DPLL (when DPLLy_DCO_SEL_REF_TCXOB = 1).

$$DPLLy\_FDEV = (Reqd\_ppb / 10^9) \times DEN_{REF} / (f_{INx} / R_{INx}) \times f_{VCOy} / (P1_{PLLy} \times PR_{REF}) \quad (16)$$

where

- y: PLL index (1 or 2)
- DPLLy_FDEV: Frequency deviation value (0 to 2^{38}–1)
- Reqd_ppb: Required DCO frequency step size (in ppb)
- DEN_{REF}: REF-DPLLy feedback divider denominator value (1 to 2^{40})
- f_{INx}: Reference input frequency (x = 0, 1, 2, 3)
- R_{INx}: Reference input divide value (1 to 2^{16}–1) (x = 0, 1, 2, 3)
- f_{VCOy}: VCOy frequency
- $P1_{PLLy}$ = PLLy primary post-divide value (4 to 9, 11, 13)
- PR_{REF}: REF-DPLLy feedback prescaler divide value (2 to 17)

Equation 17 shows the formula to compute the DPLLy_FDEV register value required to meet the specified DCO frequency step size (in ppb) when DCO mode is enabled for the TCXO-DPLL (when DPLLy_DCO_SEL_REF_TCXOB = 0).

$$DPLLy\_FDEV = (Reqd\_ppb / 10^9) \times DEN_{TCXO} / (f_{TCXO} \times D / M) \times f_{VCOy} / (P1_{PLLy} \times PR_{TCXO}) \quad (17)$$

where

- DEN_{TCXO}: TCXO-DPLLy feedback divider denominator value (fixed, 2^{40})
- f_{TCXO}: TCXO/OCXO input frequency
- D_{TCXO}: TCXO/OCXO input doubler (1 = disabled, 2 = enabled)
- M_{TCXO}: TCXO/OCXO input divide value (1 to 32)
- PR_{TCXO}: TCXO-DPLLy feedback prescaler divide value (2 to 17)

9.4.4.2 DCO Direct-Write Mode

An alternate method to update the DCO frequency is to take the current numerator value of the DPLL's fractional feedback divider, compute the adjusted numerator value by adding or subtracting the DPLLy_FDEV step value computed above, and to write the adjusted numerator value through I^2C or SPI.

Device Functional Modes (continued)

9.4.5 Zero-Delay Mode (ZDM)

Each PLL channel supports the zero-delay mode option to achieve a known and deterministic phase relationship between the reference and output clock. ZDM is supported for 2-loop and 3-loop modes through the REF-DPLL. Once PLL is locked with ZDM enabled, the PLL will have minimal phase delay (phase offset) between its reference input and the output clocks. The input-to-output phase offset (t_{PHO}) will be repeatable after exiting holdover, after a switchover event, and after device start-up. Note that ZDM and DCO mode should not be enabled at the same time within a PLL channel.

As shown in Figure 59, PLL1 supports zero-delay for OUT4/5, OUT6, and OUT7. PLL2 supports zero-delay for OUT0, OUT1, and OUT2/3 through as similar ZDM configuration. See *Zero-Delay Mode (ZDM) Configuration*.

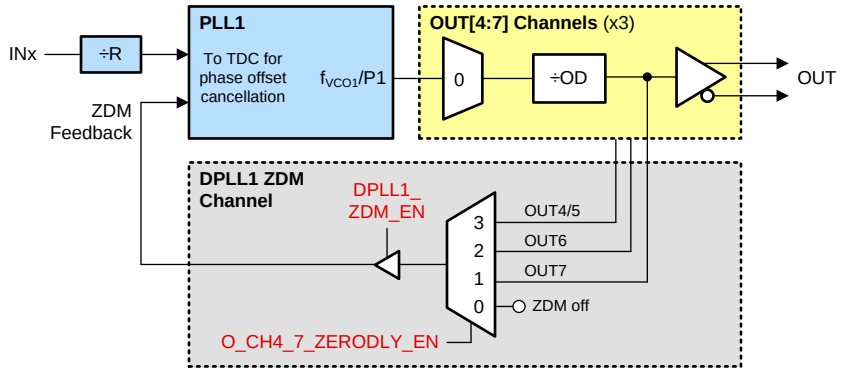


Figure 59. DPLL1 ZDM Configuration for OUT4 to OUT7

9.4.6 Cascaded PLL Operation

Each PLL channel has a VCO loopback clock (VCOx FB) routed internally to the input paths of the opposite DPLLs to support PLL cascading, where the VCO loopback clock from the first PLL stage (either PLL1 or PLL2) is used as an input reference to the second PLL stage. PLL cascading allows the second PLL must be precisely locked to the frequency of the first PLL. The internal VCO loopback configuration options are implemented identically on both PLL channels, allowing PLL2 to be cascaded after PLL1 or vice versa. The loopback configuration options include programmable VCO clock dividers, clock muxes to loop-back to either REF-DPLL or TCXO-DPLL inputs, and loopback clock validation to control the PLL lock sequence for the second PLL stage. The internal VCO loopback option eliminates the need for external clock loopback, which would otherwise require the designer to dedicate an output buffer, an input buffer, and external routing to support cascaded PLL operation. See *PLL Cascading With Internal VCO Loopback*.

9.5 Programming

9.5.1 Interface and Control

A system host device (MCU or FPGA) can use either I^2C or SPI to access the register, SRAM, and EEPROM maps. The register and EEPROM map configurations are the same for I^2C and SPI. The device can be initialized, controlled, and monitored through register access during normal operation (not hard reset by PDN = 0). Some device features can also be controlled and monitored through the external logic control and status pins.

In the absence of a host, the LMK05028 can self-start from its on-chip EEPROM or ROM page depending on the state of HW_SW_CTRL pin. The EEPROM or ROM page is used to initialize the registers upon device POR. The EEPROM configuration can be custom programmed through the register interface by either I^2C or SPI. The ROM configurations are fixed in hardware and cannot be modified.

Figure 60 shows the device control pin, register, and memory interfaces. The arrows refer to the control interface directions between the different blocks.

The register map has 800 data bytes. Some registers (such as status, internal test/diagnostic bit fields) do not need to be written or accessed during device initialization.

The SRAM/EEPROM has one register page with 509 data bytes. The SRAM/EEPROM map has fewer bytes because not all bit fields are mapped from the register space. To program the EEPROM, it is necessary to write the register contents to SRAM (internal register commit or direct write), then Program EEPROM with the register contents from SRAM. The EEPROM cannot be written directly from the registers.

The ROM has sixteen register pages, and each page has 509 data bytes (same as EEPROM). The ROM contents are fixed in hardware and cannot be modified.

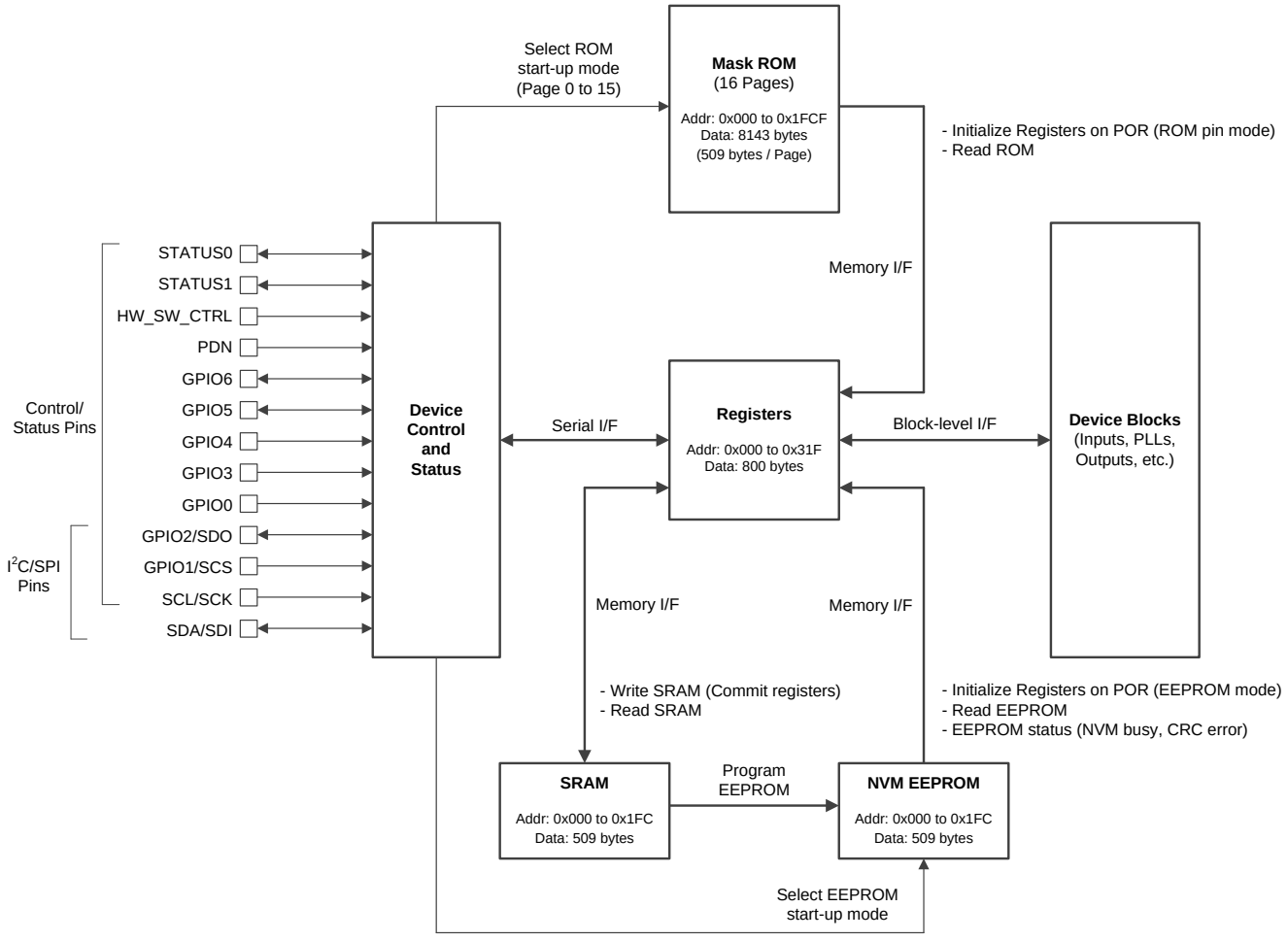


Figure 60. Device Control, Register, and Memory Interfaces

Programming (continued)

9.5.2 I²C Serial Interface

When started in I²C mode (HW_SW_CTRL = 0 or 1), the LMK05028 operates as an I²C slave and supports bus rates of 100 kHz (standard mode) and 400 kHz (fast mode). Slower bus rates can work as long as the other I²C specifications are met.

In EEPROM mode, the LMK05028 can support up to four different I²C addresses depending on the GPIO[2:1] pins. The 7-bit I²C address is 11000xxb, where the two LSBs are determined by the GPIO[2:1] input levels sampled at device POR and the five MSBs (11000b) are initialized from EEPROM. In ROM mode, the two LSBs are fixed to 00b and the five MSB (11000b) are initialized from ROM.

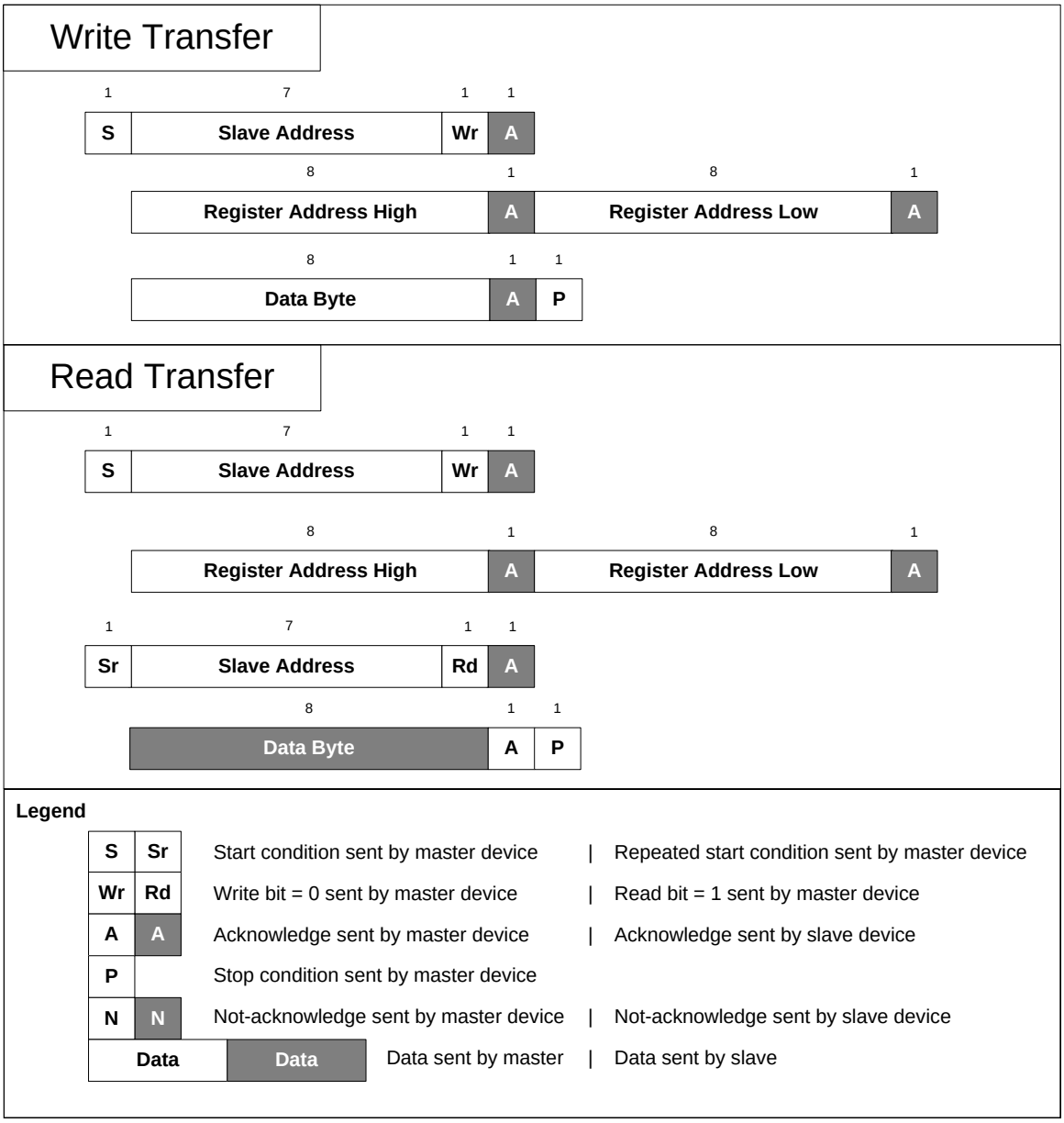


Figure 61. I²C Byte Write and Read Transfers

Programming (continued)

9.5.2.1 I²C Block Register Transfers

The device supports I²C block write and block read register transfers as shown in Figure 62

Figure 62. I²C Block Register Transfers

9.5.3 SPI Serial Interface

When started in SPI mode (HW_SW_CTRL = float), the device uses a 4-wire SPI interface with SDI, SCK, SDO, and SCS signals. The host device must present data to the device MSB first. A message includes a transfer direction bit ($\overline{W}$/R), a 15-bit address field (A14 to A0), and a 8-bit data field (D7 to D0) as shown in Figure 63. The $\overline{W}$/R bit is 0 for a SPI write and 1 for a SPI read.

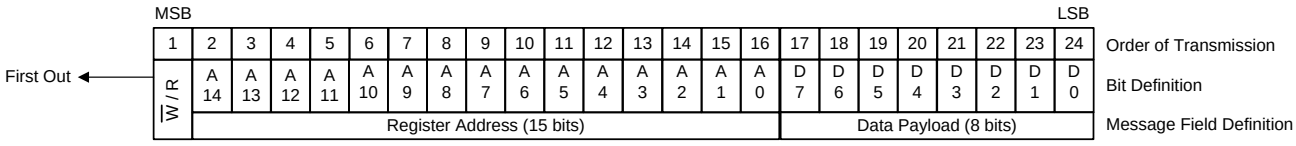


Figure 63. SPI Message Format

A message frame is initiated by asserting SCS low. The frame ends when SCS is deasserted high. The first bit transferred is the $\overline{W}$/R bit. The next 15 bits are the register address, and the remaining 8 bits are data. On write transfers, data is committed in bytes as the final data bit (D0) is clocked in on the rising edge of SCK. If the write access is not an even multiple of 8 clocks, the trailing data bits are not committed. On read transfers, data bits are clocked out from the SDO pin on the falling edges of SCK.

Programming (continued)

9.5.3.1 SPI Block Register Transfer

The device supports a SPI block write and block read transfers. A SPI block transfer is exactly (2 + N) bytes long, where N is the number of data bytes to write or read. The host device (SPI master) is only required to specify the lowest address of the sequence of addresses to be accessed. The device will automatically increment the internal register address pointer if the SCS pin remains low after the host finishes the initial 24-bit transmission sequence. Each transfer of 8 bits (a data payload width) results in the device automatically incrementing the address pointer (provided the SCS pin remains active low for all sequences).

9.5.4 Register Map Generation

The TICS Pro software tool for EVM programming has a step-by-step design flow to enter the user's clock design parameters, calculate the frequency plan, and generate the device register settings for the desired configuration. The register settings can be exported (in hex format) to enable host programming of the LMK05028 on start-up. The TICS Pro setup file can also be provided to TI for device configuration review, optimization, and to enable factory pre-programmed sample devices.

9.5.5 General Register Programming Sequence

For applications that use a system host device to program the initial LMK05028 configuration after start-up, this general procedure can be followed from the register map data generated and exported from TICS Pro:

1. Apply power to the device to start in I^2C or SPI mode. The PDN pin should be pulled high or driven high.
2. Write 9Ah to R12 to disable device auto-start and mute the outputs during programming.
3. Write 1Ah to R12 to exit soft-reset (this does not reset register values).
4. Write the register settings from lower to higher addresses (R0 to R647) while applying the following register mask (Do not modify mask bits = 1):
   - Mask R12 = A5h
   - Mask R167 = FFh
   - Mask R174 = FFh
5. Write 1b to R12[7] to assert soft-reset. This does not reset register values.
6. Write 1b to R12[7]) to begin normal device operation (starting with VCO calibration and PLL start-up).
7. See *EEPROM Programming Using Register Commit (Method #1)* to store the active configuration to the EEPROM to enable self-startup on the next power cycle.

9.5.6 EEPROM Programming Flow

Before the EEPROM can be programmed, it is necessary to program the desired configuration to the SRAM through the memory control registers. The register data can be written to SRAM by committing the active register configuration internally (Method #1), or by using direct writes to SRAM (Method #2). Method #1 requires the active registers be first programmed to the desired configuration, but does not require knowledge of the SRAM/EEPROM map. Method #2 bypasses any writes to the active registers configuration, allowing the device to continue normal operation without disruption while the SRAM/EEPROM are programmed. The EEPROM programming flow for the two methods are different and described as follows.

9.5.6.1 EEPROM Programming Using Register Commit (Method #1)

This sequence can be followed to program EEPROM from the active registers. This requires the register data in the register map format:

1. Program the desired configuration to the active registers (see *General Register Programming Sequence*).
2. *Write SRAM Using Register Commit*.
3. *Program EEPROM*.

9.5.6.1.1 Write SRAM Using Register Commit

The SRAM array is volatile shadow memory mapped to a subset of the active configuration registers that determine the device's frequency configuration at start-up.

Programming (continued)

After the active registers have been programmed, they can be internally committed to the SRAM through the following sequence:

1. Write 0h to R175 (REGCOMMIT_PG byte).
2. Write 40h to R167 (REGCOMMIT bit, self-clearing). This commits the current register data to the SRAM internally.

9.5.6.1.2 Program EEPROM

The EEPROM array is non-volatile memory mapped directly from the SRAM array.

After the register settings have been written to SRAM (by either Method #1 or #2), the EEPROM can be programmed through the following sequence:

1. Write EAh to R174 (NVMUNLK). This unlocks the EEPROM to allow programming.
2. Write 03h to R167 (NVM_ERASE_PROG bits). This programs the EEPROM from the entire SRAM contents. The total erase/program cycle takes about 230 ms.
   - **NOTE**: Steps 1 and 2 must be atomic writes without any other register transactions in-between.
3. (optional) Read or poll R167[2] (NVMBUSY bit). When this bit cleared, the EEPROM programming is done.
4. (optional) Write 00h to R174. This locks the EEPROM to protect against inadvertent programming.

On the next power-up or hard reset, the device can self-start in EEPROM mode from the newly programmed configuration. Also, the NVMCNT register value will be incremented by 1 after power-up or hard reset to reflect total number of EEPROM programming cycles completed.

9.5.6.2 EEPROM Programming Using Direct SRAM Writes (Method #2)

This sequence can be followed to program EEPROM by writing SRAM directly to avoid disruption to the current device configuration. This requires the register data in the SRAM/EEPROM map format.

1. *Write SRAM Using Direct Writes*.
2. *Program EEPROM*.

9.5.6.2.1 Write SRAM Using Direct Writes

This SRAM write method can be used if it is required to store a different device configuration to EEPROM without disrupting the current operational state of the device. This method requires the SRAM/EEPROM map data to be already generated, which can be done by the TICS Pro software. The SRAM can be directly written *without modifying the active configuration registers* through the following sequence:

1. Write the most significant 5 bits of the SRAM address to R169 (MEMADR byte 1) and write the least significant 8 bits of the SRAM address to R170 (MEMADR byte 0).
2. Write the SRAM data byte to R172 (RAMDAT byte) for the SRAM address specified in the previous step in the same register transaction.
   - Any additional write transfers in same transaction will cause the SRAM address pointer to be auto-incremented and a subsequent write will take place at the next SRAM address.
   - Byte or Block write transfers to R172 can be used to write the entire SRAM map sequentially from Byte 0 to 508 (509 bytes total).
   - Alternatively, it is valid to write R169 and R170 before each write to R172 to set the memory address explicitly (that is, bypass the memory pointer auto-increment).
   - Access to the SRAM will terminate at the end of current write transaction. Note that reading the RAMDAT register will also auto-increment the memory address pointer.

9.5.7 Read SRAM

The contents of the SRAM can be read back, one word at a time, starting with that of the requested address through the following sequence. This sequence can be used to verify the contents written to SRAM before an EEPROM program cycle.

1. Write the most significant 5 bits of the SRAM address to R169 (MEMADR byte 1) and write the least significant 8 bits of the SRAM address to R170 (MEMADR byte 0).

Programming (continued)

2. The SRAM data located at the address specified in the step above can be obtained by reading R172 (RAMDAT byte) in the same register transaction.
   – Any additional read transfers that is part of the same transaction will cause the SRAM address to be auto-incremented and a subsequent read will take place at the next SRAM address.
   – Byte or Block read transfers from R172 can be used to read the entire SRAM map sequentially from Byte 0 to 508 (509 bytes total).
   – Access to SRAM will terminate at the end of current register transaction.

9.5.8 Read EEPROM

The contents of the EEPROM can be read back, one word at a time, starting with that of the requested address through the following sequence. This sequence can be used to verify the contents written to EEPROM after an EEPROM program cycle.

1. Write the most significant 5 bit of the EEPROM address in R169 (MEMADR byte 1) and write the least significant 8 bits of the EEPROM address in R170 (MEMADR byte 0).
2. The EEPROM data located at the address specified in the step above can be obtained by reading R171 (NVMDAT byte) in the same register transaction.
   – Any additional access that is part of the same transaction will cause the EEPROM address to be incremented and a read will take place of the next EEPROM address.
   – Byte or Block read transfers from R171 can be used to read the entire EEPROM map sequentially from Byte 0 to 508 (509 bytes total).
   – Access to EEPROM will terminate at the end of current register transaction.

Programming (continued)

9.5.9 EEPROM Start-Up Mode Default Configuration

The device is factory pre-programmed with the following EEPROM default configuration.

Table 11. LMK05028 Default Configuration

SYSTEM CLOCKS	FREQUENCY (Hz)	INPUT TYPE	0-PPM REF CLK
XO	48,000,000	DC-DIFF(ext. term)	XO
TCXO	-		
CLOCK INPUTS	FREQUENCY (Hz)	DPLL REF MUX	INPUT TYPE
IN0	156,250,000	DPLL 1,2	AC-DIFF(ext. term)
IN1	156,250,000	DPLL 1,2	AC-DIFF(ext. term)
IN2	27,000,000	DPLL 1,2	AC-DIFF(ext. term)
IN3	10,000,000	DPLL 1,2	AC-DIFF(ext. term)
DPLL1 INPUT SELECT MODE	MANUAL REGISTER SELECTION	DPLL1 INPUT	AUTO PRIORITY
Auto Revertive	IN0	IN0	1st
		IN1	2nd
		IN2	3rd
		IN3	4th
DPLL2 INPUT SELECT MODE	MANUAL REGISTER SELECTION	DPLL2 INPUT	AUTO PRIORITY
Auto Revertive	IN0	IN0	1st
		IN1	2nd
		IN2	3rd
		IN3	4th
CLOCK OUTPUTS	FREQUENCY (Hz)	OUTPUT MUX	OUTPUT TYPE
OUT0	322,265,625.0	PLL 1	AC-LVDS
OUT1	122,880,000.0	PLL 2	AC-LVDS
OUT2	122,880,000.0	PLL 2	AC-LVDS
OUT3	122,880,000.0	PLL 2	AC-LVPECL
OUT4	122,880,000.0	PLL 2	AC-LVPECL
OUT5	122,880,000.0	PLL 2	AC-LVDS
OUT6	122,880,000.0	PLL 2	AC-LVDS
OUT7	322,265,625.0	PLL 1	AC-LVDS
PLL CONFIGURATION	PLL MODE	REF-DPLL BW (Hz)	TCXO-DPLL BW (Hz)
PLL1	2-loop (REF-DPLL)	100	-
PLL2	2-loop (REF-DPLL)	100	-
REF INPUT MONITORS (1)	VALIDATION TIMER (s)	FREQ DET VALID (ppm)	FREQ DET INVALID (ppm)
IN0	0.1	-	-
IN1	0.1	-	-
IN2	0.1	-	-
IN3	0.1	-	-
REF INPUT MONITORS (2)	LATE DETECT WINDOW (µs)	EARLY DETECT WINDOW (µs)	1-PPS JITTER THRESHOLD (µs)
IN0	-	-	-
IN1	-	-	-
IN2	-	-	-
IN3	-	-	-

Programming (continued)

Table 11. LMK05028 Default Configuration (continued)

DPLL LOCK DETECT	FREQ LOCK (ppm)	FREQ UNLOCK (ppm)	
DPLL1	1	3	
DPLL2	1	3	
DCO MODE	DCO MODE SELECT	DCO STEP SIZE (ppb)	
DPLL1	DCO Disabled	-	
DPLL2	DCO Disabled	-	
ZERO DELAY MODE	ZDM FEEDBACK CLOCK		
DPLL1	Disabled		
DPLL2	Disabled		

9.6 Register Maps

See the *LMK05028 Programming Guide* (SNAU233) for the register map with register descriptions.

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

10.1.1 Device Start-Up Sequence

The device start-up sequence is shown in Figure 64. If an output channel's VDDO_x is delayed after the device POR, the output channel is held in reset and its output is muted. Once VDDO_x is ramped above its threshold of about 1.5 V, the output channel is held in reset until its programmable timeout counter expires before the output driver is unmuted and clock starts up without any glitches.

Application Information (continued)

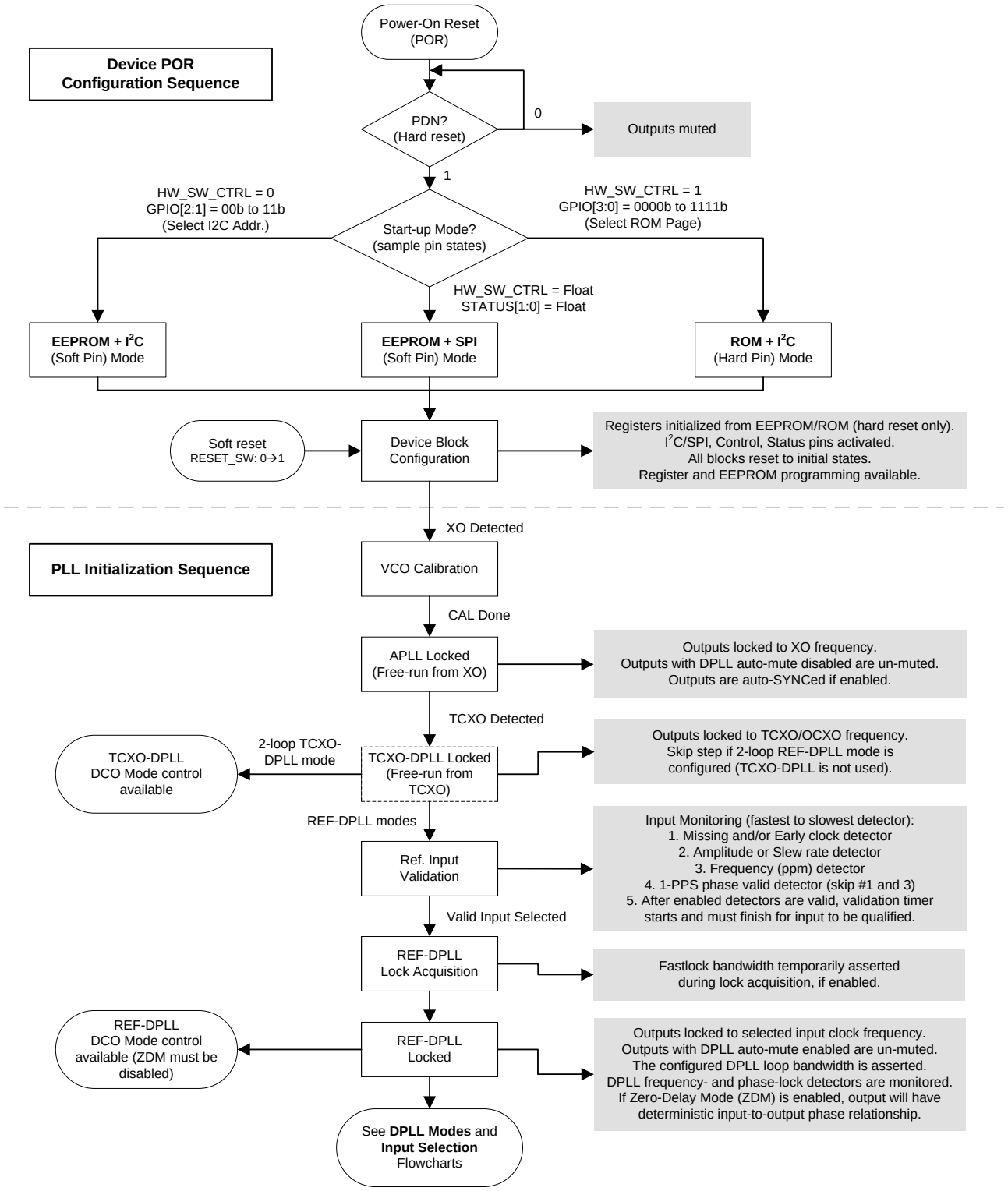


Figure 64. Device Start-Up Sequence

Application Information (continued)

10.1.2 Power Down (PDN) Pin

The PDN pin (active low) can be used for device power-down and used to initialize the POR sequence. When PDN is pulled low, the entire device is powered down and the serial interface is disabled. When PDN is pulled high, the device POR sequence is triggered to begin the device start-up sequence and normal operation as depicted in Figure 64. If the PDN pin is toggled to issue a momentary hard reset, the negative pulse applied to the PDN pin should be greater than 200 ns to be captured by the internal digital system clock.

Table 12. PDN Control

PDN PIN STATE	DEVICE OPERATION
0	Device is disabled
1	Normal operation

10.1.3 Power Rail Sequencing, Power Supply Ramp Rate, and Mixing Supply Domains

10.1.3.1 Mixing Supplies

The LMK05028 incorporates flexible power supply architecture. While all VDD core supplies should be powered by the same 3.3-V rail, the individual output supplies can be powered from separate 1.8-V, 2.5-V or 3.3-V rails. This can allow all output supplies at 1.8 V to minimize power consumption. It can also allow mixed output driver levels simultaneously, for example, a 2.5-V LVCMOS clock from a 2.5-V rail and other differential clocks from a 1.8-V rail.

10.1.3.2 Power-On Reset (POR) Circuit

The LMK05028 integrates a built-in power-on reset (POR) circuit that holds the device in reset until all of the following conditions have been met:

- All VDD core supplies have ramped above 2.72 V
- PDN pin has ramped above 1.2 V (V_{IH})

10.1.3.3 Powering Up From a Single-Supply Rail

As long as all VDD core supplies are driven by the same 3.3-V supply rail that ramp in a monotonic manner from 0 V to 3.135 V, irrespective of the ramp time, then there is no requirement to add a capacitor on the PDN pin to externally delay the device power-up sequence. As shown in Figure 65, the PDN pin can be left floating or otherwise driven by a system host device to meet the clock sequencing requirements in the system.

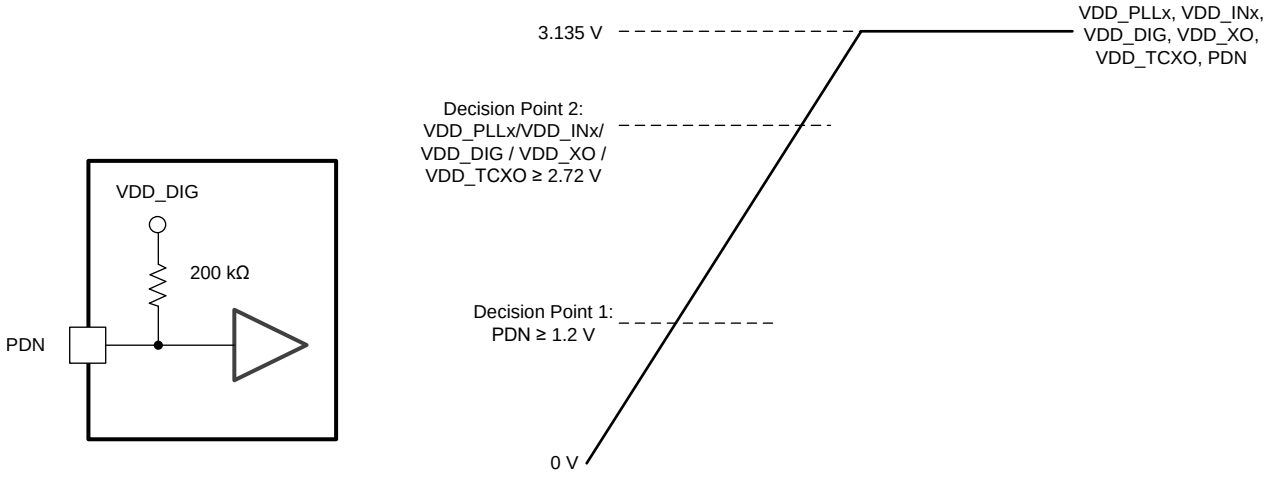


Figure 65. Recommendation for Power Up From a Single-Supply Rail

10.1.3.4 Power Up From Split-Supply Rails

If some VDD core supplies are driven from different supply rails, TI recommends starting the PLL calibration after all of the core supplies have settled at 3.135 V. This can be realized by delaying the PDN low-to-high transition. The PDN input incorporates a 200-kΩ resistor to VDD_DIG and as shown in Figure 66, a capacitor from the PDN pin to GND can be used to form an R-C time constant with the internal pullup resistor. This R-C time constant can be designed to delay the low-to-high transition of PDN until all the core supplies have settled at 3.135 V. Alternatively, the PDN pin can be driven high by a system host or power management device to delay the device power-up sequence until all VDD supplies have ramped.

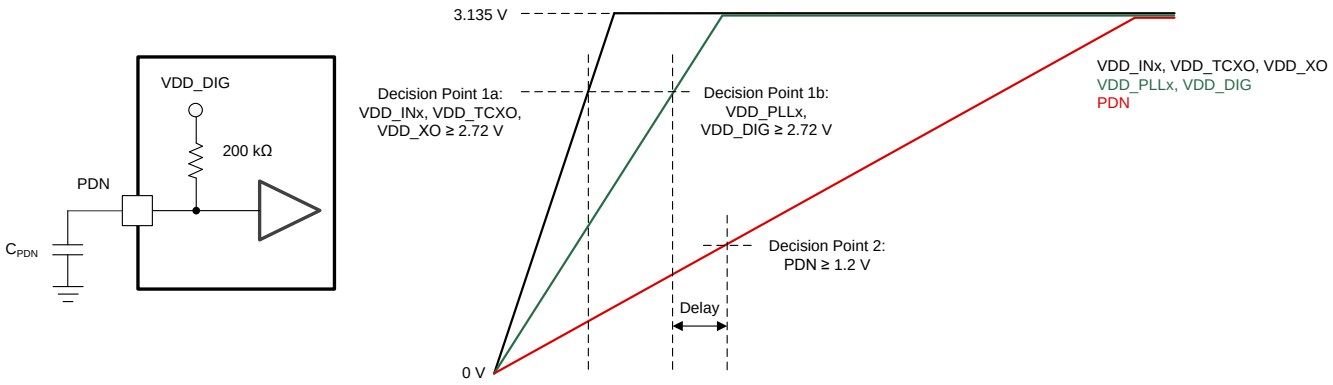


Figure 66. Recommendation for Power Up From Split-Supply Rails

10.1.3.5 Non-Monotonic or Slow Power-Up Supply Ramp

In case the VDD core supplies ramp with a non-monotonic manner or with a slow ramp time from 0 V to 3.135 V of over 100 ms, TI recommends delaying the VCO calibration until after all of the core supplies have settled at or above 3.135 V. This can be realized by delaying the PDN low-to-high transition using one of the methods described in Figure 66.

10.1.4 Slow or Delayed XO Start-Up

Because the external XO clock input is used as the reference input for the VCO calibration, the XO input amplitude and frequency must be stable before the start of VCO calibration to ensure successful PLL lock and output start-up. If the XO clock is not stable prior to VCO calibration, the VCO calibration can fail and prevent PLL lock and output clock start-up.

If the XO clock has a slow start-up time or glitches on power-up (due to a slow or non-monotonic power supply ramp, for example),TI recommends to delay the start of VCO calibration until after the XO is stable. This could be achieved by delaying the PDN low-to-high transition until after the XO clock has stabilized using one of the methods described in Figure 66. It is also possible to issue a device soft-reset after the XO clock has stabilized to manually trigger the VCO calibration and PLL start-up sequence.

10.2 Typical Application

Figure 67 shows a reference schematic to help implement the LMK05028 and its peripheral circuitry. Power filtering examples are given for the core supply pins and independent output supply pins. Single-ended LVCMOS, AC-coupled differential, and HCSL clock interfacing examples are shown for the clock input and output pins. An external LVCMOS oscillator drives an AC-coupled voltage divider network as an example to interface the 3.3-V LVCMOS output to meet the input voltage swing specified for the XO or TCXO inputs. The required external capacitors are placed close to the LMK05028 and shown with the recommended values. External pullup and pulldown resistor options at the logic I/O pins set the default input states. The I^2C or SPI pins and other logic I/O pins can be connected to a host device (not shown) to program and control the LMK05028 and monitor its status. This example assumes the device will start up from EEPROM mode with an I^2C interface (HW_SW_CTRL = 0).

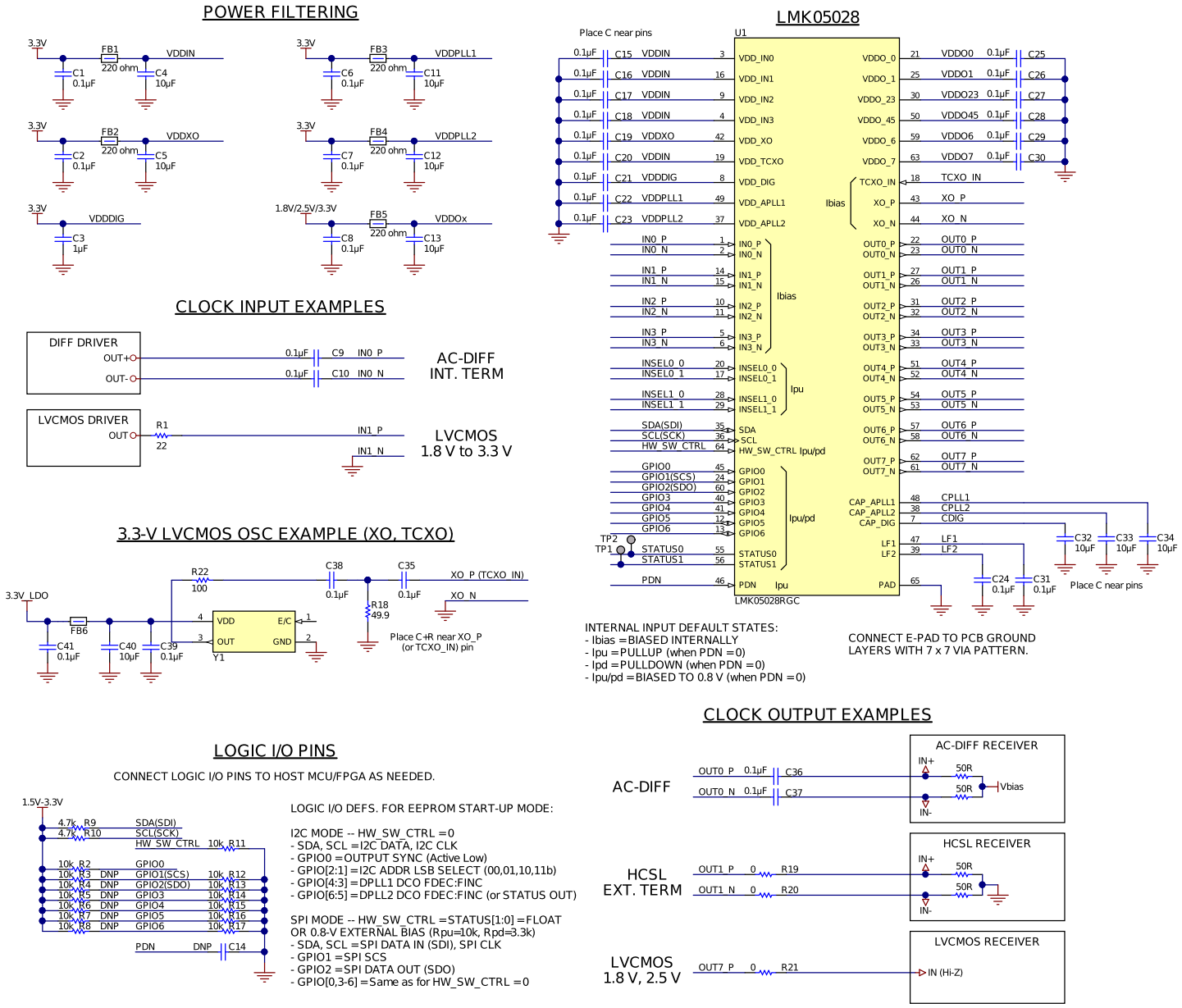


Figure 67. LMK05028 Reference Schematic Example

10.2.1 Design Requirements

In a typical application, the following design requirements or parameters should be considered to implement the overall clock solution:

1. Device initial configuration: Host programmed (MCU or FPGA) or factory pre-programmed.
2. Device start-up mode and serial interface. Typically, this will be EEPROM + I^2C or SPI mode.
3. XO frequency, signal type, and phase noise or jitter
4. TCXO frequency and stability if any of the following is required:
   - Standard-compliant frequency stability (such as SyncE, SONET/SDH, IEEE 1588)
   - Lowest possible close-in phase noise at offsets ≤ 100 Hz
   - Narrow DPLL bandwidth ≤ 10 Hz
5. For each PLL domain, determine the following:
   - Input clocks: frequency, buffer mode, priority, and input selection mode
   - Output clocks: frequency, buffer mode
   - DPLL loop mode, loop bandwidth, and market segment
   - DCO mode or Zero delay
6. Input clock and PLL monitoring options
7. Status outputs and interrupt flag
8. Power supply rails

10.2.2 Detailed Design Procedure

In a typical application, TI recommends the following steps:

1. The LMK05028 GUI in the TICS Pro programming software has a step-by-step design flow to enter the design parameters, calculate the frequency plan for each PLL domain, and generate the register settings for the desired configuration. The register settings can be exported (in hex format) to enable host programming or factory pre-programming.
   - If using a generic (non-custom) device, a host device can program the register settings through the serial interface after power-up and issue a soft-reset (by RESET_SW bit) to start the device. The host can also store the settings to the EEPROM to allow self-startup with these register settings on subsequent power-on reset cycles.
   - Alternatively, a LMK05028 setup file for TICS Pro (.tcs) can be sent to TI to request custom factory pre-programmed devices.
2. Tie the HW_SW_CTRL pin to ground to select EEPROM+I^2C mode, or bias the pin to V_{IM} through the weak internal resistors or external resistors to select EEPROM+SPI mode. Determine the logic I/O pin assignments for control and status functions. See *Device Start-Up Modes*.
   - Connect I^2C/SPI and logic I/O pins (1.8-V compatible levels) to the host device pins with the proper I/O direction and voltage levels.
3. Select a XO frequency by following *Oscillator Input (XO_P/N)*.
   - Choose a XO with target phase jitter performance < 300 fs RMS (12 kHz to 20 MHz).
   - For a 3.3-V LVCMOS driver, follow the OSC clock interface example in Figure 67. Power the OSC from a low-noise LDO regulator or optimize its supply filtering to avoid supply-induced jitter on the XO clock.
   - **TICS Pro:** Configure the XO input buffer mode to match the XO driver interface requirements. See Table 4.
4. If a TCXO/OCXO is needed, select the frequency by following *TCXO/OCXO Input (TCXO_IN)*.
   - Choose a TCXO/OCXO that meets the frequency stability and accuracy requirements required for the output clocks during free-run or holdover.
   - For a 3.3-V LVCMOS driver, follow the OSC clock interface example in Figure 67.
   - A (clipped) sinewave TCXO/OCXO with less than 1.3-Vpp swing can be simply AC-coupled to the input pin.
   - **TICS Pro:** The TCXO/OCXO input buffer is enabled when either PLL channel uses the TCXO-DPLL.

5. For each PLL domain, wire the clock I/O in the schematic and use TICS Pro to configure the device settings as follows:
   - Reference inputs: Follow the LVCMOS or differential clock input interface examples in Figure 67 or *Clock Input Interfacing and Termination*.
     - **TICS Pro:** Configure the reference input buffer modes to match the reference clock driver interface requirements. See *Table 5*.
     - LVCMOS clock input should be used for input frequencies below 5 MHz when amplitude monitoring is enabled.
   - **TICS Pro:** Configure the DPLL input selection modes and input priorities. See *Reference Input Mux Selection*.
   - **TICS Pro:** Output clock assignment guidelines to minimize crosstalk and spurs.
     - OUT[4:7] bank requires at least one clock from the PLL1 domain. OUT[4:7] bank is preferred for PLL1 clocks.
     - OUT[0:3] bank requires at least one clock from the PLL2 domain (if PLL2 is enabled). OUT[0:3] bank is preferred for PLL2 clocks.
     - Group identical output frequencies (or harmonic frequencies) on adjacent channels, and use the output pairs with a single divider (OUT2/3 or OUT4/5) when possible to minimize power.
     - Separate clock outputs when the difference of the two frequencies, $|f_{OUTx} - f_{OUTy}|$, falls within the jitter integration bandwidth (12 kHz to 20 MHz, for example). Any outputs that are potential aggressors should be separated by at least four static pins (power pin, logic pin, or disabled output pins) to minimize potential coupling. If possible, separate these clocks by the placing them on opposite output banks, which are on opposite sides of the chip for best isolation.
     - Avoid or isolate any LVCMOS output (strong aggressor) from other jitter-sensitive differential output clocks. If a LVCMOS output is required, use dual complementary LVCMOS mode (+/- or -/+) with the unused LVCMOS output left floating with no trace. Furthermore, the output slew rate could also be slowed to Normal mode (CHx_SLEW_RATE bit) to reduce the coupling strength of an LVCMOS output.
     - If not all outputs pairs are used in the application, consider connecting OUT0 and/or OUT1 to a pair of RF coaxial test structures for testing purposes (such as SMA, SMP ports). OUT0 and OUT1 are capable of selecting a buffered copy of the XO clock or the TCXO/Ref Bypass clock as well as any PLL post-divider clock.
   - **TICS Pro:** Configure output divider and drivers.
     - Configure the output driver modes to match the receiver clock input interface requirements. See Table 9.
     - Configure any output SYNC groups that need their output phases synchronized. See *Output Synchronization (SYNC)*.
     - Configure the output auto-mute modes, output mute levels, and APLL and DPLL mute options. See *Output Auto-Mute During LOL or LOS*.
   - Clock output Interfacing: Follow the single-ended or differential clock output interface examples in Figure 67 or *Clock Output Interfacing and Termination*.
     - Differential outputs should be AC-coupled and terminated and biased at the receiver inputs.
     - HCSL outputs should have 50-Ω termination to GND (at source or load side) unless the internal source termination is enabled by programming.
     - LVCMOS outputs have internal source termination to drive 50-Ω traces directly. LVCMOS V_{OH} level is determined by VDDO voltage (1.8 V and 2.5 V).
   - **TICS Pro:** Configure the PLL loop mode. See *PLL Configurations for Common Applications*.
     - *3-Loop mode*: Supports standards-compliant synchronization using a low-cost holdover TCXO/OCXO, very low loop bandwidths (≤10 Hz), or both. 3-loop mode also supports 1-PPS input synchronization.
     - *2-Loop REF-DPLL mode*: Supports higher loop bandwidth (>10 Hz) and relaxed holdover stability without a TCXO/OCXO.
     - *2-Loop TCXO-DPLL mode*: Locks to a TCXO/OCXO input and is typically used with DCO mode enabled for external clock steering (such as IEEE 1588 PTP).
   - **TICS Pro:** Configure the REF-DPLL loop bandwidth.
     - Below the loop bandwidth, the reference noise is added to the REF-TDC noise floor (and the XO

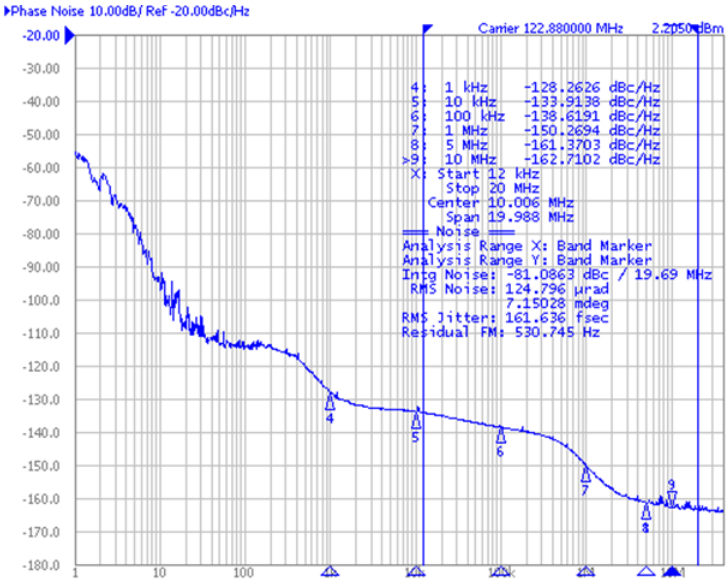
noise in 2-loop mode). Above the loop bandwidth, the reference noise will be attenuated with roll-off up to 60 dB/decade. The optimal bandwidth depends on the relative phase noise between the reference input and the XO (2-loop mode) or the TCXO (3-loop mode).
  - *3-Loop mode*: The bandwidth is typically 10 mHz to 10 Hz to attenuate wander, or determined by the applicable standard specification.
  - *2-Loop mode*: The bandwidth is typically 10 Hz or higher. Target a bandwidth below 200 Hz if the PLL VCO frequency is an integer multiple of the reference input frequency.
- **TICS Pro:** Configure the TCXO-DPLL loop bandwidth.
  - The optimal bandwidth depends on the relative phase noise between the TCXO/OCXO and the XO. Below the loop bandwidth, the TCXO/OCXO noise is added to the TCXO-TDC noise floor. Above the loop bandwidth, the OCXO/TCXO noise will be attenuated.
  - *3-Loop mode*: The bandwidth should be at least 50x higher than the REF-DPLL bandwidth for loop stability.
  - *2-Loop TCXO-DPLL mode*: Target a bandwidth below 300 Hz if the PLL VCO frequency is an integer multiple of the TCXO/OCXO frequency.
- **TICS Pro:** Configure the Market Segment parameter to optimize the DPLL for the desired use case.
  - *SyncE/SONET*: REF-TDC rate is targeted for approximately 400 kHz. Hitless switching is enabled. This supports SyncE/SONET and other use cases using a narrow loop bandwidth (≤10 Hz) in 3-loop mode with a TCXO/OCXO to set the frequency stability and wander performance.
  - *Wireless/BTS*: REF-TDC rate is maximized for lowest in-band TDC noise contribution. Hitless switching is enabled. Supports wireless and other use cases where close-in phase noise is critical. This is used to achieve –112 dBc/Hz at 100-Hz offset for a 122.88-MHz output.
  - *OTN/JitterAtten*: REF-TDC rate is targeted for approximately 1 MHz. Hitless switching is disabled. Supports OTN/OTU and traditional jitter cleaning use cases with wider bandwidths (>10 Hz) in 2-loop mode and relaxed holdover frequency accuracy (no TCXO/OCXO).
- **TICS Pro:** If clock steering is needed (such as for IEEE 1588 PTP), configure DCO mode for the REF or TCXO loop and enter the frequency step size (in ppb). The FDEV step register will be computed according to *DCO Frequency Step Size*. To allow DCO frequency updates using the external control pins, enable the FINC/FDEC functionality on the needed GPIO pins by setting the appropriate register bits (GPIO[3:6]_FDEV_EN).
- **TICS Pro:** If deterministic input-to-output clock phase is needed, configure Zero-Delay mode and select the primary output channel that must be phase-aligned with the input. For DPLL1, any output from the OUT[4:7] bank can be selected for zero-delay feedback. For DPLL2, any output from the OUT[0:3] bank can be selected for zero-delay feedback. See *Zero-Delay Mode (ZDM) Configuration*.

6. **TICS Pro:** Configure the reference input monitoring options for each reference input. Disable the monitor when not required or when the input operates beyond the monitor's supported frequency range. See *Reference Input Monitoring*.
   - *Amplitude monitor*: Set the LVCMOS detected slew rate edge or the differential input amplitude threshold to monitor input signal quality. Disable the monitor for a differential input below 5 MHz or else use LVCMOS input clock.
   - *Frequency monitor*: Set the valid and invalid thresholds (in ppm).
   - *Missing pulse monitor*: Set the late window threshold (T_{LATE}) to allow for the longest expected input clock period, including worst-case cycle-to-cycle jitter. For a gapped clock input, set T_{LATE} based on the number of allowable missing clock pulses.
   - *Runt pulse monitor*: Set the early window threshold (T_{EARLY}) to allow for the shortest expected input clock period, including worst-case cycle-to-cycle jitter.
   - *1-PPS Phase validation monitor*: Set the phase validation jitter threshold, including worst-case input cycle-to-cycle jitter.
   - *Validation timer*: Set the amount of time the reference input must be qualified by all enabled input monitors before the input is valid for selection.
7. **TICS Pro:** Configure the DPLL lock detect and tuning word history monitoring options for each channel. See *PLL Lock Detectors* and *Tuning Word History*.
   - *DPLL tuning word history*: Set the history count/averaging time (T_{AVG}), history delay/ignore time (T_{IGN}), and intermediate averaging option.

– *DPLL frequency lock and phase lock detectors*: Set the lock and unlock thresholds for each detector.

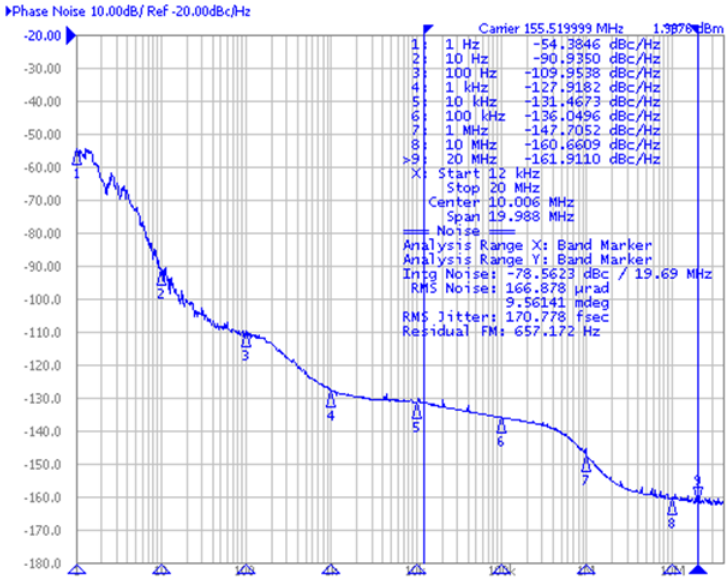
8. **TICS Pro:** Configure each status output pin and interrupt flag as needed. See *Status Outputs* and *Interrupt*.
   – Select the desired status signal selection, status polarity, and driver mode (3.3-V LVCMOS or open-drain). Open-drain requires an external pullup resistor.
   – If the Interrupt is enabled and selected as a status output, configure the mask bit for any interrupt source to be ignored, interrupt flag polarity, and the combinational gate logic (AND/$\overline{\text{OR}}$) as desired.

10.2.3 Application Curves



AC-LVPECL output, f_{IN} = 25 MHz, f_{TCXO} = 10 MHz (OCXO), f_{XO} = 48.0048 MHz, $f_{TCXO-TDC}$ = 20 MHz

Figure 68. 122.88-MHz Output Phase Noise (3-Loop), Wireless Use Case



AC-LVPECL output, f_{IN} = 19.44 MHz, f_{TCXO} = 12.8 MHz (OCXO), f_{XO} = 48.0048 MHz, $f_{TCXO-TDC}$ = 25.6 MHz, $BW_{REF-DPLL}$ = 1 Hz, $BW_{TCXO-DPLL}$ = 200 Hz

Figure 69. 155.52-MHz Output Phase Noise (3-Loop), Telecom Use Case

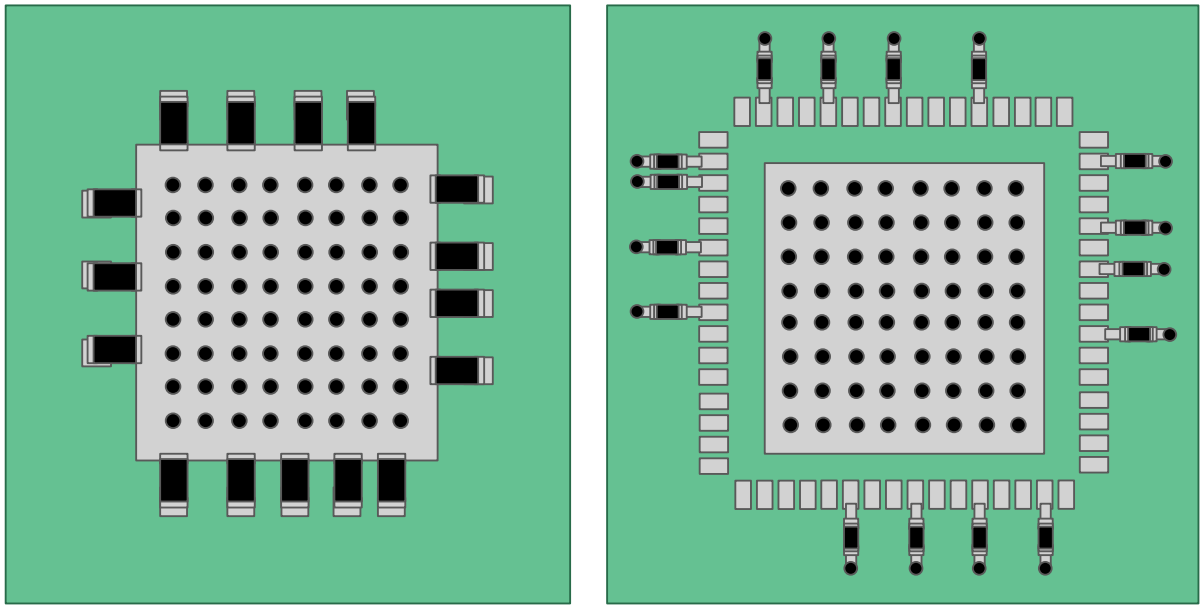
10.3 Do's and Don'ts

- Power all VDD pins with proper supply decoupling and bypassing connect like shown in Figure 67.
- Power down unused blocks through registers to minimize power consumption.
- Leave unused clock outputs floating and powered down through register control.
- Leave unused clock inputs floating.
- For EEPROM+SPI Mode: Leave HW_SW_CTRL and STATUS[1:0] pins floating during POR to ensure proper start-up. These pins has internal biasing to V_{IM} internally.
  - If HW_SW_CTRL or either STATUS pin is connected to a host device (MCU or FPGA), the external device must be configured with high-impedance input (no pullup or pulldown resistors) to avoid conflict with the internal bias to V_{IM}. If needed, external biasing resistors (10-kΩ pullup to 3.3 V and 3.3-kΩ pulldown) can be connected on each STATUS pin to bias the inputs to V_{IM} during POR.
- Use a low-noise, high-PSRR LDO regulator to power the external oscillators used to drive the XO and TCXO inputs. Typically, oscillator jitter performance is typically impacted by switching noise on its power supply.
- Include a dedicated serial port to the I^2C or SPI pins of the LMK05028.
  - This allows off-board programming for device bring-up, debug, and diagnostics using TI's USB hardware interface and software GUI tools.

11 Power Supply Recommendations

11.1 Power Supply Bypassing

Figure 70 shows two general placements of power supply bypass capacitors on either the back side or the component side of the PCB. If the capacitors are mounted on the back side, 0402 components can be employed. For component side mounting, use 0201 body size capacitors to facilitate signal routing. A combination of component side and back side placement can be used. Keep the connections between the bypass capacitors and the power supply on the device as short as possible. Ground the other side of the capacitor using a low-impedance connection to the ground plane.



Back Side Component Side

(**Does not** indicate actual location of the LMK05028 supply pins)

Figure 70. Generalized Placement of Power Supply Bypass Capacitors

12 Layout

12.1 Layout Guidelines

- Isolate input, XO, TCXO/OCXO, and output clocks from adjacent clocks with different frequencies and other nearby dynamic signals.
- Consider the XO and TCXO/OCXO placement and layout in terms of supply/ground noise and thermal gradients from adjacent circuitry (for example, power supplies, FPGA, ASIC) as well as system/board-level vibration and shock. These factors can affect the frequency stability/accuracy and transient performance of the oscillators.
- Avoid impedance discontinuities on controlled-impedance 50-Ω single-ended (or 100-Ω differential) traces for clock and dynamic logic signals.
- Place bypass capacitors close to the VDD and VDDO pins on the same side as the LMK05028, or directly below the IC pins on the back side of the PCB. Larger decoupling capacitor values can be placed further away.
- Place external capacitors close to the CAP_x and LFx pins.
- If possible, use multiple vias to connect wide supply traces to the respective power islands or planes.
- Use at least 7x7 through-hole via pattern to connect the IC ground/thermal pad to the PCB ground planes.

12.2 Layout Example

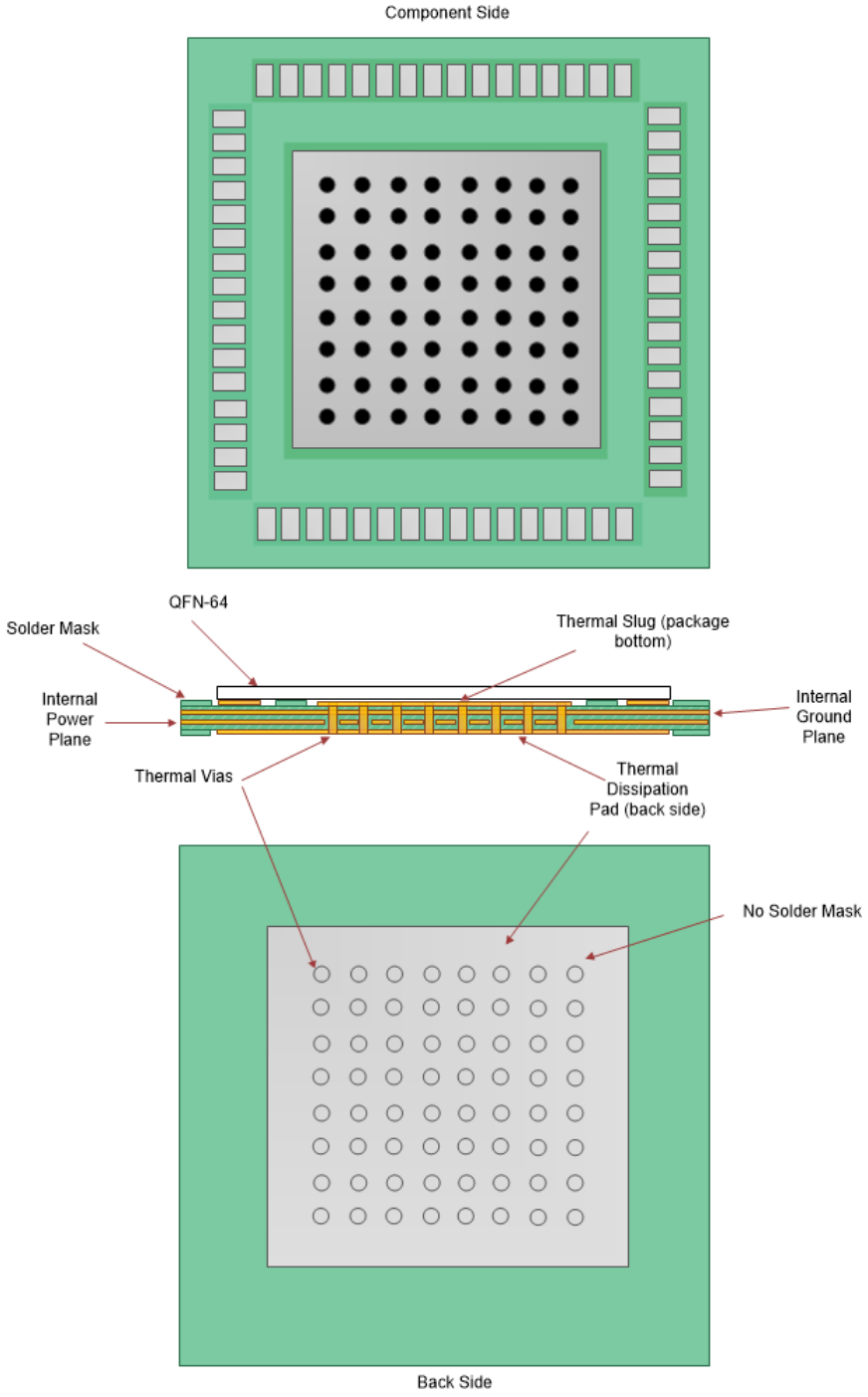


Figure 71. General PCB Ground Layout for Thermal Reliability (8+ Layers Recommended)

12.3 Thermal Reliability

The LMK05028 is a high-performance device. To ensure good electrical and thermal performance, it is recommended to design a thermally-enhanced interface between the IC ground/thermal pad and the PCB ground using at least 7x7 through-hole via pattern connected to multiple PCB ground layers like shown in Figure 71.

13 Device and Documentation Support

13.1 Device Support

13.1.1 Clock Architect

Clock Architect is an online tool used for part selection with the LMK05028. It also supports part selection, loop filter design, and phase noise simulation for other TI clock devices. For Clock Architect, go to www.ti.com/clockarchitect.

13.1.2 TICS Pro

TICS Pro is an offline software tool for EVM programming and also for register map generation to program a device configuration for a specific application. For TICS Pro, go to www.ti.com/tool/TICSPRO-SW.

13.2 Documentation Support

13.2.1 Related Documentation

For related documentation, see the following:

- *ITU-T G.8262 Compliance Test Result for the LMK05028* (SNAA315)
- *LMK05028 Programming Guide* (SNAU233)
- *LMK05028EVM User's Guide* (SNAU223)

13.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

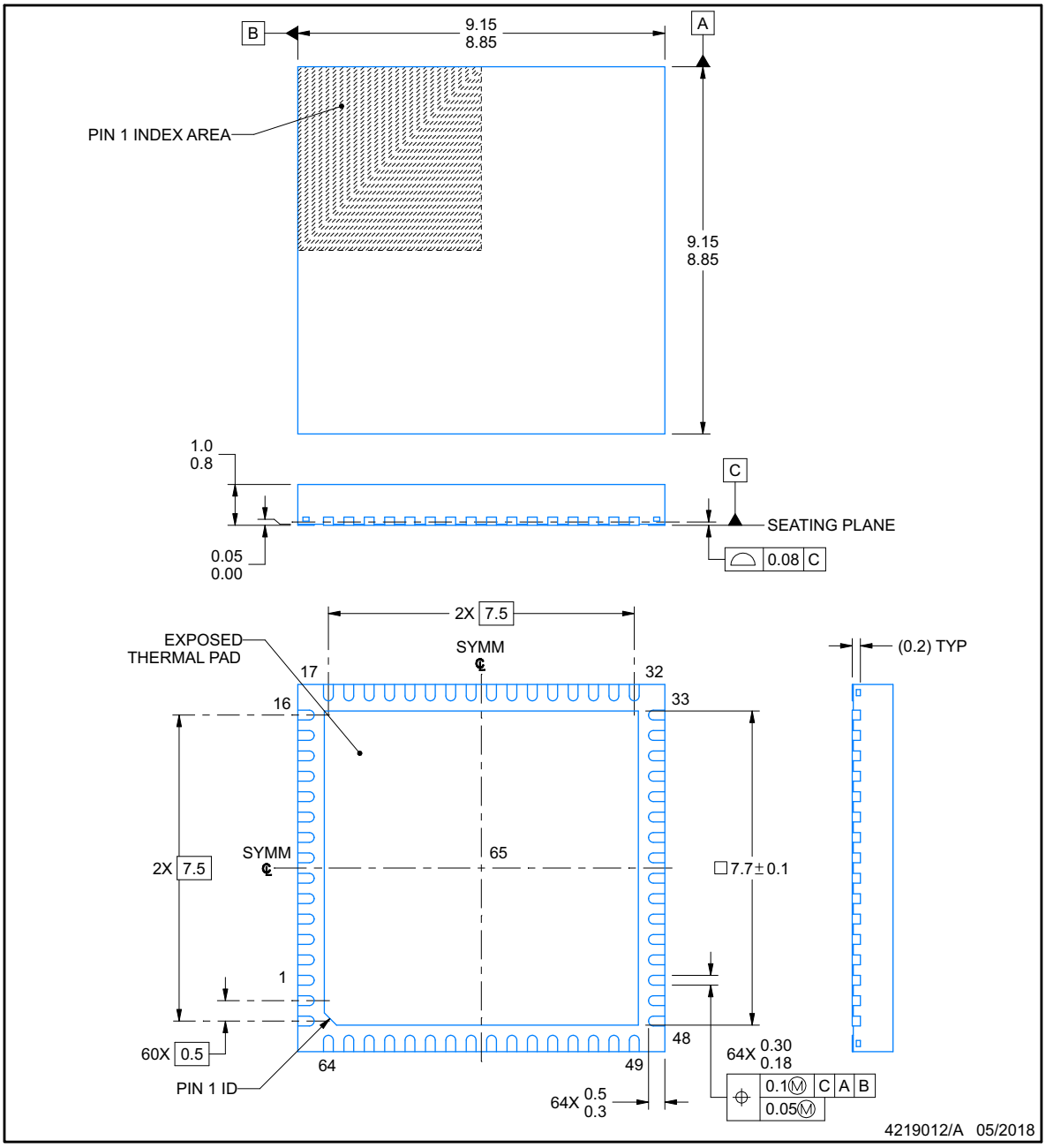
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

RGC0064J

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



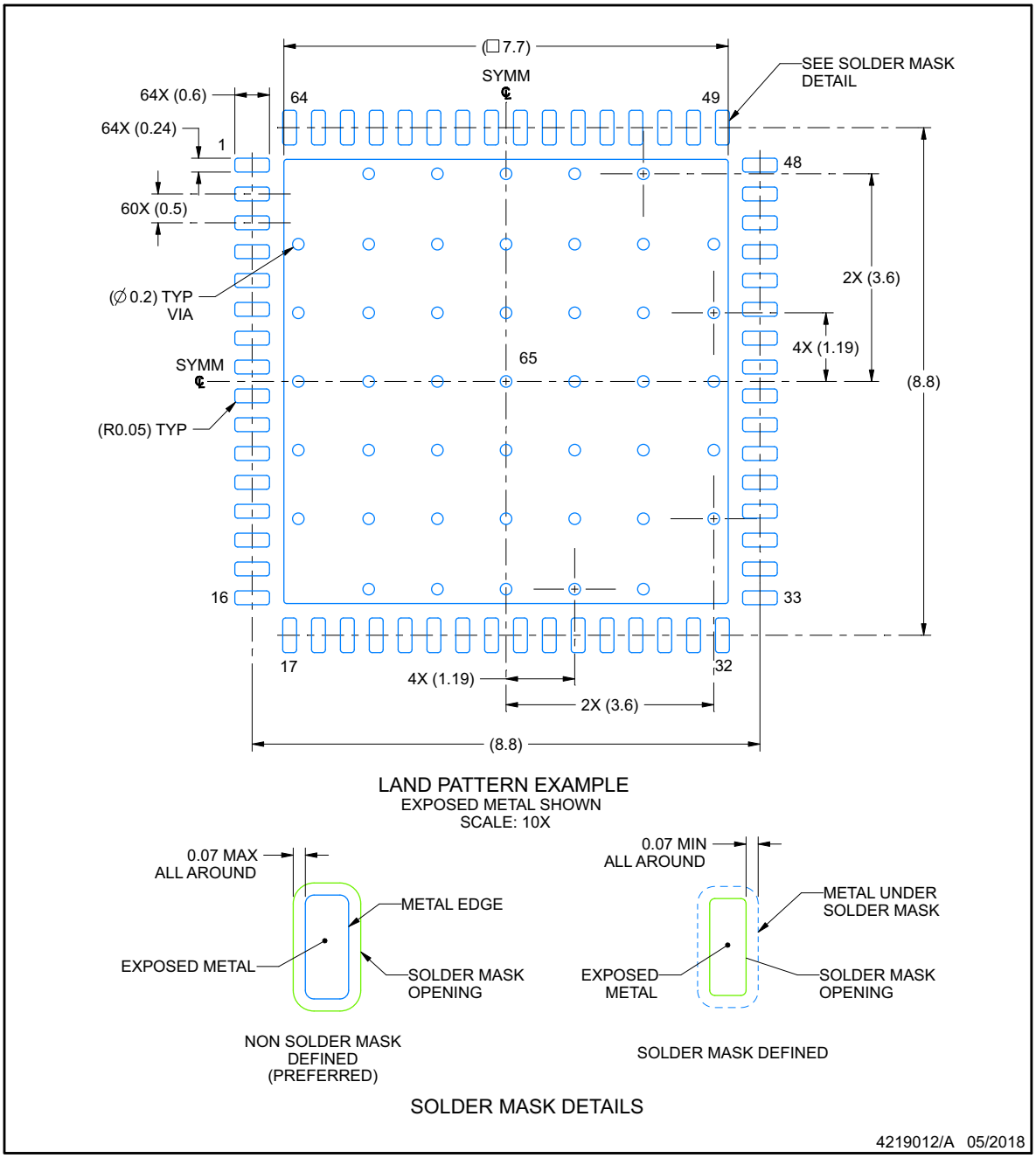
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

RGC0064J — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



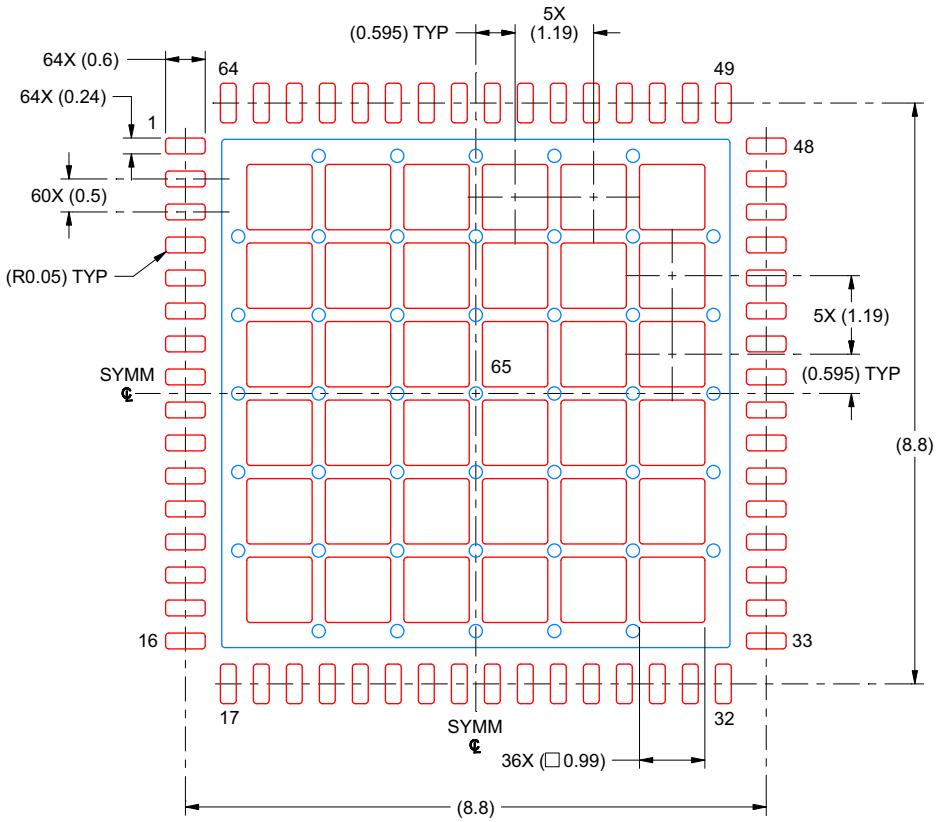
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGC0064J — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 10X

EXPOSED PAD 65
60% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4219012/A 05/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMK05028RGCR	ACTIVE	VQFN	RGC	64	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	K5028	Samples
LMK05028RGCT	ACTIVE	VQFN	RGC	64	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	K5028	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

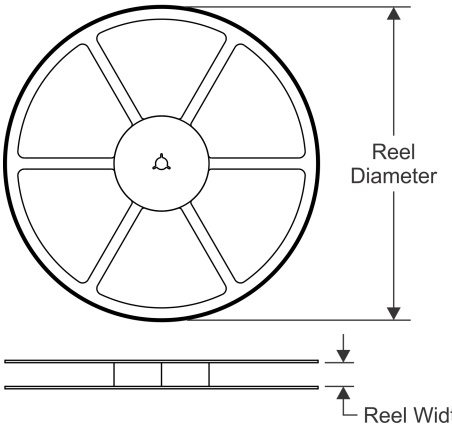
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

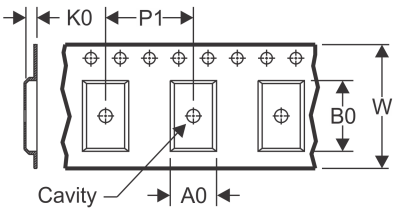
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

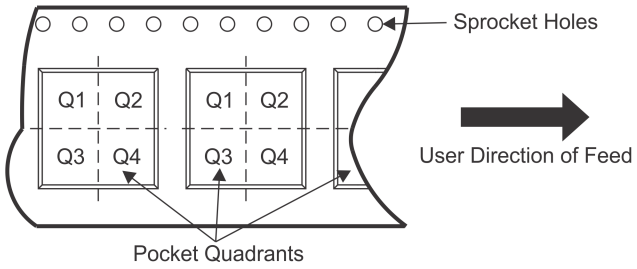


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

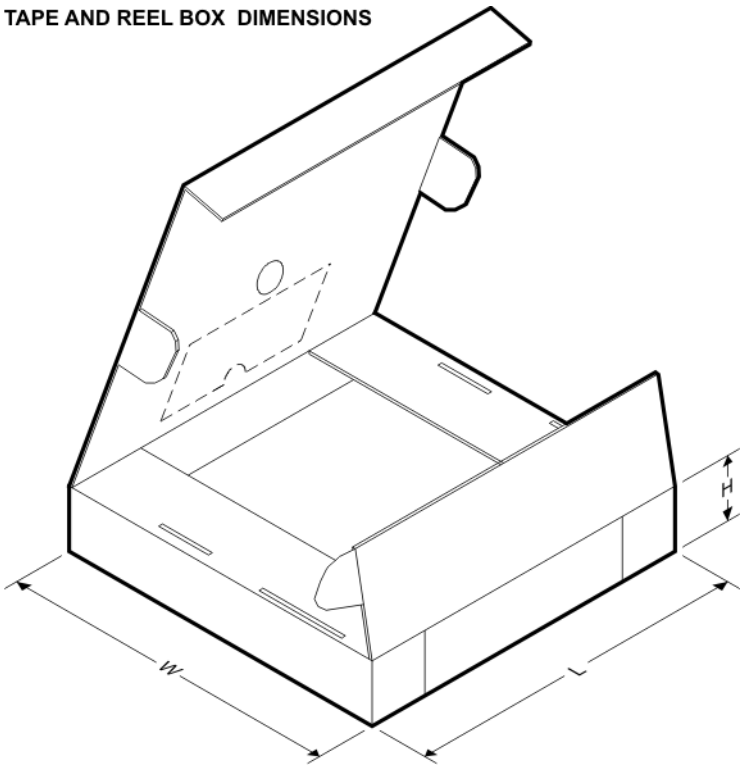
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LMK05028RGCR	VQFN	RGC	64	2500	330.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2
LMK05028RGCT	VQFN	RGC	64	250	180.0	16.4	9.3	9.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LMK05028RGCR	VQFN	RGC	64	2500	367.0	367.0	38.0
LMK05028RGCT	VQFN	RGC	64	250	210.0	185.0	35.0

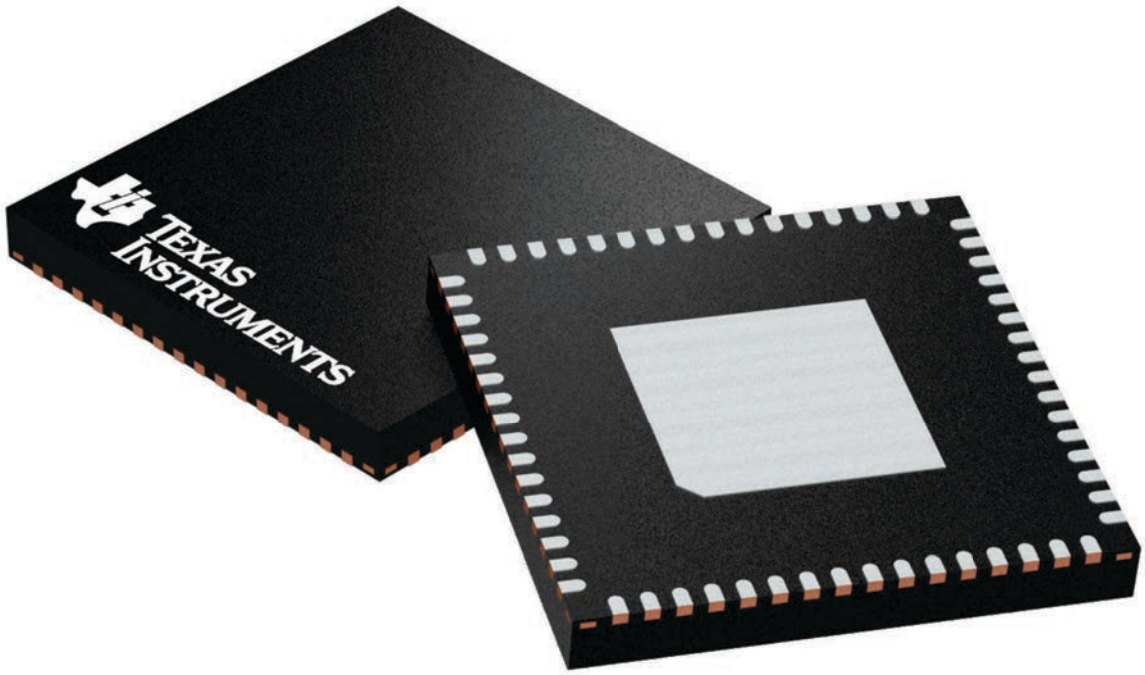
GENERIC PACKAGE VIEW

RGC 64

VQFN - 1 mm max height

9 x 9, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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