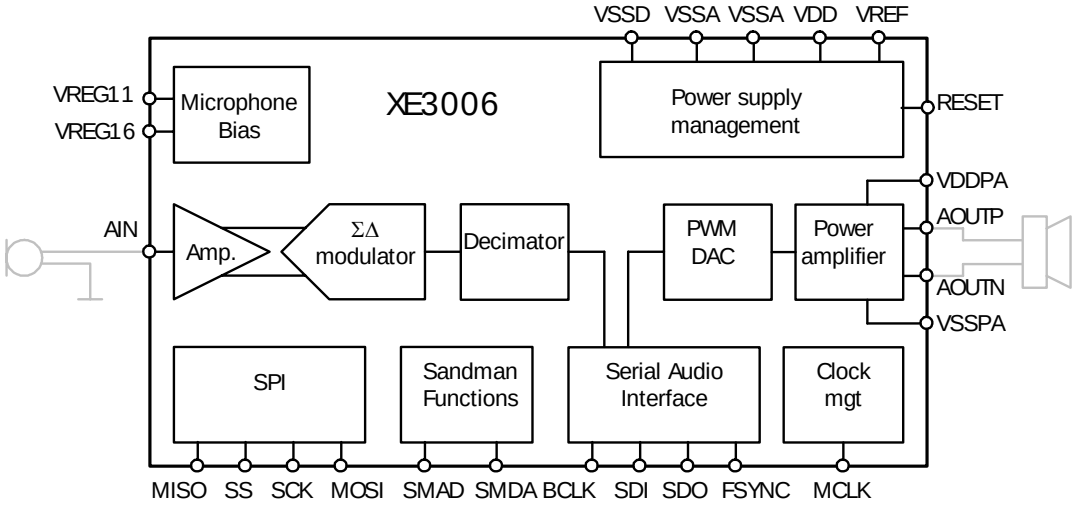


XE3005 / XE3006

Low-Power Audio CODEC

GENERAL DESCRIPTION

The XE3005 is an ultra low-power CODEC (Analog to Digital and Digital to Analog Converter) for voice and audio applications. It includes microphone supply, preamplifier, 16-bit ADC, 16-bit DAC, serial audio interface, power management and clock management for the ADC and the DAC. The sampling frequency of the ADC and of the DAC can be adjusted from 4 kHz to 48 kHz.

The XE3006 also includes the Sandman™ function, which signals whether a relevant voice or audio signal is present for the ADC or DAC.

APPLICATIONS

- Wireless Headsets
- Bluetooth™ headset
- Hands-free telephony
- Digital hearing instruments
- Consumer and multimedia applications
- All battery-operated portable audio devices

FEATURES

- Ultra low-power consumption, below 2 mW
- Low-voltage operation down to 1.8 V
- Sandman™ function to reduce system power consumption (XE3006)
- Single supply voltage
- Adjustable sampling frequency: 4 – 48 kHz
- Digital format: 16 bit 2s complement
- Requires a minimum number of external components
- Easy interfacing to various DSPs
- Direct connection to microphone and speaker
- Various programming options

QUICK REFERENCE DATA

• supply voltage	1.8 – 3.6 V
• current (@20 kHz sampling)	0.4 mA
• sampling frequency	4 – 48 kHz
• Typical dynamic range ADC	78 dB
• Typical dynamic range DAC	78 dB

ORDERING INFORMATION

Part	Package	Ext. part no.	Temp. range
XE3005	TSSOP 20 pins	XE3005I033TRLF	-20 to 70° C
XE3005	Lead free uCSP® 20 balls	XE3005I064TRLF	-20 to 70° C
XE3006	TSSOP 24 pins	XE3006I019	-20 to 70° C

Table of Contents

1 DEVICE DESCRIPTION

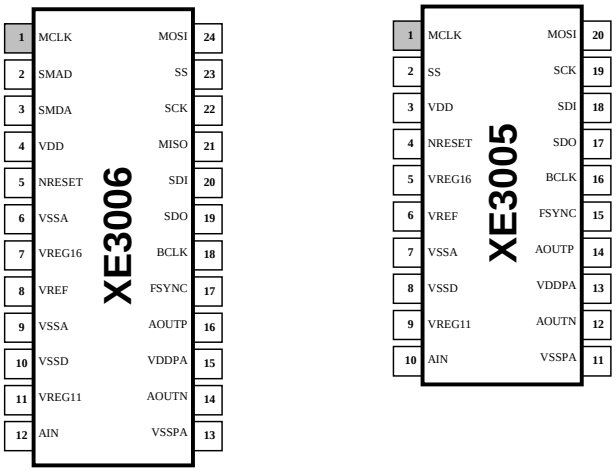


Figure 1: Pin layout of the XE3006 and XE3005 in TSSOP

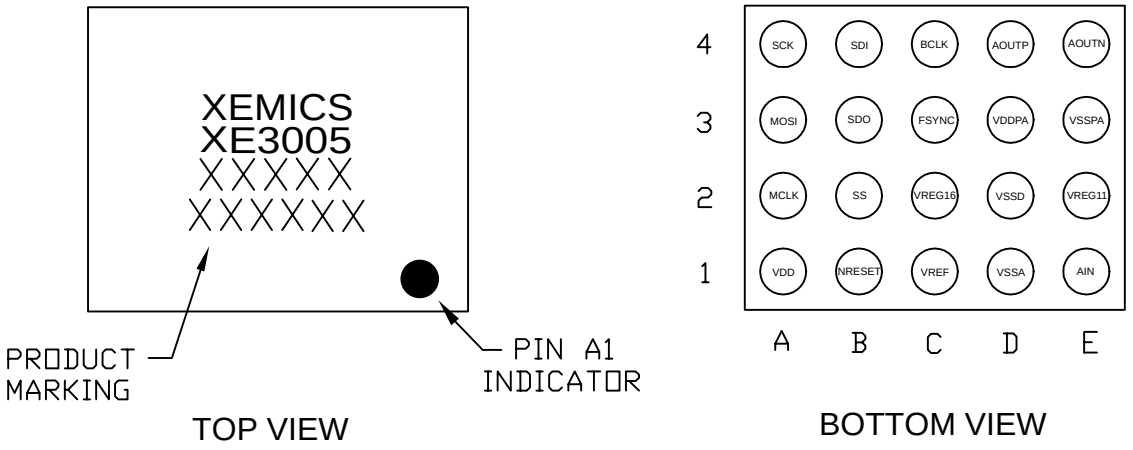


Figure 2: Pin layout of the XE3005 in uCSP®

The XE3006 is available in a TSSOP24 package. The XE3005 is available in a TSSOP20 and uCSP® package. Detailed information is found in chapter 8, Mechanical Information.

1.1 TERMINALS DESCRIPTION XE3005/6

Terminals					Description
XE3006	XE3005		Name	Type [1]	
TSSOP24	TSSOP20	uCSP®			
1	1	A2	MCLK	DI	Master Clock. MCLK derives the internal clocks of ADC and DAC
2	N/A	N/A	SMAD	DO	Sandman output ADC
3	N/A	N/A	SMDA	DO	Sandman output DAC
4	3	A1	VDD	AI	Digital power supply
5	4	B1	NRESET	ZI/O	Reset signal generated by the CODEC. If required, the reset signal can be applied externally to initialize all the internal CODEC registers
6	N/A	N/A	VSSA	AI	Analog ground
7	5	C2	VREG16	AO	Regulator voltage 1.6 V. Can be used to supply the microphone
8	6	C1	VREF	AO	Reference voltage
9	7	D1	VSSA	AI	Analog ground
10	8	D2	VSSD	AI	Digital ground
11	9	E2	VREG11	AO	ADC Regulated microphone output supply voltage 1.1 V
12	10	E1	AIN	AI	ADC Analog input signal
13	11	E3	VSSPA	AI	DAC Power Amplifier Ground
14	12	E4	AOUTN	AO	DAC Analog Output negative
15	13	D3	VDDPA	AI	DAC Power Amplifier Supply
16	14	D4	AOUTP	AO	DAC Analog Output positive
17	15	C3	FSYNC	DI/O	Serial audio interface Frame Synchronization
18	16	C4	BCLK	DI/O	Serial audio interface Bit Clock
19	17	B3	SDO	ZO	Serial audio interface Data Output
20	18	B4	SDI	DI PD	Serial audio interface Data Input
21	N/A	N/A	MISO	ZO	SPI Master In Slave Out
22	19	A4	SCK	DI PD	SPI Serial Clock
23	2	B2	SS	DI PU	SPI Slave Select
24	20	A3	MOSI	DI PD	SPI Master Out Slave In

Note: (1) AI = Analog Input AO = Analog Output
DI = Digital Input DO = Digital Output
DI/O = Digital In or Out ZO = Hi Impedance or Output
PU = internal Pull Up PD = internal Pull Down
ZI/O = Hi impedance In or Out

2 FUNCTIONAL DESCRIPTION

A CODEC is typically used for voice and audio applications as an interface between a Digital Signal processor (DSP) or microcontroller and the analogue interfaces like a microphone and loudspeaker.

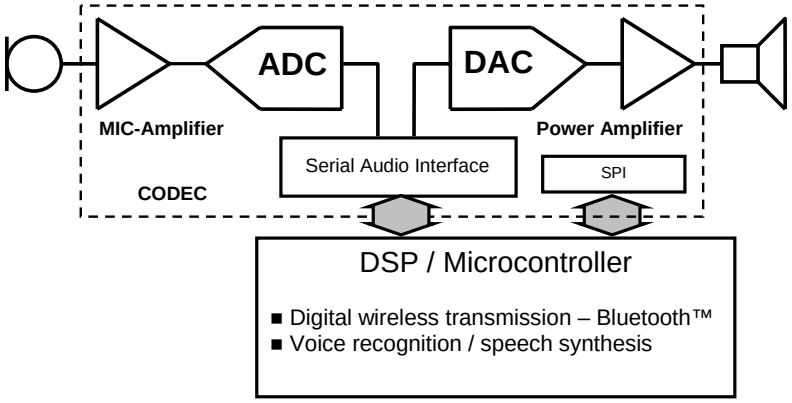


Figure 3: Typical usage of CODEC

This chapter provides a brief description of the CODEC features relating to the CODEC configuration. The configuration of the CODEC is defined by programming registers through a serial interface. A detailed description of the registers defining details of the CODEC setup can be found in chapter 3 and 7. Digital voice and audio samples are passed through the Serial Audio Interface.

2.1 DEVICE FUNCTIONS

2.1.1 ADC Signal Channel

The ADC channel is a chain of programmable amplifier, band-pass filter, sigma-delta modulator and a decimation filter. The amplifier gain is programmable to 5x (default) and 20x. The band-pass filter has cut-off frequencies proportional to the sampling rate. The sigma-delta modulator operates at a frequency of 64 times the sampling rate. The analog modulator is followed by a digital decimation filter. The digital output data (16 bits, 2's complement format) is made available through the Serial Audio Interface. The format of the Serial Audio interface can be selected through register J.

With the default register settings the ADC can run at a sampling frequency up to 20 kHz. When used with a sampling frequency higher than 20 kHz, then register C has to be changed.

The whole ADC chain can be powered-down through register I.

2.1.2 MIC Input

The programmable pre-amplifier and the microphone bias sources VREG11 or VREG16 are optimized to operate with electret microphones. VREG11 provides a 1.1 V reference voltage. The VREG11 can deliver up to 50 µA. VREG11 is enabled through control register E. VREG16 is a regulated voltage of typically 1.6V and can deliver up to 1 mA.VREG16 is always enabled.

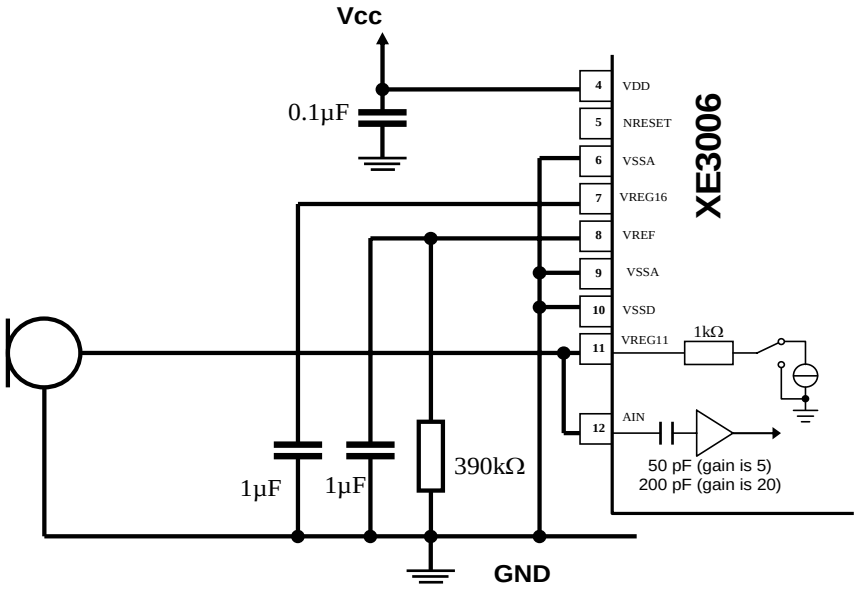


Figure 4: Typical microphone interface (1.1 V / 50 uA bias through VREG11)

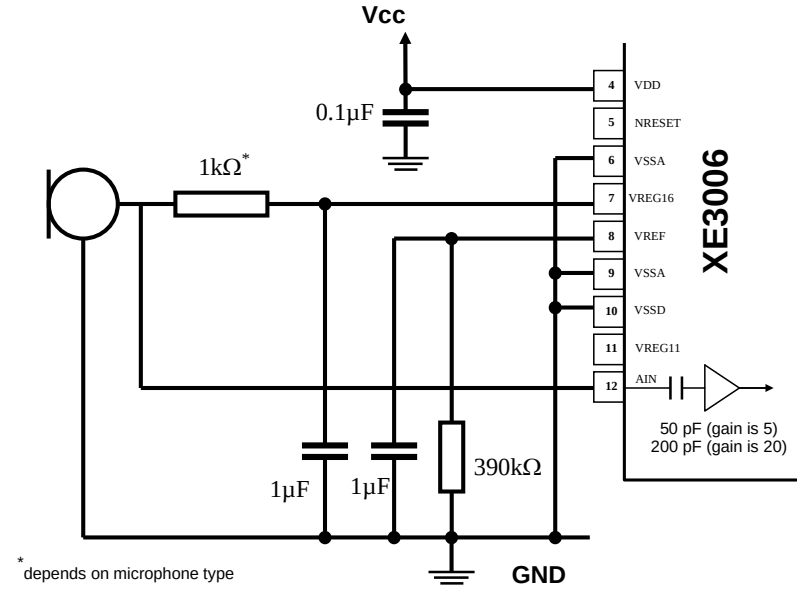


Figure 5: Typical microphone interface (1.6 V / 1 mA bias through VREG16)

2.1.3 DAC Signal Channel

The DAC is based on a multi bit sigma-delta modulator, which operates at a frequency of 8 times the sampling rate. The outputs of the modulator are 2's complement words of 6 bit. A pulse-width modulator (PWM) converts the 6 bit words into 2 single bit streams at 256 times the sampling frequency. Finally the 2 bit streams are supplied to the power amplifier. The Power Amplifier is a Class D amplifier, which offers higher efficiency than the traditional Class AB topologies. It uses a three-state unbalanced PWM. This means that both channels of the PA (AOUTP and AOUTN) will not switch at the same time, therefore the outputs are not purely differential (see figure 5 and 6)

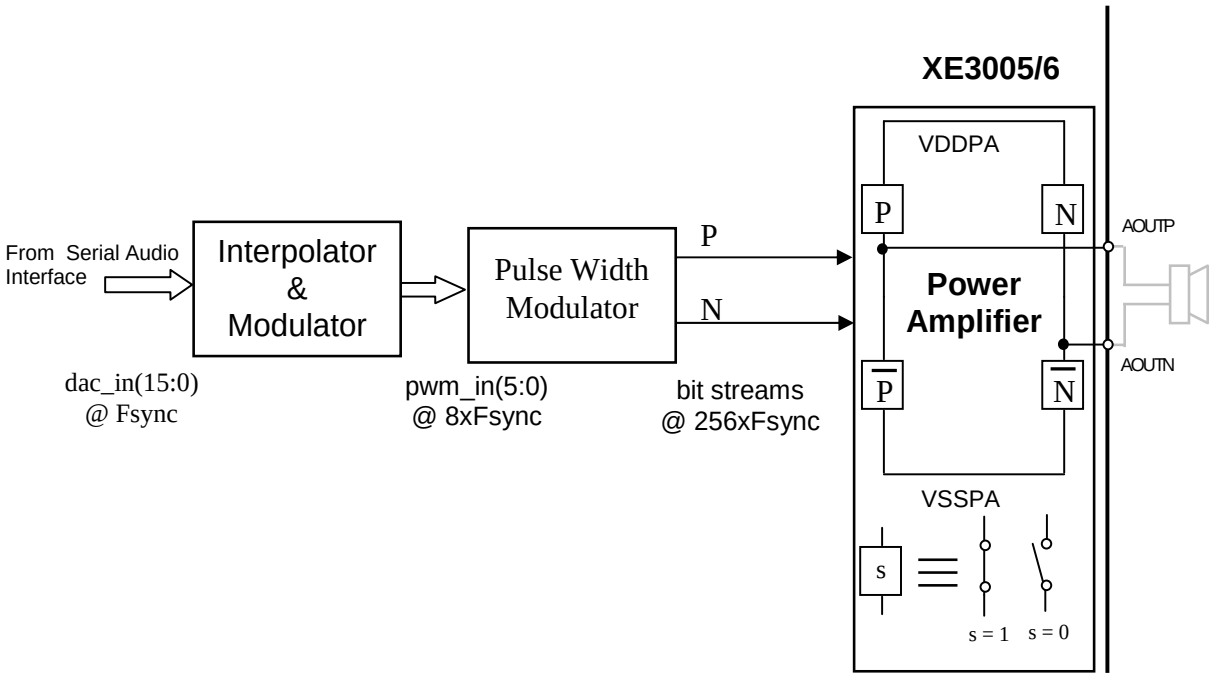


Figure 6: DAC block diagram

Figure 6 shows the relation of input and output samples of the PWM (The timing diagram is not to scale in the time-axis).

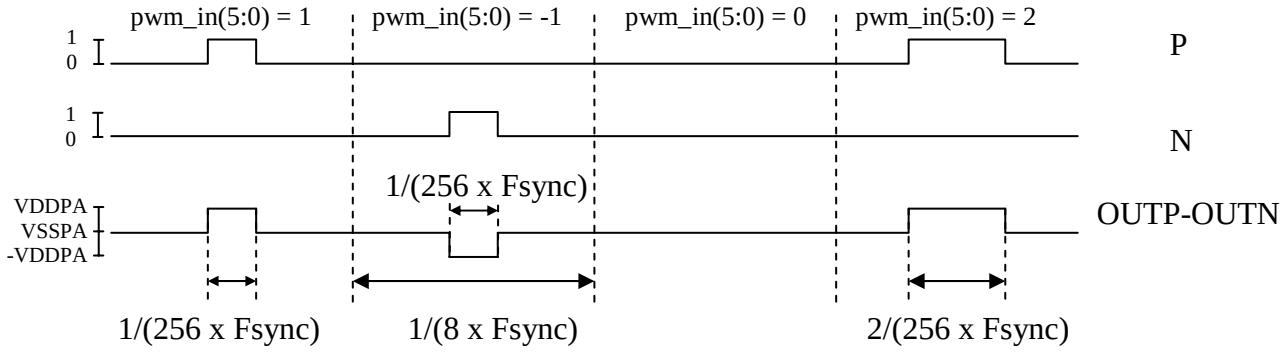


Figure 7: Examples PWM in and out (not to scale)

The DAC receives 16-bit wide 2's complement format through the Serial Audio Interface. The protocol can be selected through register J. The complete DAC and PA amplifier chain can be powered-down through register I.

2.1.4 Digital Loop Back

In digital loop back mode, the ADC output is routed directly to the DAC input. This allows in-circuit system level tests. The digital loop back mode can be selected through register J.

2.1.5 Operating Frequency

A master clock (MCLK) has to be applied to the XE3005/3006. The clock frequency of the signal applied to the MCLK pin may vary between 1.024 MHz minimum and 33.9 MHz maximum. The maximum internal clock signal frequency (MCLK/div_factor) should not exceed 12.288 MHz.

The div_factor can be set by the user in register I to 1,2 or 4. The default value for div_factor is '1'.

2.1.6 Serial Audio Interface

The Serial Audio Interface is a 4-wire interface for bi-directional communication of audio data. It operates on the bit serial clock BCLK and the frame synchronization signal FSYNC. The sampling frequency of the CODEC corresponds to the rate at which the Audio Serial Interface will put out succeeding frames. One frame always corresponds to one sample. One frame always contains 2 channels.

Synchronizing the Serial Audio Interface to the MCLK is recommended. FSYNC and MCLK must have a fixed ratio as defined by the following relation:

FSYNC = Sampling frequency = frame rate = MCLK/(256 x div_factor).

The pin BCLK defines the time when the data must be presented to the serial audio interface and shifted into (pin SDI) or out of (pin SDO) the CODEC. The number of BCLK periods in one FSYNC period is 32. The user can select to use the first 16 clock cycles (channel 1) or the second 16 clock cycles (channel 2) of BLCK to shift in or out the data samples.

The table below shows some examples of the relationships between MCLK, BCLK and FSYNC

MCLK	Div_factor	BCLK	FSYNC
2048 kHz	1	256 kHz	8 kHz
8192 kHz	4	256 kHz	8 kHz
5120 kHz	1	640 kHz	20 kHz
22579.2 kHz	2	1411.2 kHz	44.1 kHz

The table below shows the possible functional configurations of the serial audio interface

CODEC	supported protocol
master	LFS (Long Frame Sync)
slave	LFS, LFS Optimization and SFS (Short Frame Sync)

By default the Serial Audio Interface operates in slave, SFS mode. In slave mode the user needs to generate the signals BLCK, FSYNC and supply to the CODEC.

In master mode the CODEC generates the BLCK and FSYNC signals. In that case the BLCK operates at 32 times the frequency of FSYNC. The CODEC master mode can be used with the LFS protocol only.
The register J is used for the different setups of the serial audio interface.

2.1.7 Serial Peripheral Interface - SPI

The SPI interface is used to control register values. It is a serial communications interface that is independent of the rest of the CODEC. It allows the device to communicate synchronously with a microprocessor or DSP. The CODEC interface only implements a slave controller.
A detailed description can be found in chapter 3.3.

2.1.8 Sandman™ ADC Function

The Sandman™ function monitors the signals, which are processed in the ADC signal channel and the DAC signal channel. The logic output signal SMAD indicates whether the ADC signal channel has processed an audio signal or only noise, and for how long. The reference signal amplitude can be selected through register O, the time window parameters are the off time and on time (registers L, M and N).

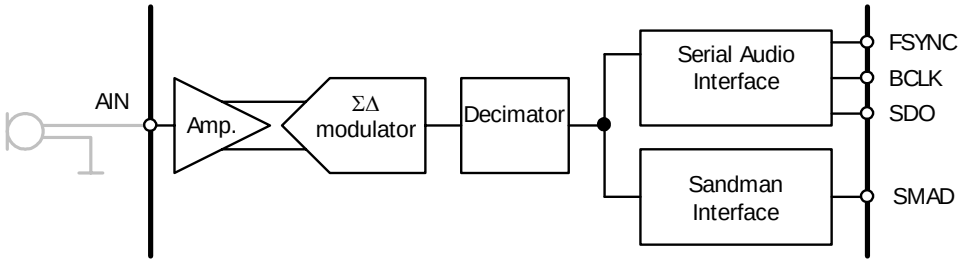


Figure 8: Implementation of the Sandman function for the ADC (SMAD)

The logic output SMAD can be used to power-down or reduce clock speed in other devices in the application, such as a microcontroller, DSP or wireless link. Also, SMAD can be used as phone pick-up indicator. The Sandman™ function is illustrated in Figure 9 and is valid for both SMAD (related to the ADC signal) and SMDA (related to the DAC signal).

Initially, SMAD is inactive (low), which means that “noise” is processed by the ADC, i.e. no audio signal amplitude above the Reference. The Sandman™ Interface compares every output sample of the ADC signal channel to the Reference value. If the signal is lower than the Reference value, SMAD remains inactive (low).

As soon as the signal passes the reference (time = 1), the on-time counter is started. (for the moment defined by time=’x’ see Figure 9). However, as the signal returns below the reference (time = 2) before the on-time counter has reached the on time, the on-time counter is reset and the SMAD signal remains inactive (low).

The next time the signal gets higher than the Reference (time = 3), the on-time counter is started again and when it reaches the on time, the SMAD signal becomes active (high), indicating that an audio signal is present (time = 4). As long as the signal remains above the Reference, nothing happens and the SMAD signal remains active (high). When the signal falls below the Reference (time = 5), the off-time counter is started, but as it does not reach the off time before the signal passes again the Reference (time = 6), SMAD remains active (high). Also during the period from time = 7 to time = 8, the off time counter does not reach the off time.
When the signal falls below the Reference (time = 9) and remains below the Reference until the off-time counter has reached the off-time, the SMAD signal is changed into the inactive (low) state (time = 10).

2.1.9 Sandman™ DAC Function

The Sandman™ function monitors the signals, which are processed in the ADC signal, channel and the DAC signal channel. The logic output signal SMDA indicates whether the DAC signal channel processes an audio signal or only noise, and this for certain duration. The reference signal amplitude can be selected through register P, the time window parameters are the off time and on time (registers L, M and N).

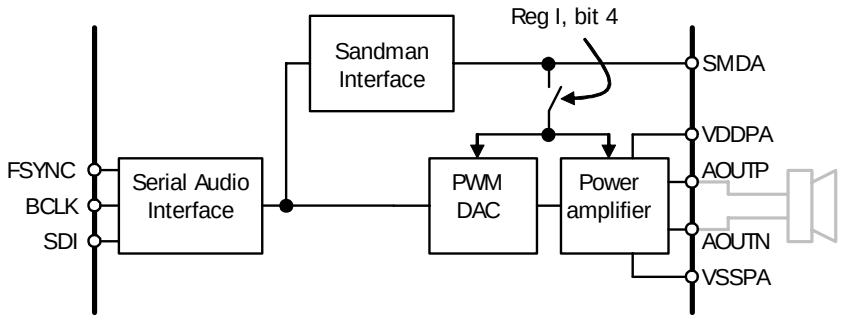


Figure 9: Implementation of the Sandman function for the DAC (SMDA)

The logic output SMDA can be employed to power-down other devices in the application, such as an external audio power amplifier. By setting bit 4 in register I, the on-chip DAC signal channel can be powered-down through SMDA too. The Sandman™ function is illustrated in Figure 9 and is valid for both SMAD (related to the ADC signal) and SMDA (related to the DAC signal).

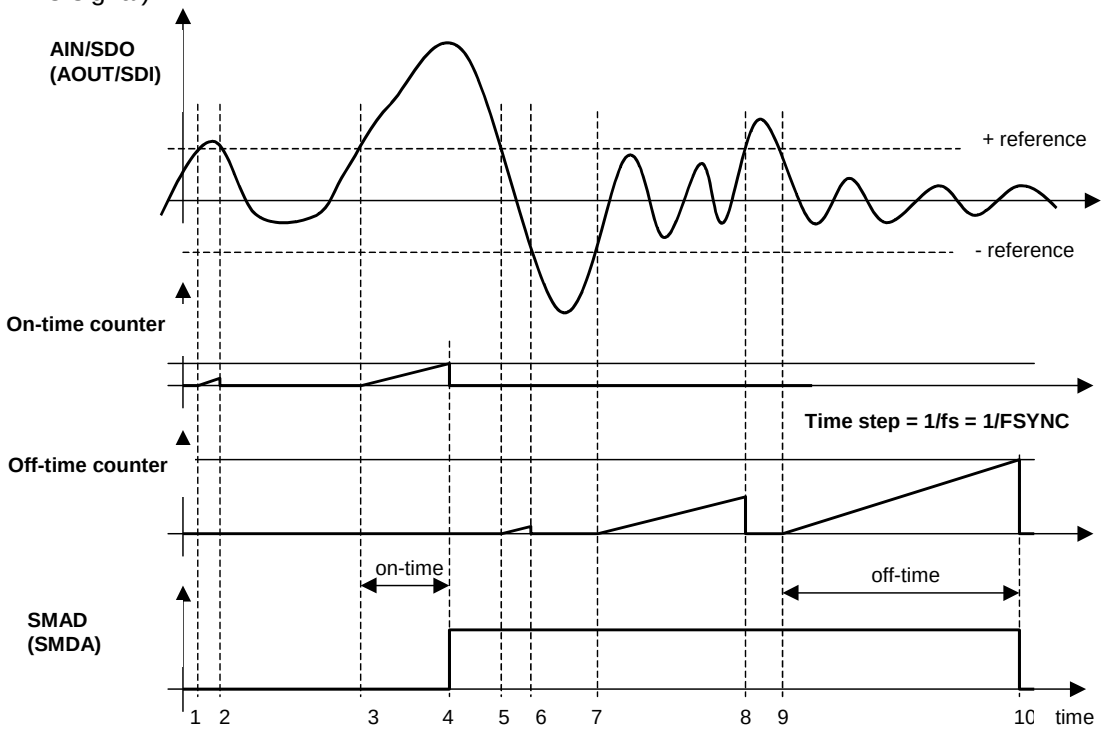


Figure 10: Illustration of the Sandman™ function.

The above illustration is valid for either the SMAD output as a result of AIN/SDO or for the SMDA output as a function of AOUT/SDI.

2.1.10 Start-up and Initialization

The CODEC generates its own power on reset signal after a power supply is connected to the VDD pin. The reset signal is made available for the user at the pin NRESET. The rising edge of the NRESET indicates that the startup sequence of the CODEC has finished. In most applications the NRESET pin can be left open.

The NRESET signal generated by the CODEC is used to initialize the various blocks in the device and guarantees a correct start-up of the circuit. The start-up sequence that is automatically carried out upon power-up of the device is listed below and illustrated in Figure 10.

1. NRESET is low (0V) when the device is not powered and remains low for a short time when VDD (upper curve in Figure 10) is applied. The low state sustains while VDD, VREG16, VREF are stabilizing.

2. As soon as the MCLK signal is present, a counter is activated that counts 2^{21} periods of the MCLK. After this moment the NRESET is in the high state (VDD).

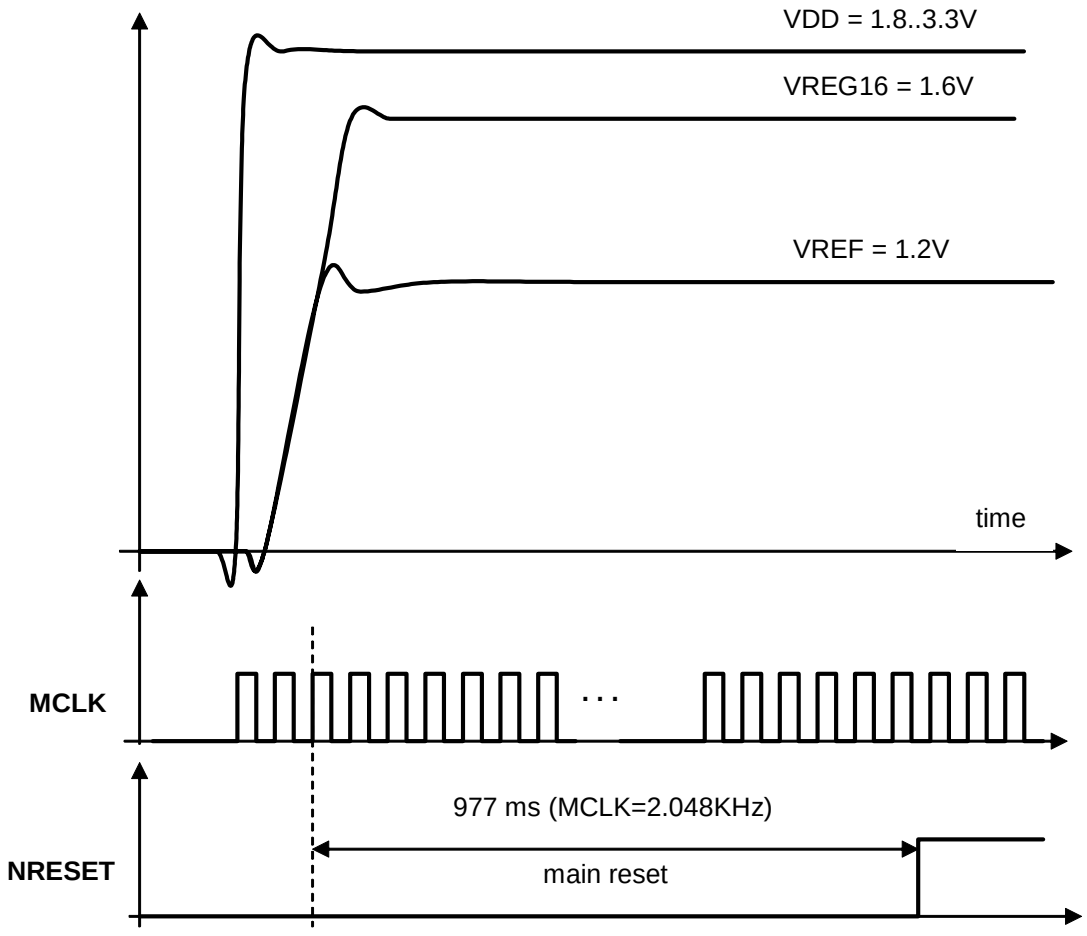


Figure 11: Startup sequence and NRESET signal after power-on.

The user can use the NRESET pin in 3 different ways and combinations:

1. Leave the NRESET pin not connected. In this case the CODEC will startup as described in figure 10.
2. Use the NRESET pin as an output to indicate, to e.g. a microcontroller, that the CODEC finished its power up sequence and that the CODEC is ready to operate.
3. Use the NRESET pin to force a re-initialization of the registers to their default values. In this case the user has to force the NRESET to 0V for at least 32 periods of the MCLK. The circuit which forces the NRESET to 0V should be able to sink at least 50 uA.

Figure 12 shows the block diagram of the CODEC reset.

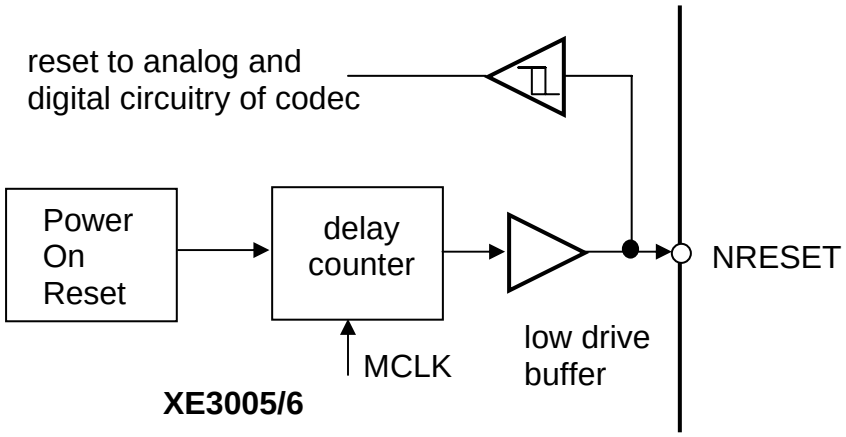


Figure 12: Codec reset circuitry

2.2 POWER-DOWN FUNCTIONS

2.2.1 Software Power-Down

Register I allows for the selective power down of the ADC signal channel or the DAC signal channel through SPI control. The wake-up time, after powering down the device is typically 200µs. The maximum standby current is 96µA, depending highly upon the Master clock (MCLK), see 5.3.5.2 Low Power Modes.

2.2.2 Hardware Power-Down

The device has no power-down pin. However, by holding down (0 V) the NRESET pin (resetting the device) as well as the pins MCLK, BCLK and FSYNC, the power consumption will reach the standby current of typically 16µA. Use the standard procedure for power up (see start-up and initialization procedure) after a hardware power down and apply your registers setup procedure.

3 SERIAL COMMUNICATIONS

3.1 SERIAL AUDIO INTERFACE

The Serial Audio Interface is a 4-wire interface for bi-directional communication of audio data. The 4 terminals are listed below:

- BCLK: Bit serial clock, one clock cycle corresponds to one data bit transmitted or received.
- FSYNC: Frame Synchronization. This signal indicates the start of a data word. The frequency of the FSYNC corresponds to the sample frequency of the CODEC.
- SDI: Serial Data In, data received from external device and sent to DAC.
- SDO: Serial Data Out, data received from ADC and sent to external device.

The same clock (BCLK) and synchronization (FSYNC) signals are used for both sending and receiving. The synchronization signal FSYNC must have a fixed ratio with the master clock signal MCLK.

The Serial Audio Interface supports two formats that are commonly used for audio/voice CODECs and that are referred to as SFS (Short Frame Synchronization) and LFS (Long Frame Synchronization). Data can be transmitted and received in 2 channels. Which channel is selected depends on the programmed values in the registers. The two interface protocols are shown below.

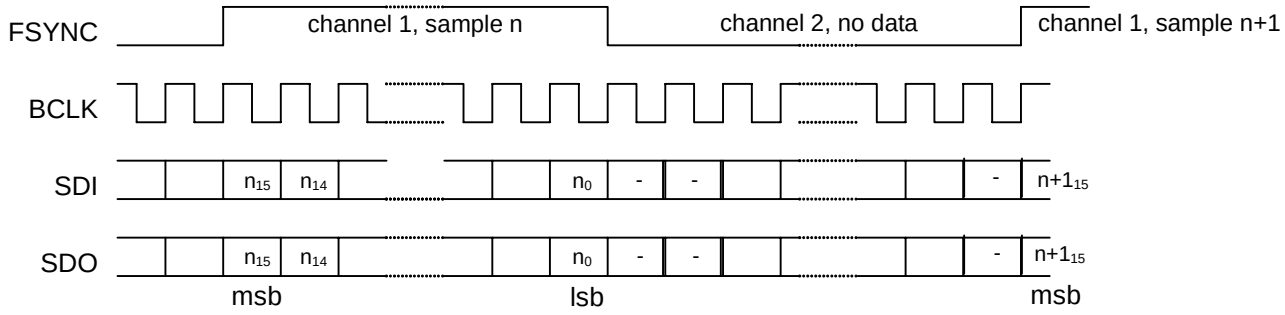


Figure 13: Audio interface timing LFS mode, channel 1

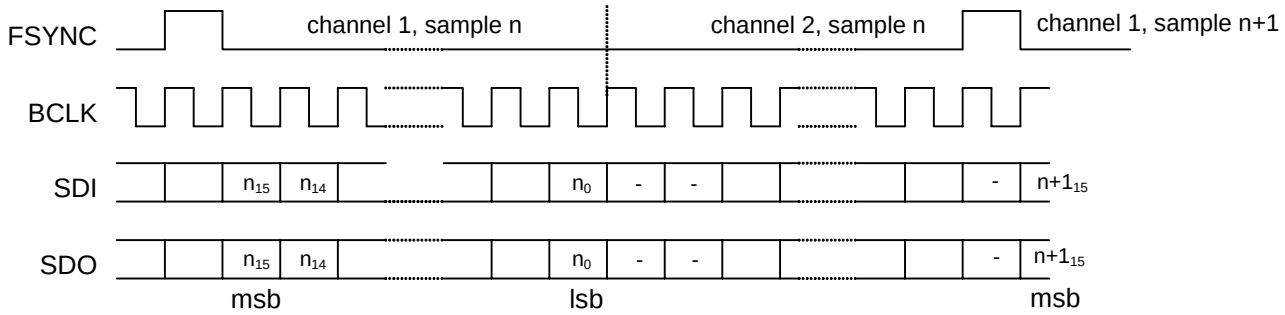


Figure 14: Audio interface timing in SFS mode, channel 1

SDI Data should be changed on the rising edge of BCLK. The SDI data will be read by the CODEC on the falling edge of BLCK. SDO data will change on the rising edge of the BCLK. The SDO data should be read on the falling edge of the BLCK. Each rising edge of the FSYNC indicates the start of a new sample.

3.1.1 LFS Optimization

For transmitting and receiving, 32 clock cycles in one frame are always required (figure 12 and 13). This is even the case when only 16 bits have to be sent or received. In most cases this can be handled easily with a DSP and microcontroller.

If the user wants to send a minimum of BLCK cycles, it is possible to shorten channel 1 (channel 2 can not be shortened).

In the LFS mode the possibility exists to shorten the number of BLCK cycles to 17 instead of 32. In this case the data is transmitted and received in channel 2. Channel 1 is shortened to one BLCK cycle only.

Note! This optimization is possible in slave mode only.

The figure 15 shows this special LFS mode.

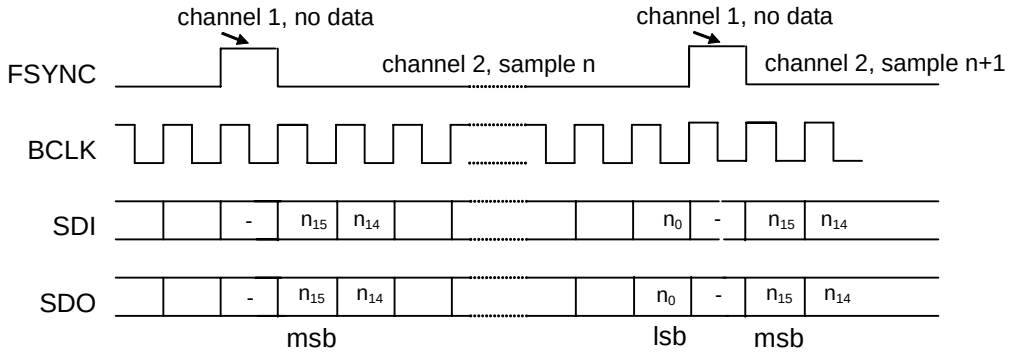


Figure 15: Audio interface timing in LFS mode, 17 BLCK cycles, channel 2

3.2 REGISTER PROGRAMMING

The control registers define the configuration of the CODEC and define the various modes of operation. During power-up, all registers will be configured with default values. The control register set consists of 16 registers. A detailed description is provided chapter 7.

The control registers can be changed in the two following ways:

1. Logic values at SPI pins during power-up

There are 3 bits inside the registers which are configured depending on the logic values of the pins SS, SCK and MOSI during the power up startup sequence as described in section 2.1.10

Value at power up	Influenced bits of registers	comments
SS = 1 SS = 0	Register I(0)=0 Register I(0)=1	MCLKDIV division by 1 MCLKDIV division by 2
SCK = 0 SCK = 1	Register J(0)=1 Register J(0)=0	SFS protocol LFS protocol
MOSI = 0 MOSI = 1	Register E(2) = 0 Register E(2) = 1	preamplifier gain x5 preamplifier gain x20

Using the SPI pins at startup the user is able to configure the CODEC in the corresponding setups without reprogramming through the SPI interface and protocol. In best case the SPI interface can then be completely omitted and the 3 SPI pins can be fixed to '0' or '1'.

2. Programming through SPI interface after power-up

Once the device has been powered up, the configuration registers can be modified at all times (also when the device is active) through the SPI interface.

The following section describes the SPI protocol which is required to change the control registers from their default values.

3.3 SERIAL PERIPHERAL INTERFACE - SPI

The serial peripheral interface (SPI) allows the device to communicate synchronously with other devices such as a microprocessor or a DSP. The CODEC interface only implements a slave controller. This section describes the communication from master (e.g. DSP) to slave (CODEC pin MOSI) and from slave (CODEC pin MISO) to a master (e.g. DSP).

Four lines are used to transmit data between the slave and master:
- MOSI (Master Out, Slave In) data from master to slave, synchronous with the SPI clock (SCK).
- MISO (Master In, Slave Out) data from slave to master, synchronous with the SPI clock (SCK).
- SCK (Serial Clock) synchronizes the data bits of MOSI and MISO.
- SS (Slave Select) Slave devices are selected by activating SS.

3.3.1 Protocol

During SPI communication, data is simultaneously transmitted and received.

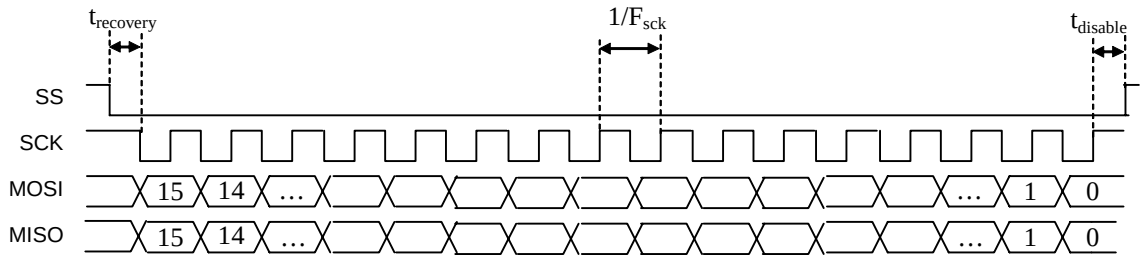


Figure 16: SPI signal timing

The master puts data on the MOSI line on the falling edge of SCK; the slave reads the data on the rising edge of SCK. The slave puts data on the MISO line on the falling edge of SCK; the master reads the data on the rising edge of SCK. Transmission in either direction is by 2 bytes with MSB first.

The SS pin should be kept low during the whole transfer of data.

There are three timing constraints:

- Recovery time ($t_{recovery}$) between the falling edge of SS and the falling edge of SCK.

- Disable time ($t_{disable}$) between the last rising edge of SCK and the rising edge of SS.
- SCK frequency (F_{SCK})

Delay	Min	Max	Unit	Comments
$t_{recover}$	125	-	ns	
$t_{disable}$	2 x T_{master}	-	ns	T_{master} = clock period of the master clock MCLK
F_{SCK}		0.5 x F_{master}	Hz	F_{master} = frequency of the master clock MCLK

3.3.2 SPI Interface Modes

There are two SPI modes: read and write.

3.3.2.1 Read Mode

Read communication always takes place in pairs of bytes. A read request of 2 bytes is sent on the MOSI line. The content of the addressed register, one byte, is dumped on the MISO line during the transmission of the second byte on the MOSI. The formats of one byte are the following:

bit	7	6	5	4	3	2	1	0
mosi	1	1	0	msb		A (4:0)		lsb

bit	7	6	5	4	3	2	1	0
miso	msb			D(7:0)				lsb

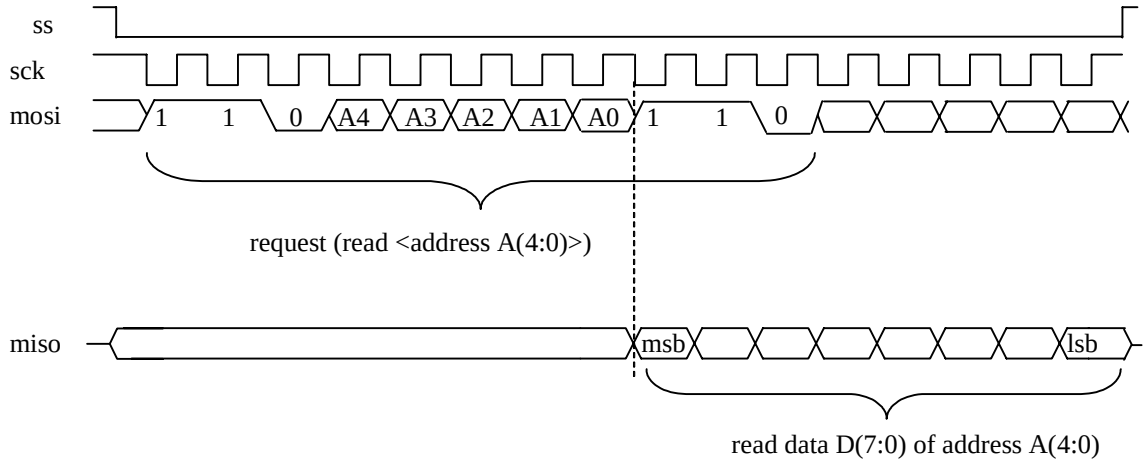


Figure 17: SPI signal timing in read mode

3.3.2.2 Write Mode

Write communication always takes place in pairs of bytes. The format of the 2 bytes is:

Bit	7	6	5	4	3	2	1	0
mosi	1	0	0	msb		A(4:0)		lsb

Bit	7	6	5	4	3	2	1	0
mosi	msb			D(7:0)				lsb

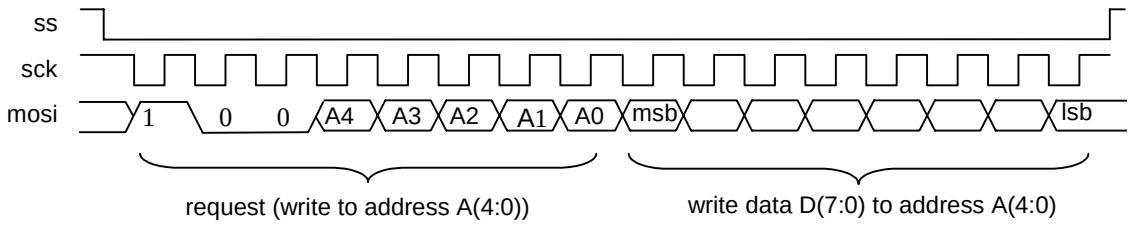


Figure 18: SPI signal timing in write mode

4 SANDMAN™ FUNCTION (XE3006)

The Sandman™ function analyzes the audio signals in the ADC and DAC. Its output signals indicate whether an audio signal is present in the ADC or DAC or if the processed signal is just noise. The threshold or reference value between noise and audio signal as well as the minimum duration of an audio signal is user-programmable through the SPI interface. If the XE3006 CODEC is used in a system that includes a microcontroller, a DSP or an RF link, the outputs of the Sandman™ Interface can be used to bring these devices into standby or sleep mode whenever no audio signal is being processed. In this way, the Sandman™ function contributes to significant additional power savings on the system level outside the XE3006 chip.

The Sandman™ Interface consists of 2 digital outputs:

- The SMAD detects whether the ADC processes an audio signal. The calculation is made with the digital data leaving the ADC.
- The SMDA detects whether an audio signal is processed by the DAC. The calculation is made with the digital data entering through the Audio Interface.

The Sandman™ Interface is implemented for the ADC and for the DAC in an identical way. It works with a set of 4 user-defined parameters: off time, on-time, ADC-reference and DAC-reference. The on time and the off time are the same for ADC and DAC. However, the reference values for the ADC and the DAC are adjusted separately, as indicated in the table below.

Input parameters	Register	Sandman ADC	Sandman DAC
Off-time1(7:0)	L	X	X
Off-time2(15:8)	M	X	X
On-time(7:0)	N	X	X
ADC_reference(7:0)	O	X	-
DAC_reference(7:0)	P	-	X

The Sandman™ Interface (for the ADC as well as for the DAC) is configured with three parameters:

- **Reference (7:0):** Absolute value under which the signal is considered noise and above which the signal is considered to be an audio signal. The Sandman™ function is disabled (SMAD or SMDA at logic 1) if this parameter is zero. The ADC and the DAC have separate Reference values.

- **Off-time (15:0):** Time until power down. The number of sequential samples that have to be lower than the Reference for the power down signal to become active. The Sandman™ function is disabled (SMAD or SMDA at logic 1) if this parameter is zero. The ADC and DAC have one common Off-time value.

- **On-time (7:0):** Time until wakeup. The number of sequential samples that have to be higher than the Reference for the power down signal to become inactive. The Sandman™ function is disabled (SMAD or SMDA at logic 1) if this parameter is zero. The ADC and DAC have one common On-time value.

All these parameters are set in the registers L, M, N, O and P.

Reference(7:0)	On-time(7:0)	Off-time(15:0)	Sandman (SMAD or SMDA)	Comments
0	don't care	don't care	logic 1 (disable function)	Sandman disable
don't care	0	don't care	logic 1 (disable function)	Sandman disable
don't care	don't care	0	logic 1 (disable function)	Sandman disable
1.-.255 corresponds to 128.-.32640	1.-.255 corresponds to 50 μs – 12 ms	1 - 65535 corresponds to 50 μs - 3.2 sec	logic 1 (signal higher than ref) logic 0 (signal lower than ref)	all registers ≠ zero time for FSYNC = 20kHz

The reference (7:0) value is related to the absolute value of the 16 bits input signal. The following format is used for the comparison:

- 16 bit inputs data (2's-complement) : 0**111'1111'1**111'1111 = 0x7FFF max positive value
- 8 bit reference (unsigned) : 0**111'1111'1**000'0000 = 0xFF00/2 reference max

So the reference is compared to the 8 most significant bits of the absolute value of the input signal:

reference(7:0)	Absolute reference	AIN (mV) if gain = 4	AIN (mV) if gain = 20
0	0	0.00	0.00
1	128	1.10	0.27
2	256	2.20	0.55
⋮	⋮	⋮	⋮
255	255 × 128 = 32640	280	70

The values in this table are amplitude values, RMS values can be derived by dividing the numbers by √2.

The working mechanism of the Sandman™ function is the following:
The incoming data is compared to the reference after each time step (1/FSYNC = 50μs if FSYNC = 20kHz).

- **During the On-time phase**
  If the input data is higher than the reference, a counter will be incremented otherwise the counter is reset.
  When the counter reaches the On-time value, then the SMAD or SMDA signal is activated (high level).

- **During the Off-time phase**
  If the input data is lower than the reference, a counter will be incremented otherwise the counter is reset.
  When the counter reaches the Off-time value, then the SMAD or SMDA signal is deactivated (low level).

In a first approximation, the following points are recommended:

- **On-time at least 1ms**. If the On-time is shorter than 1 ms, the Sandman™ function becomes sensitive to spikes in the audio input signal AIN.

- **Off-time at least 10ms,** the Off-time should be longer than $1/f_{min}$ = 10ms, (code = 200). f_{min} is the minimum audio frequency = 100Hz if FSYNC = 20kHz. The value of f_{min} scales proportionally with the sampling frequency FSYNC. A high-pass filter in the ADC filters out signals below 100Hz.

- Reference should be adjusted just above the noise level.

The CODEC bandwidth is around 100 Hz to 10 kHz at the nominal system frequency settings (MCLK = 5 MHz, CKDIV = 1, FSYNC = 20 kHz).

In digital loop back mode, the data entering into the Audio Interface is not transferred to the DAC. However, the Sandman™ function (if activated) continues to output the SMDA signal based on the data entered into the Audio Interface (input terminal SDI).

5 SPECIFICATIONS

5.1 ABSOLUTE MAXIMUM RATINGS

Stresses above those listed in the following table may cause permanent failure. Exposure to absolute ratings for extended periods may affect device reliability.

The values are in accordance with the Absolute Maximum Rating System (IEC 134).
All voltages are referenced to ground (VSSA and VSSD).
Analog and digital grounds are equal (VSSA = VSSD).

Symbol	Parameter	Conditions	Min	Max	Unit
VDD	Supply voltage		-0.3	3.65	V
Tstg	Storage temperature		-65	150	°C
TA	Operating free-air temperature, TA		-20	70	°C
Ves	Electrostatic discharge protection	1)		500	V
Ilus	Static latchup current	2)	10	98	mA
Vlud	Dynamic latchup voltage	2)		50	V

1) Tested according MIL883C Method 3015.6, class JEDEC 1B (Standardized Human Body Model: 100 pF, 1500 Ω, 3 pulses, protection related to substrate).
2) Static and dynamic latchup values are valid at 27 °C.

5.2 RECOMMENDED OPERATING CONDITIONS

All voltages referenced to ground (VSSA and VSSD).

	Min	Typ	Max	Unit
Supply voltage, VDD	1.8	3.0	3.6	V
Analog signal peak input voltage, AIN (gain = 20x)			65	mV
Analog signal peak input voltage, AIN (gain = 5x)			270	mV
Differential output load resistance	16	32		Ohm
Master clock frequency	1.024		33	MHz
ADC or DAC conversion rate		20	48	kHz
Operating free-air temperature, TA	-20		70	°C

5.3 ELECTRICAL CHARACTERISTICS

The operating conditions in this section are: VDD = 3.0 V, T = 25°C.

5.3.1 Digital Inputs and Outputs, FSYNC = 20 kHz, output not loaded

	Parameter	Test Conditions	Min	Typ	Max	Unit
VOH	High-level output voltage, DOUT	IO = -360uA	2.4		VDD+0.5	V
VOL	Low-level output voltage, DOUT	IO = 2mA	VSSD-0.5		0.4	V
IIH	High-level input current, any digital input	VIH = 3.3 V			10	uA
IIL	Low-level input current, any digital input	VIL = 0.6 V			10	uA
Ci	Input capacitance				10	pF
Co	Output capacitance				10	pF

5.3.2 ADC Dynamic Performance, FSYNC = 20 kHz

	Parameter	Test Conditions	Min	Typ	Max	Unit
SNR	Signal-to-noise ratio	Pre-amp gain = 5x Vin=250mV (full scale)	72	78		dB
THD	Total harmonic distortion	¼ full scale		0.5		%
Flo	Low cut-off frequency (-3 dB), See Note 1	FSYNC = 20 kHz	60	70	80	Hz
Fhi	High cut-off frequency (-3 dB), See Note 2	FSYNC = 20 kHz		10		kHz
GD	Group delay	FSYNC = 20 kHz			150	us

Note 1) Flo is proportional to FSYNC
Note 2) Fhi equals FSYNC/2

5.3.3 ADC Channel Characteristics, FSYNC = 20 kHz

	Parameter	Test Conditions	Min	Typ	Max	Unit
Vip	Peak input voltage (single ended)	Pre-amp gain = 5x			270	mV
		Pre-amp gain = 20x			65	
Vneq	Equivalent input noise	A-weighted, 100 Hz-10 kHz pre-amp gain = 5x			20	µV rms
		A-weighted, 100 Hz-10 kHz pre-amp gain = 20x			5	
	Dynamic range	Pre-amp gain = 5x Vin=250mV (full scale)	72	78		dB
PSRR	Power supply rejection ratio, input referred	Up to 1 kHz		60		dB
Cin	Input capacitor	Preamp-gain = 5x		50		pF
		Preamp gain = 20x		200		
Rin	Input resistance VIN – VSSA		1			MOhm
Eg	gain error	VDD 1.8-3.3V		+/- 0.1		[%]
	offset error	VDD 1.8-3.3V		-60		LSB
	input noise	VDD 1.8-3.3V		6.7		LSB
INL	Integral non linearity	VDD 1.8-3.3V		+/- 5		LSB
DNL	Differential non linearity	VDD 1.8-3.3V		+/- 0.1		LSB

5.3.4 DAC Dynamic Performance, load is an LC filter at 10 kHz

FSYNC = 20 kHz, MCLK = 5 MHz, for info on the LC filter see chapter 6, Application Information.

	Parameter	Test Conditions	Min	Typ	Max	Unit
SNR	Signal-to-noise ratio	Bandwidth 10 kHz	72	78		dB
THD	Total harmonic distortion	¼ full scale		0.5		%
	Dynamic range	Bandwidth 10 kHz	72	78		dB
GD	Group delay	FSYNC = 20 kHz			150	µs

5.3.5 Power Supply

5.3.5.1 Regulated supply characteristics @ T = 25°C

	Parameter	Test Conditions	Min	Typ	Max	Unit
VREF	reference Voltage	1µF capacitor 390 kΩ resistor		1.2		V
VREG11	regulated Voltage 1.1V			1.1		V
I_vreg11	available current			35	50	µA
R_vreg11	output impedance			1	1.5	kOhm
VREG16	regulated Voltage 1.6V	1µF capacitor	1.5	1.6		V
I_vreg16	available output current				1	mA
VREF PSRR	power supply rejection ratio, input referred	up to 1 kHz		60		dB
VREG11 PSRR	power supply rejection ratio, input referred	up to 1 kHz		60		dB
VREG16 PSRR	power supply rejection ratio, input referred	up to 1 kHz		40		dB

5.3.5.2 Low power mode

Stand-by mode @ VDD = 3.0V, T = 25°C

	Parameter	Test Conditions	Min	Typ	Max	Unit
Istb1	Supply current in standby mode	ADC off, DAC off MCLK = 5 MHz,		28	56	µA
Istb2	Supply current in standby mode	ADC off, DAC off MCLK = 12.2880 MHz		48	96	µA
Istb3	Supply current in standby mode	NRESET mode MCLK = 0		20	40	µA

Stand-by mode @ VDD = 1.8V, T = 25°C

	Parameter	Test Conditions	Min	Typ	Max	Unit
Istb1	Supply current in standby mode	ADC off, DAC off MCLK = 5 MHz,		25	50	µA
Istb2	Supply current in standby mode	ADC off, DAC off MCLK = 12.2880 MHz		31	62	µA
Istb3	Supply current in standby mode	NRESET mode MCLK = 0		16	32	µA

5.3.5.3 Normal operation, output load consumption is not included.

Normal operations @ VDD = 3.0V, FSYNC = 20 kHz, T = 25°C, Register C(7:0) = 0xF0

	Parameter	Test Conditions	Min	Typ	Max	Unit
IDD	Supply current CODEC	ADC on, DAC on FSYNC = 20 kHz, no load		350	700	µA
IADC	Supply current ADC	ADC on, DAC off FSYNC = 20 kHz, no load		240	480	µA
IDAC	Supply current DAC	ADC off, DAC on FSYNC = 20 kHz, no load		120	240	µA

Normal operations @ VDD = 3.0V, FSYNC = 48 kHz, T = 25°C, Register C(7:0) = 0xC4

	Parameter	Test Conditions	Min	Typ	Max	Unit
IDD	Supply current CODEC	ADC on, DAC on FSYNC = 48 kHz, no load		860	1720	µA
IADC	Supply current ADC	ADC on, DAC off FSYNC = 48 kHz, no load		600	1200	µA
IDAC	Supply current DAC	ADC off, DAC on FSYNC = 48 kHz, no load		280	560	µA

Normal operations @ VDD = 1.8V, FSYNC = 20 kHz, T = 25°C, Register C(7:0) = 0xF0

	Parameter	Test Conditions	Min	Typ	Max	Unit
IDD	Supply current CODEC	ADC on, DAC on FSYNC = 20 kHz, no load		250	500	µA
IADC	Supply current ADC	ADC on, DAC off FSYNC = 20 kHz, no load		200	400	µA
IDAC	Supply current DAC	ADC off, DAC on FSYNC = 20 kHz, no load		65	130	µA

Normal operations @ VDD = 1.8V, FSYNC = 48 kHz, T = 25°C, Register C(7:0) = 0xC4

	Parameter	Test Conditions	Min	Typ	Max	Unit
IDD	Supply current CODEC	ADC on, DAC on FSYNC = 48 kHz, no load		625	1250	µA
IADC	Supply current ADC	ADC on, DAC off FSYNC = 48 kHz, no load		505	1010	µA
IDAC	Supply current DAC	ADC off, DAC on FSYNC = 48 kHz, no load		140	280	µA

5.3.6 Timing Requirements of serial audio interface

Ref. No. *	Characteristics	Test Conditions	Min	Typ	Max	Unit
1	Master Clock Frequency for MCLK = 1/ T		1024	5.12	33	MHz
1	MCLK Duty Cycle		45		55	%
2	Rise Time for All Digital Signals				10	ns
3	Fall Time for All Digital Signals				10	ns
4	Hold time BCLK or FSYNC high after MCLK low		T/4			ns
5	Setup time BCLK or FSYNC high to MCLK low		T/4			ns
6	Hold time BCLK or FSYNC low after MCLK low	C_{Load} = 10pF	T/4			ns
7	Setup time BCLK or FSYNC low to MCLK low		T/4			ns
8	Bit Clock Frequency for BCLK = 1 / T_{BCLK}			32xFSYNC	MCLK/2	MHz
9	Setup time data input SDI to BCLK low		T_{BCLK}/4			ns
10	Hold time data input SDI after BCLK low		T_{BCLK}/4			ns
11	Delay time SDO valid after BCLK high				T_{BCLK}/4	ns
12	Setup time data input FSYNC to BCLK low		T_{BCLK}/4			ns
13	Hold time data input FSYNC after BCLK low		T_{BCLK}/4			ns

*****see figure 18,19 for LFS and 20, 21 for SFS

5.3.6.1 Timing diagram of the serial audio interface – LFS mode

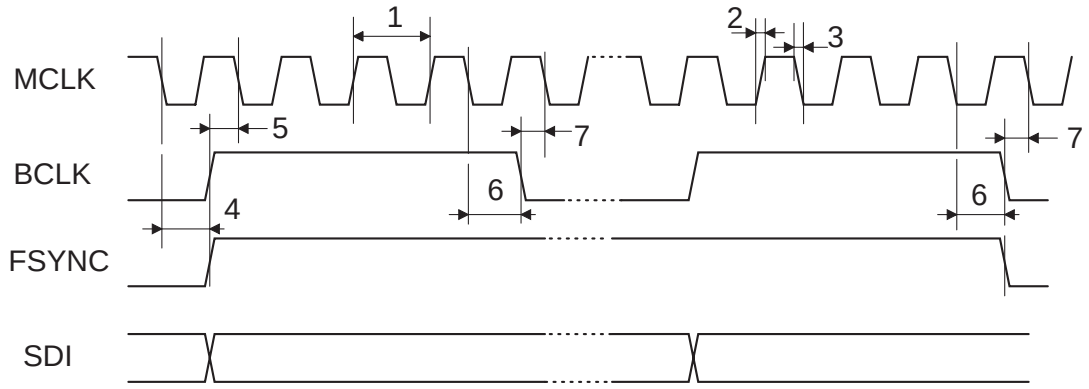


Figure 18: LFS, timing diagram

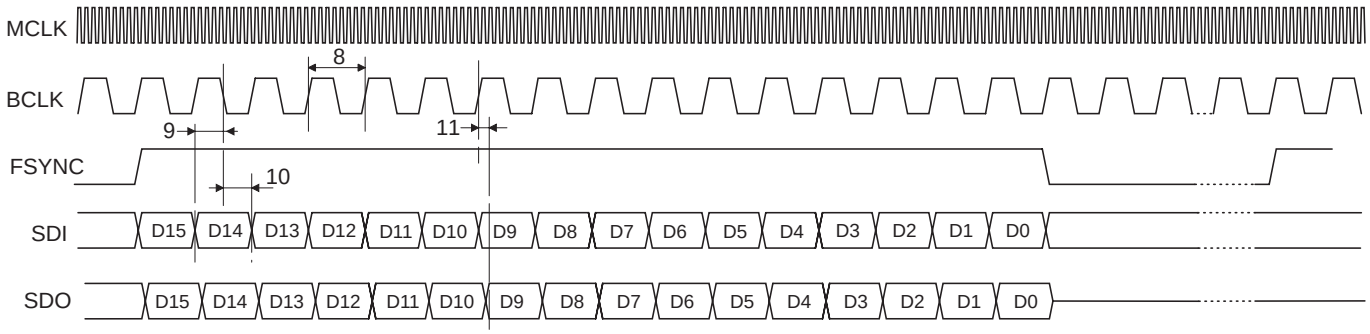


Figure 19: LFS, zoom timing diagram

5.3.6.2 Timing diagram of the serial audio interface – SFS mode

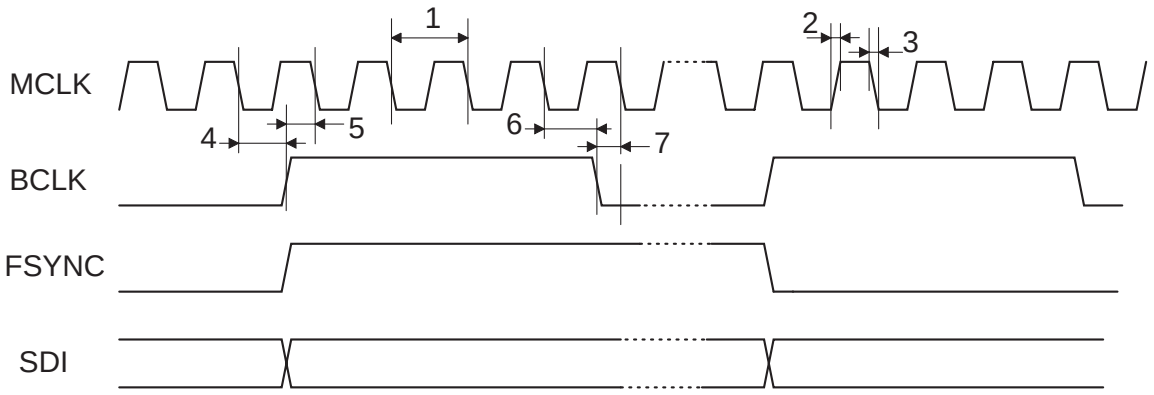


Figure 20: SFS, timing diagram

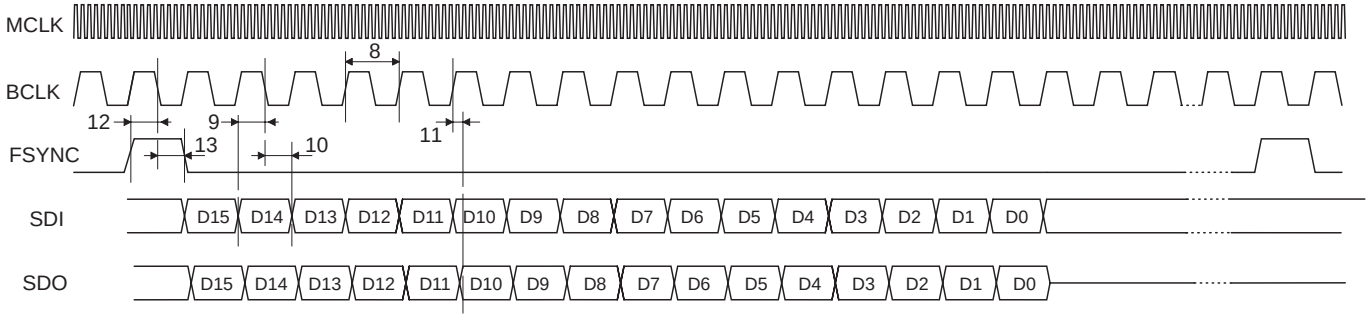


Figure 21: SFS zoom timing diagram

5.3.7 Timing Requirements of the Serial Peripheral Interface

Ref. No.*	Characteristics	Test Conditions	Min	Typ	Max	Unit
1	Serial Clock Frequency for SCK = 1 / TSCK				MCLK/2	MHz
1	MCLK Duty Cycle		45		55	%
2	Recovery Time		125			ns
3	Disable Time	C_{Load} = 10pF	2T			ns
4	Setup time MISO valid to SCK high		TSCK/4			ns
5	Hold time MISO valid after SCK high		TSCK/4			ns
6	Delay time MOSI valid after SCK low		TSCK/4			ns

* see figure 22

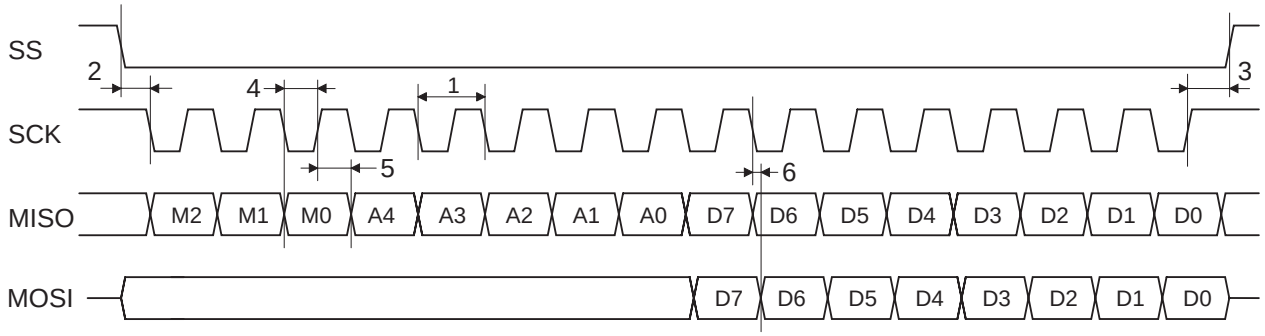


Figure 22: Serial Peripheral Interface timing

6 APPLICATION INFORMATION

6.1 APPLICATION SCHEMATICS – XE3006

6.1.1 Typical Application schematic

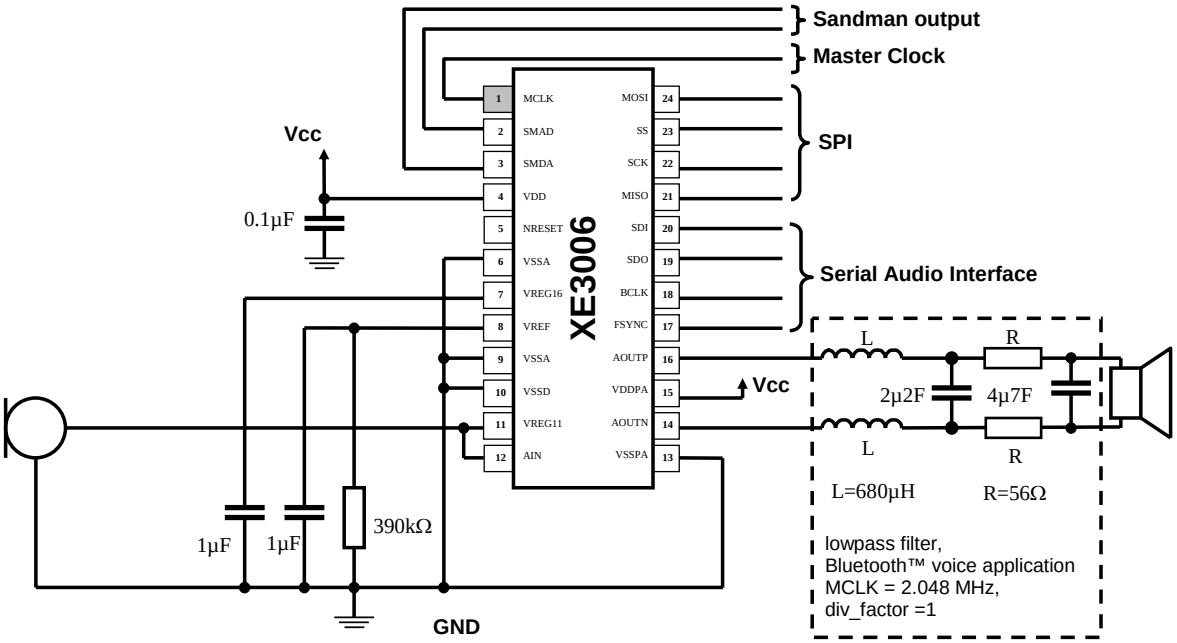


Figure 23: Typical Application with 3rd order LC output Filter

6.1.2 External components required for optimal performances

The following minimum set-up of external components is required:

- Capacitor for Vref: 1 µF
- Resistor for Vref: 390 kΩ
- Capacitor for VREG16: 1 µF

The low pass filter between the DAC output and the speaker depends on the CODEC settings and the speaker type.

7 REGISTER DESCRIPTION

7.1 REGISTER FUNCTIONAL SUMMARY

The following registers can be programmed by the SPI to configure the operation modes. See also section 3.2 Register Programming.

Name	Description
Register C	ADC current setting. The data in this register has the following functions:
	• Adjust the ADC current for FSYNC > 20kHz
	• 0xF0 for FSYNC<= 20 kHz, 0xC4 for FSYNC > 20 kHz.
Register E	Analog Input. The data in this register has the following functions:
	• Enable/disable microphone bias source of 1.1 V
	• Gain setting of pre-amplifier.
Register I	Function enable and clock division. The data in this register has the following functions:
	• Enable/disable Sandman function of DAC
	• Enable/disable DAC channel (DAC, power amplifier)
	• Enable/disable ADC channel (pre-amplifier, ADC, decimation filter)
	• Division of master clock
Register J	Audio Interface Configuration. The data in this register has the following functions:
	• Enable/disable digital loopback
	• Channel select receive
	• Select master / slave mode
	• Output impedance
	• Channel select transmit
	• Select short / long frame sync
Register L	Sandman™ function, Off-time, low byte. The data in this register has the following function:
	• Define Off-time (low byte) of the Sandman™ function
Register M	Sandman™ function, Off-time, high byte. The data in this register has the following function:
	• Define Off-time (high byte) of the Sandman™ function
Register N	Sandman™ function, On-time. The data in this register has the following function:
	• Define On-time of the Sandman™ function
Register O	Sandman™ function, reference for ADC. The data in this register has the following function:
	• Define reference amplitude for ADC for Sandman™ function
Register P	Sandman™ function, reference for DAC. The data in this register has the following function:
	• Define reference amplitude for DAC for Sandman™ function

7.2 REGISTER DEFINITIONS

The complete register setup consists of 24 registers of 8 bits each, as shown in the table below. All registers are preconfigured with the default values and do not have to be programmed by the user if no changes in the setup are required.
The registers C, E, I and J can be used to configure the XE3005 and XE3006 differently than the default setup.

The registers L, M, N, O and P are related to the Sandman™ function available in the XE3006.

Register	Address (hex)	Name	Default value (hex)
A	0x00	Reserved	0x48
B	0x01	Reserved	0x8F
C	0x02	ADC current	0xF0
D	0x03	Reserved	0x00
E	0x04	Analog input	0x08/0x0C
F	0x05	Reserved	0x82
G	0x06	Reserved	0x00
H	0x07	Reserved	0x00
I	0x08	Block on/off and clock division	0x00/0x01
J	0x09	Audio interface configuration	0x25/0x24
K	0x0A	Reserved	0x00
L	0x0B	Sandman™ function, off-time byte 1	0x00
M	0x0C	Sandman™ function, off-time byte 2	0x00
N	0x0D	Sandman™ function, on-time	0x00
O	0x0E	Sandman™ function, reference for ADC	0x00
P	0x0F	Sandman™ function, reference for DAC	0x00

Register C (7:0) address 0x02	ADC current	Default value: 0xF0	Description
7:0	ADC current	0xF0	0xF0 for FSYNC<= 20 kHz, 0xC4 for FSYNC > 20 kHz.

Register E (7:0) address 0x04	ADC input	Default value 0x08/0x0C	Description
7	VMIC_EN	0	Generation of the microphone supply at pin VREG11: 1: enables VREG11 0: disables VREG11
6:3	reserved	0001	reserved
2	PREAMP_ GAIN	0 or 1	Gain of preamplifier: 0: 5x (270 mV peak) 1: 20x (65 mV peak) The default is depending on the logic value of the pin MOSI during startup (see section 3.2) MOSI=0, default will be set to 0 MOSI=1, default will be set to 1
1:0	reserved	00	reserved

Register I (7:0) address 0x08	block on/off and clock division	Default value 0x00/0x01	Description
7:4		0000	reserved
3	EN_DAC	0	0: enable 1: disable DA converter (DAC + PA)
2	EN_ADC	0	0: enable 1: disable AD converter (Preamp + ADC + decimator)
1:0	MCLKDIV	00 or 01	Division factor of the master clock: 00: 1 01: 2 10: reserved 11: 4 The default is depending on the logic value of the pin SS during startup (see Section 3.2) SS=0, default will be set to 1 SS=1, default will be set to 0

Register J (7:0) address 0x09	Audio interface configuration	Default value 0x25/ 0x24	Description
7	LOOPBACK	0	0: disable loopback, normal mode 1: enable loopback => The CODEC connects internally the ADC output to DAC input
6	RX_FIRST_ SECOND	0	0: Receive audio data in the first 16-bit channel after the frame synchronization. 1: Receive audio data in the second 16-bit channel after the frame synchronization.
5	reserved	1	reserved
4	MASTER	0	1: enable audio interface in master mode (only for LFS) 0: enable audio interface in slave mode (LFS, LFS Optimization or SFS)
3	SDO_HI_EN	0	0: SDO is continuously in output mode for both data channels. 1: SDO is in output mode when transmitting a channel with data (J(2) or J(1)=1). It is switched automatically into high-impedance state when a channel with no data is transmitted (J(2) or J(1)=0).
2	TX_FIRST	1	1: transmit the audio data in the first 16-bit channel after the frame synchronization. 0: do no transmit data in the first channel.
1	TX_SECOND	0	1: transmit the audio data in the second 16-bit channel after the frame synchronization. 0: do no transmit data in the second channel.
0	PROTOCOL	0 or 1	1: Short Frame Synchronization mode (slave mode). 0: Long Frame Synchronization mode (master or slave mode). The default is depending on the logic value of the pin SCK during startup (see Section 3.2) SCK=0, default will be set to 1 SCK=1, default will be set to 0

Register L (7:0) address 0x0B	Sandman™ function, off-time, least significant byte	Default value 0x00	Description
7:0	SM_OFF_LSB	00000000	Least significant byte of the off-time of the Sandman™ function

Register M (7:0) address 0x0C	Sandman™ function, off-time, most significant byte	Default value 0x00	Description
7:0	SM_OFF_MSB	00000000	Most significant byte of the off-time of the Sandman™ function

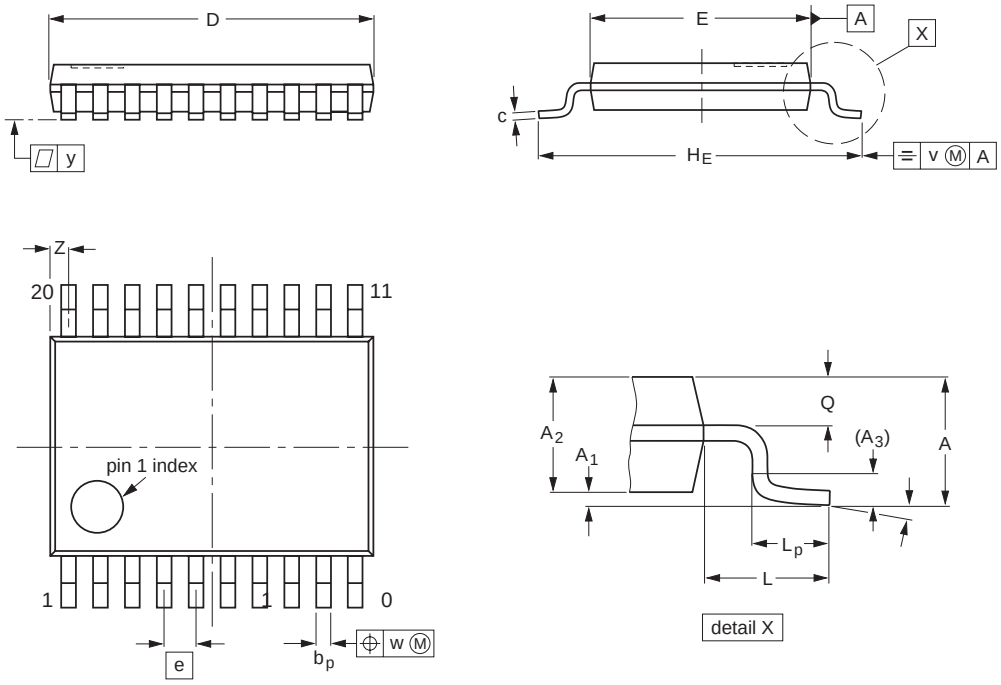
Register N (7:0) address 0x0D	Sandman™ function, on-time	Default value 0x00	Description
7:0	SM_ON	00000000	On-time of the Sandman™ function

Register O (7:0) address 0x0E	Sandman™ function, reference for ADC	Default value 0x00	Description
7:0	SMAD_REF	00000000	Reference amplitude for ADC for Sandman™ function

Register P (7:0) address 0x0F	Sandman™ function, reference for DAC	Default value 0x00	Description
7:0	SMDA _REF	00000000	Reference amplitude for DAC for Sandman™ function

8 MECHANICAL INFORMATION

8.1 XE3005 PACKAGE SIZE (TSSOP20)



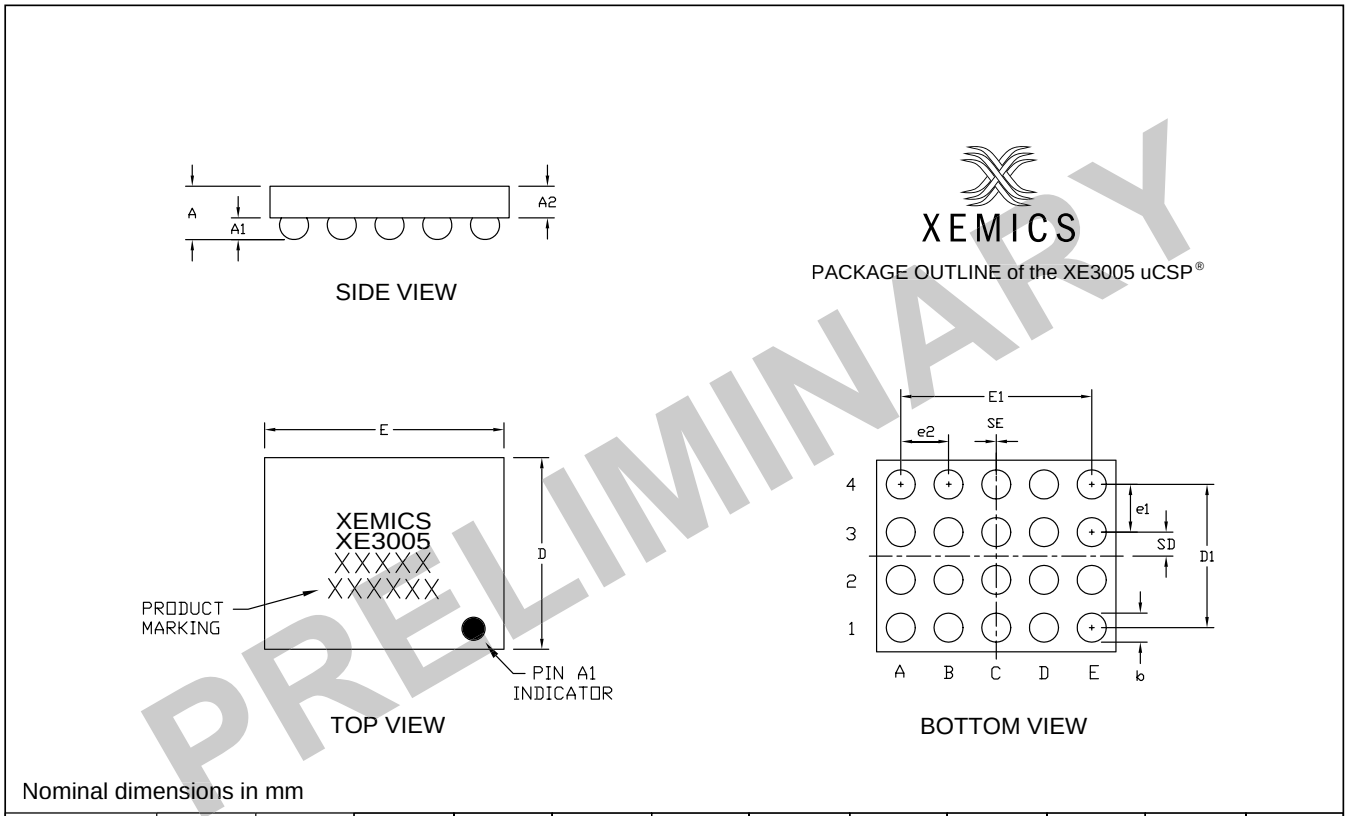
DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D	E	e	H_E	L	L_p	Q	v	w	y	Z	
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8^o 0^o

Figure 24: TSSOP20

Plastic Thin Shrink Small Outline Package, 20 leads, body width: 4.4 mm

8.2 XE3005 PACKAGE SIZE (5X4 UCSP®)



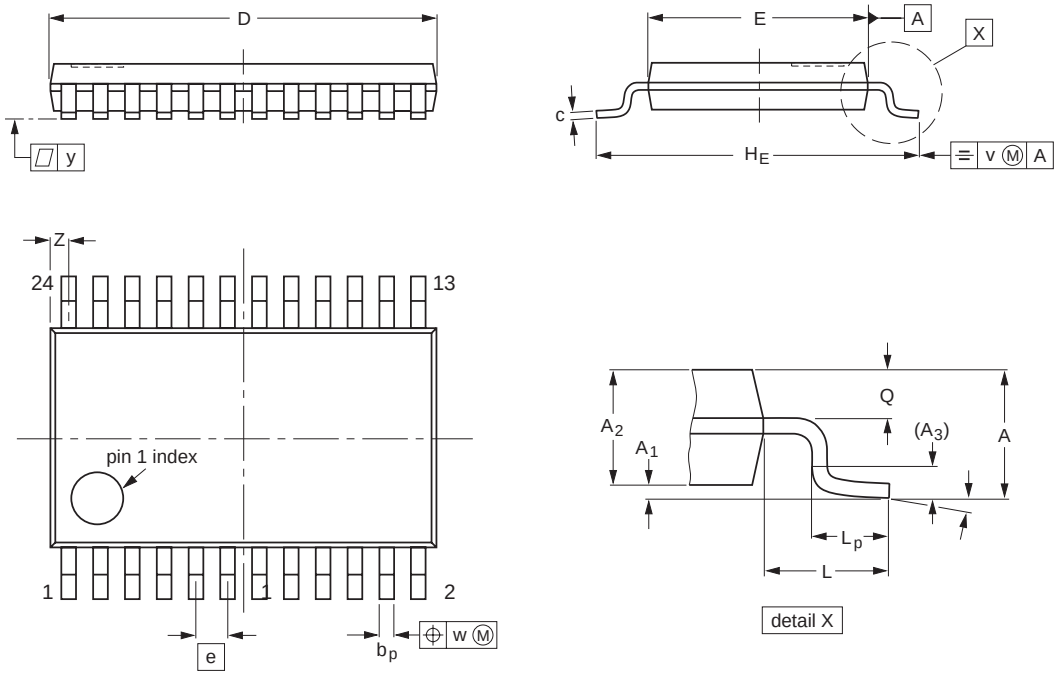
Nominal dimensions in mm

	A	A1	A2	b	D	D1	E	E1	e1	e2	SD	SE
	< 0.8	0.31	0.46 max	0.37	2.745 ± 0.075	1.95	3.225 ± 0.125	2.40	0.65	0.60	0.325 ± 0.075	0 ± 0.125

Figure 25: 5x4 uCSP®

Ultra Chip Scale Package, 5 x 4 balls array.

8.3 XE3006 PACKAGE SIZE (TSSOP24)



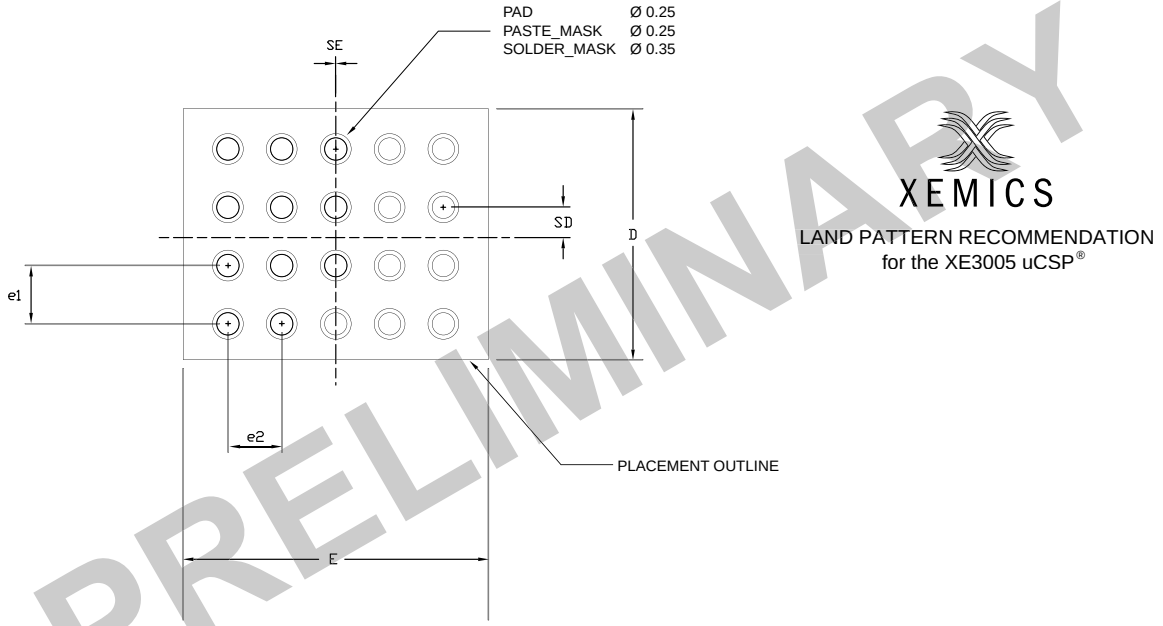
DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D	E	e	H_E	L	L_p	Q	v	w	y	Z	
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8^o 0^o

Figure 26: TSSOP24

Plastic Thin Shrink Small Outline Package with 24 leads and a body width of 4.4 mm.

9 XE3005 LAND PATTERN RECOMMENDATIONS (5X4 UCSP®)



Nominal dimensions in mm

	D	E	e1	e2	SD	SE						
	2.82	3.35	0.65	0.60	0.325	0						

Figure 27: Land pattern recommendations (5x4 uCSP®)

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