NCP1608

Critical Conduction Mode PFC Controller Utilizing a Transconductance Error Amplifier

The NCP1608 is an active power factor correction (PFC) controller specifically designed for use as a pre−converter in ac−dc adapters, electronic ballasts, and other medium power off−line converters (typically up to 350 W). It uses critical conduction mode (CrM) to ensure near unity power factor across a wide range of input voltages and output power. The NCP1608 minimizes the number of external components by integrating safety features, making it an excellent choice for designing robust PFC stages. It is available in a SOIC−8 package.

General Features

- Near Unity Power Factor
- No Input Voltage Sensing Requirement
- Latching PWM for Cycle−by−Cycle On Time Control (Voltage Mode)
- Wide Control Range for High Power Application (>150 W) Noise Immunity
- Transconductance Error Amplifier
- High Precision Voltage Reference (±1.6% Over the Temperature Range)
- Very Low Startup Current Consumption (≤ 35 μA)
- Low Typical Operating Current Consumption (2.1 mA)
- Source 500 mA/Sink 800 mA Totem Pole Gate Driver
- Undervoltage Lockout with Hysteresis
- Pin−to−Pin Compatible with Industry Standards
- This is a Pb−Free and Halide−Free Device

Safety Features

- Overvoltage Protection
- Undervoltage Protection
- Open/Floating Feedback Loop Protection
- Overcurrent Protection
- Accurate and Programmable On Time Limitation

Typical Applications

- Solid State Lighting
- Electronic Light Ballast
- AC Adapters, TVs, Monitors
- All Off−Line Appliances Requiring Power Factor Correction

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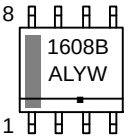
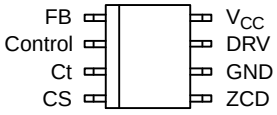
SOIC−8
D SUFFIX
CASE 751

MARKING DIAGRAM



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

PIN CONNECTION



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCP1608BDR2G	SOIC−8 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

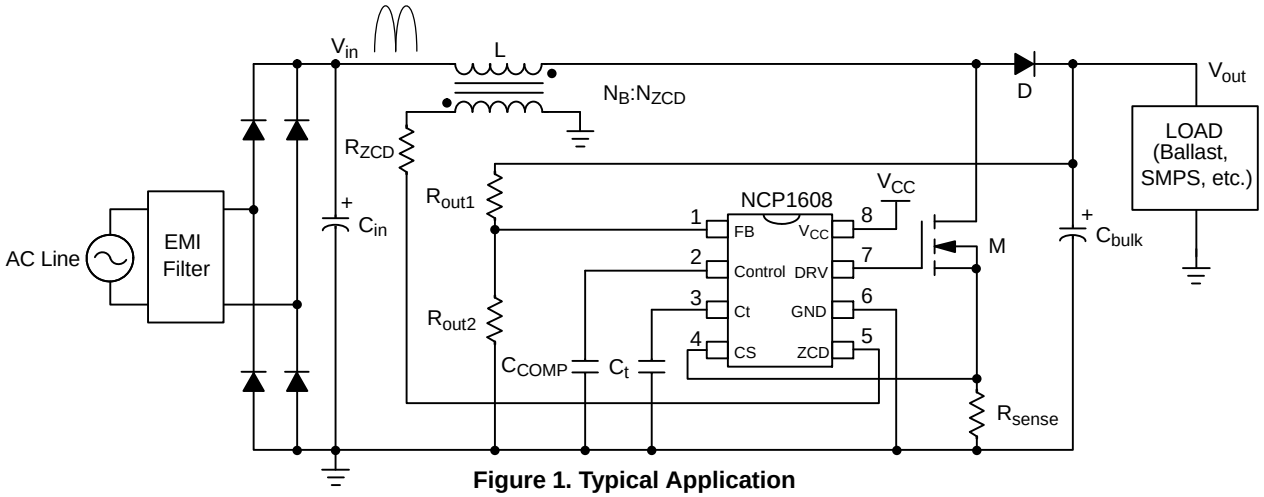


Figure 1. Typical Application

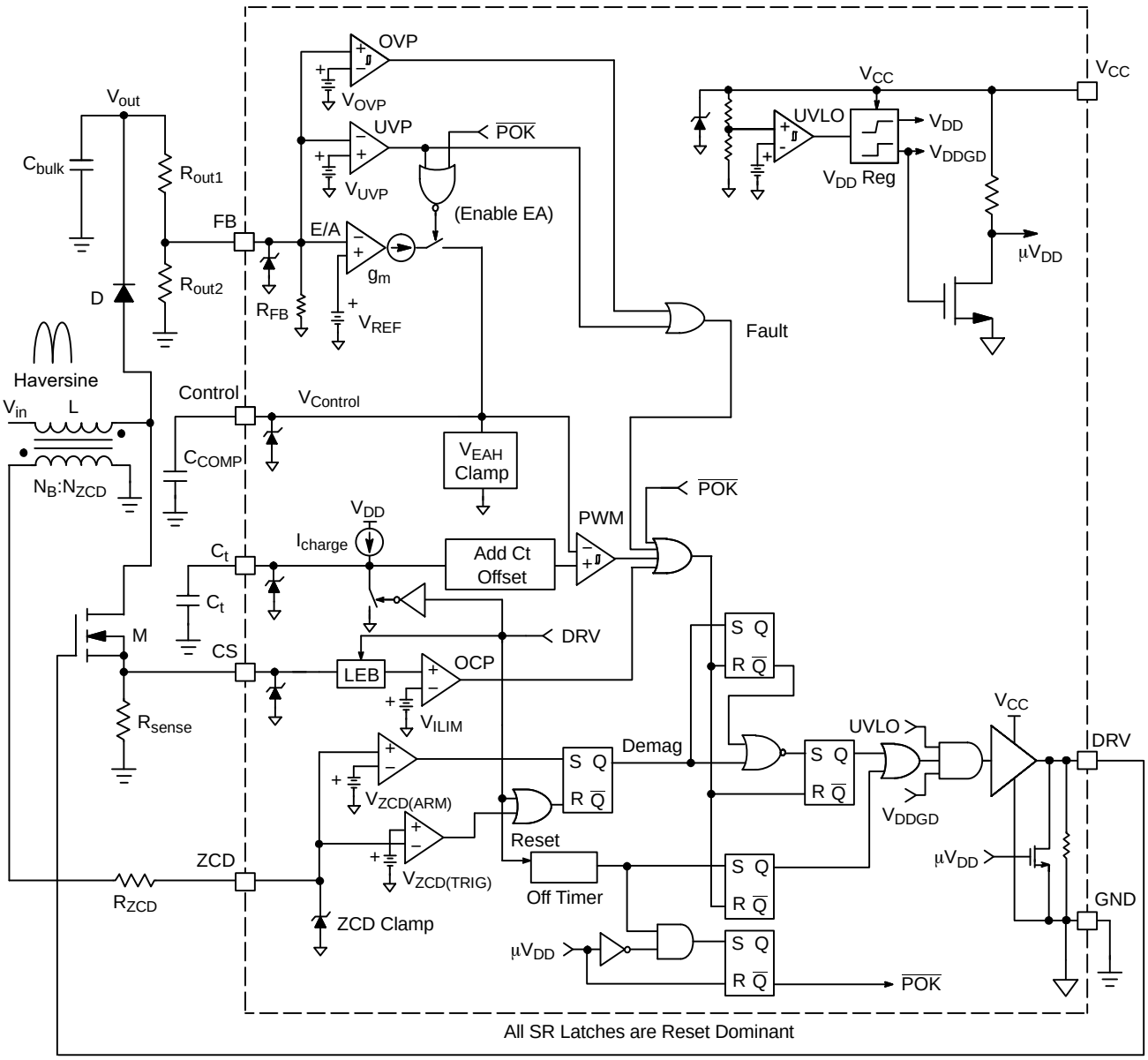


Figure 2. Block Diagram

Table 1. PIN FUNCTION DESCRIPTION

Pin	Name	Function
1	FB	The FB pin is the inverting input of the internal error amplifier. A resistor divider scales the output voltage to V_{REF} to maintain regulation. The feedback voltage is used for overvoltage and undervoltage protections. The controller is disabled when this pin is forced to a voltage less than V_{UVP}, a voltage greater than V_{OVP}, or floating.
2	Control	The Control pin is the output of the internal error amplifier. A compensation network is connected between the Control pin and ground to set the loop bandwidth. A low bandwidth yields a high power factor and a low Total Harmonic Distortion (THD).
3	Ct	The Ct pin sources a current to charge an external timing capacitor. The circuit controls the power switch on time by comparing the Ct voltage to an internal voltage derived from $V_{Control}$. The Ct pin discharges the external timing capacitor at the end of the on time.
4	CS	The CS pin limits the cycle−by−cycle current through the power switch. When the CS voltage exceeds V_{ILIM}, the drive turns off. The sense resistor that connects to the CS pin programs the maximum switch current.
5	ZCD	The voltage of an auxiliary winding is sensed by this pin to detect the inductor demagnetization for CrM operation.
6	GND	The GND pin is analog ground.
7	DRV	The integrated driver has a typical source impedance of 12 Ω and a typical sink impedance of 6 Ω.
8	V_{CC}	The V_{CC} pin is the positive supply of the controller. The controller is enabled when V_{CC} exceeds $V_{CC(on)}$ and is disabled when V_{CC} decreases to less than $V_{CC(off)}$.

Table 2. MAXIMUM RATINGS

Rating	Symbol	Value	Unit
FB Voltage	V_{FB}	−0.3 to 10	V
FB Current	I_{FB}	±10	mA
Control Voltage	$V_{Control}$	−0.3 to 6.5	V
Control Current	$I_{Control}$	−2 to 10	mA
Ct Voltage	V_{Ct}	−0.3 to 6	V
Ct Current	I_{Ct}	±10	mA
CS Voltage	V_{CS}	−0.3 to 6	V
CS Current	I_{CS}	±10	mA
ZCD Voltage	V_{ZCD}	−0.3 to 10	V
ZCD Current	I_{ZCD}	±10	mA
DRV Voltage	V_{DRV}	−0.3 to V_{CC}	V
DRV Sink Current	$I_{DRV(sink)}$	800	mA
DRV Source Current	$I_{DRV(source)}$	500	mA
Supply Voltage	V_{CC}	−0.3 to 20	V
Supply Current	I_{CC}	±20	mA
Power Dissipation (T_A = 70°C, 2.0 Oz Cu, 55 mm^2 Printed Circuit Copper Clad)	P_D	450	mW
Thermal Resistance Junction−to−Ambient (2.0 Oz Cu, 55 mm^2 Printed Circuit Copper Clad) Junction−to−Air, Low conductivity PCB (Note 3) Junction−to−Air, High conductivity PCB (Note 4)	 $R_{\theta JA}$ $R_{\theta JA}$ $R_{\theta JA}$	 178 168 127	°C/W
Operating Junction Temperature Range (Note 5)	T_J	−55 to +125	°C
Maximum Junction Temperature	$T_{J(MAX)}$	150	°C
Storage Temperature Range	T_{STG}	−65 to +150	°C
Lead Temperature (Soldering, 10 s)	T_L	300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device series contains ESD protection and exceeds the following tests:
   Pins 1 – 8: Human Body Model 2000 V per JEDEC Standard JESD22−A114E.
   Charged Device Model 1000 V per JEDEC Standard JESD22−C101E.
2. This device contains Latch−Up protection and exceeds ±100 mA per JEDEC Standard JESD78.
3. As mounted on a 40x40x1.5 mm FR4 substrate with a single layer of 80 mm^2 of 2 oz copper traces and heat spreading area. As specified for a JEDEC 51 low conductivity test PCB. Test conditions were under natural convection or zero air flow.
4. As mounted on a 40x40x1.5 mm FR4 substrate with a single layer of 650 mm^2 of 2 oz copper traces and heat spreading area. As specified for a JEDEC 51 high conductivity test PCB. Test conditions were under natural convection or zero air flow.
5. For coldest temperature, QA sampling at −40°C in production and −55°C specification is Guaranteed by Characterization.

Table 3. ELECTRICAL CHARACTERISTICS
V_{FB} = 2.4 V, $V_{Control}$ = 4 V, Ct = 1 nF, V_{CS} = 0 V, V_{ZCD} = 0 V, C_{DRV} = 1 nF, V_{CC} = 12 V, unless otherwise specified
(For typical values, T_J = 25°C. For min/max values, T_J = −55°C to 125°C (Note 6), V_{CC} = 12 V, unless otherwise specified)

Characteristic	Test Conditions	Symbol	Min	Typ	Max	Unit
STARTUP AND SUPPLY CIRCUITS						
Startup Voltage Threshold	V_{CC} Increasing	$V_{CC(on)}$	11	12	12.5	V
Minimum Operating Voltage	V_{CC} Decreasing	$V_{CC(off)}$	8.8	9.5	10.2	V
Supply Voltage Hysteresis		H_{UVLO}	2.2	2.5	2.8	V
Startup Current Consumption	0 V < V_{CC} < $V_{CC(on)}$ − 200 mV	$I_{cc(startup)}$	−	24	35	μA
No Load Switching Current Consumption	C_{DRV} = open, 70 kHz Switching, V_{CS} = 2 V	I_{cc1}	−	1.4	1.7	mA
Switching Current Consumption	70 kHz Switching, V_{CS} = 2 V	I_{cc2}	−	2.1	2.6	mA
Fault Condition Current Consumption	No Switching, V_{FB} = 0 V	$I_{cc(fault)}$	−	0.75	0.95	mA
OVERVOLTAGE AND UNDERVOLTAGE PROTECTION						
Overvoltage Detect Threshold	V_{FB} = Increasing	V_{OVP}/V_{REF}	105	106	108	%
Overvoltage Hysteresis		$V_{OVP(HYS)}$	20	60	100	mV
Overvoltage Detect Threshold Propagation Delay	V_{FB} = 2 V to 3 V ramp, dV/dt = 1 V/μs V_{FB} = V_{OVP} to V_{DRV} = 10% T_J = −40°C to +125°C T_J = −55°C to +125°C (Note 6)	t_{OVP}	 300 210	 500 500	 800 800	ns
Undervoltage Detect Threshold	V_{FB} = Decreasing	V_{UVP}	0.25	0.31	0.4	V
Undervoltage Detect Threshold Propagation Delay	V_{FB} = 1 V to 0 V ramp, dV/dt = 10 V/μs V_{FB} = V_{UVP} to V_{DRV} = 10% T_J = −40°C to +125°C T_J = −55°C to +125°C (Note 6)	t_{UVP}	 100 50	 200 200	 300 300	ns
ERROR AMPLIFIER						
Voltage Reference	T_J = 25°C T_J = −40°C to 125°C T_J = −55°C to 125°C (Note 6)	V_{REF}	2.475 2.460 2.450	2.500 2.500 2.500	2.525 2.540 2.540	V
Voltage Reference Line Regulation	$V_{CC(on)}$ + 200 mV < V_{CC} < 20 V	$V_{REF(line)}$	−10	−	10	mV
Error Amplifier Current Capability	V_{FB} = 2.6 V V_{FB} = 1.08*V_{REF} V_{FB} = 0.5 V T_J = −40°C to +125°C T_J = −55°C to +125°C (Note 6)	$I_{EA(sink)}$ $I_{EA(sink)OVP}$ $I_{EA(source)}$	6 10 −250 −250	10 20 −210 −210	20 30 −110 −88	μA
Transconductance	V_{FB} = 2.4 V to 2.6 V T_J = 25°C T_J = −40°C to 125°C T_J = −55°C to +125°C (Note 6)	gm	 90 70 70	 110 110 110	 120 135 150	μS
Feedback Pin Internal Pull−Down Resistor	V_{FB} = V_{UVP} to V_{REF}	R_{FB}	2	4.6	10	MΩ
Feedback Bias Current	V_{FB} = 2.5 V T_J = −40°C to +125°C T_J = −55°C to +125°C (Note 6)	I_{FB}	 0.25 0.2	 0.54 0.54	 1.25 1.25	μA
Control Bias Current	V_{FB} = 0 V	$I_{Control}$	−1	−	1	μA
Maximum Control Voltage	$I_{Control(pullup)}$ = 10 μA, V_{FB} = V_{REF} T_J = −40°C to +125°C T_J = −55°C to +125°C (Note 6)	V_{EAH}	 5 5	 5.5 5.5	 6 6.05	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
6. For coldest temperature, QA sampling at −40°C in production and −55°C specification is Guaranteed by Characterization.

Table 3. ELECTRICAL CHARACTERISTICS (Continued)
V_{FB} = 2.4 V, $V_{Control}$ = 4 V, Ct = 1 nF, V_{CS} = 0 V, V_{ZCD} = 0 V, C_{DRV} = 1 nF, V_{CC} = 12 V, unless otherwise specified
(For typical values, T_J = 25°C. For min/max values, T_J = −55°C to 125°C (Note 6), V_{CC} = 12 V, unless otherwise specified)

Characteristic	Test Conditions	Symbol	Min	Typ	Max	Unit
ERROR AMPLIFIER						
Minimum Control Voltage to Generate Drive Pulses	$V_{Control}$ = Decreasing until V_{DRV} is low, V_{Ct} = 0 V T_J = −40°C to +125°C T_J = −55°C to +125°C (Note 6)	$Ct_{(offset)}$	 0.37 0.37	 0.65 0.65	 0.88 1.1	V
Control Voltage Range	$V_{EAH} - Ct_{(offset)}$	$V_{EA(DIFF)}$	4.5	4.9	5.3	V
RAMP CONTROL						
Ct Peak Voltage	$V_{Control}$ = open	$V_{Ct(MAX)}$	4.775	4.93	5.025	V
On Time Capacitor Charge Current	$V_{Control}$ = open V_{Ct} = 0 V to $V_{Ct(MAX)}$	I_{charge}	235	275	297	μA
Ct Capacitor Discharge Duration	$V_{Control}$ = open V_{Ct} = $V_{Ct(MAX)}$ −100 mV to 500 mV	$t_{Ct(discharge)}$	−	50	150	ns
PWM Propagation Delay	dV/dt = 30 V/μs V_{Ct} = $V_{Control}$ − $Ct_{(offset)}$ to V_{DRV} = 10%	t_{PWM}	−	130	220	ns
CURRENT SENSE						
Current Sense Voltage Threshold		V_{ILIM}	0.45	0.5	0.55	V
Leading Edge Blanking Duration	V_{CS} = 2 V, V_{DRV} = 90% to 10%	t_{LEB}	100	190	350	ns
Overcurrent Detection Propagation Delay	dV/dt = 10 V/μs V_{CS} = V_{ILIM} to V_{DRV} = 10%	t_{CS}	40	100	170	ns
Current Sense Bias Current	V_{CS} = 2 V	I_{CS}	−1	−	1	μA
ZERO CURRENT DETECTION						
ZCD Arming Threshold	V_{ZCD} = Increasing	$V_{ZCD(ARM)}$	1.25	1.4	1.55	V
ZCD Triggering Threshold	V_{ZCD} = Decreasing	$V_{ZCD(TRIG)}$	0.6	0.7	0.83	V
ZCD Hysteresis		$V_{ZCD(HYS)}$	500	700	900	mV
ZCD Bias Current	V_{ZCD} = 5 V	I_{ZCD}	−2	−	+2	μA
Positive Clamp Voltage	I_{ZCD} = 3 mA T_J = −40°C to +125°C T_J = −55°C to +125°C (Note 6)	$V_{CL(POS)}$	 9.8 9.2	 10 10	 12 12	V
Negative Clamp Voltage	I_{ZCD} = −2 mA T_J = −40°C to +125°C T_J = −55°C to +125°C (Note 6)	$V_{CL(NEG)}$	 −0.9 −1.1	 −0.7 −0.7	 −0.5 −0.5	V
ZCD Propagation Delay	V_{ZCD} = 2 V to 0 V ramp, dV/dt = 20 V/μs V_{ZCD} = $V_{ZCD(TRIG)}$ to V_{DRV} = 90%	t_{ZCD}	−	100	170	ns
Minimum ZCD Pulse Width		t_{SYNC}	−	70	−	ns
Maximum Off Time in Absence of ZCD Transition	Falling V_{DRV} = 10% to Rising V_{DRV} = 90%	t_{start}	75	165	300	μs
DRIVE						
Drive Resistance	I_{source} = 100 mA I_{sink} = 100 mA	R_{OH} R_{OL}	− −	12 6	20 13	Ω
Rise Time	10% to 90%	t_{rise}	−	35	80	ns
Fall Time	90% to 10%	t_{fall}	−	25	70	ns
Drive Low Voltage	V_{CC} = $V_{CC(on)}$−200 mV, I_{sink} = 10 mA	$V_{out(start)}$	−	−	0.2	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
6. For coldest temperature, QA sampling at −40°C in production and −55°C specification is Guaranteed by Characterization.

TYPICAL CHARACTERISTICS

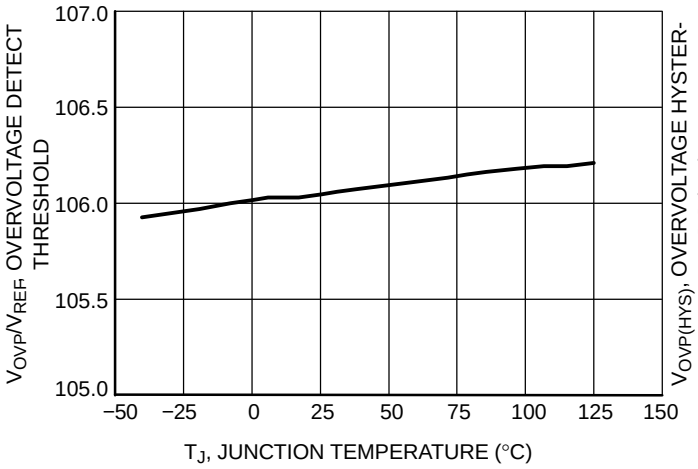


Figure 3. Overvoltage Detect Threshold vs. Junction Temperature

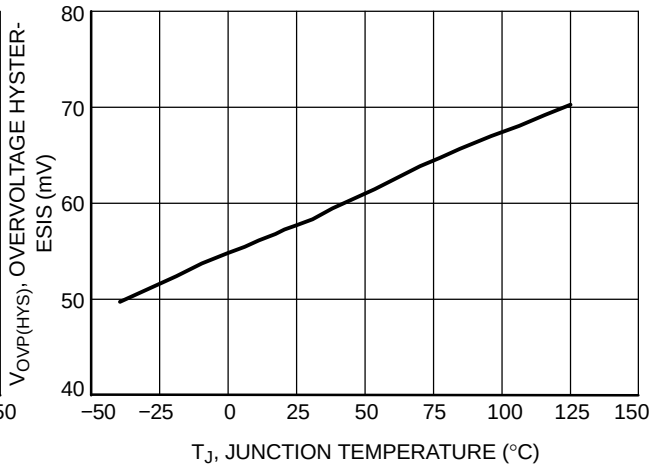


Figure 4. Overvoltage Hysteresis vs. Junction Temperature

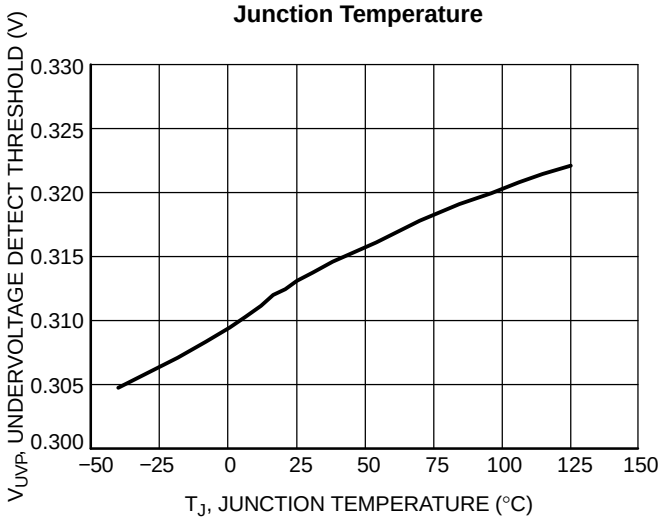


Figure 5. Undervoltage Detect Threshold vs. Junction Temperature

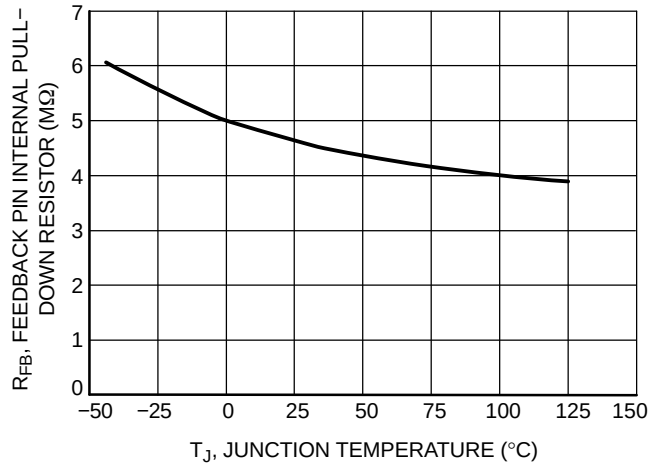


Figure 6. Feedback Pin Internal Pull−Down Resistor vs. Junction Temperature

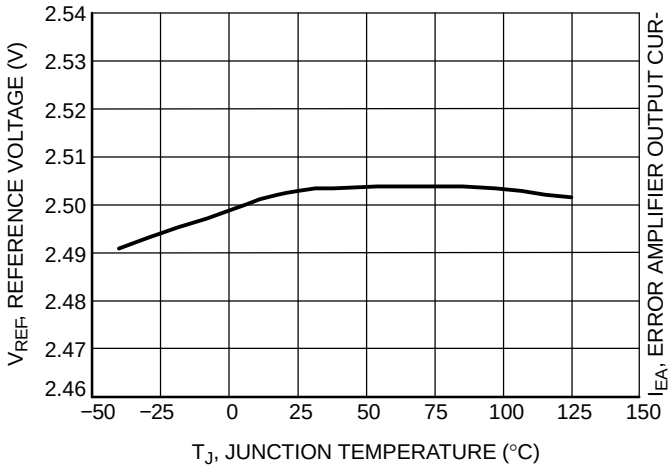


Figure 7. Reference Voltage vs. Junction Temperature

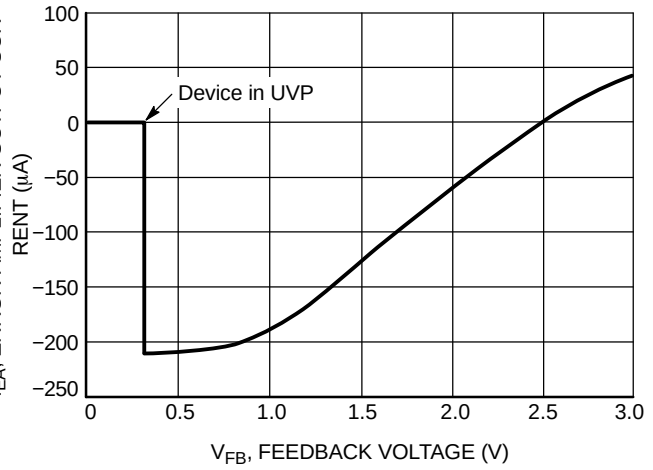


Figure 8. Error Amplifier Output Current vs. Feedback Voltage

TYPICAL CHARACTERISTICS

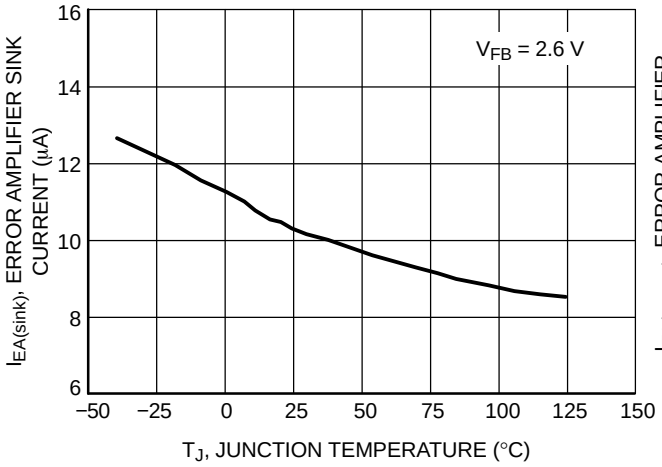


Figure 9. Error Amplifier Sink Current vs. Junction Temperature

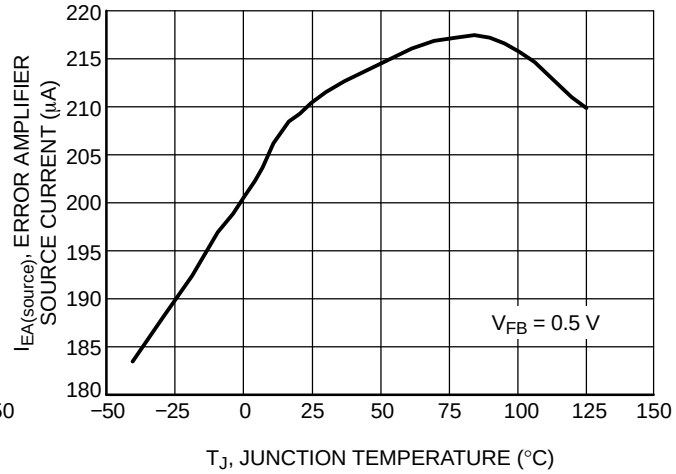


Figure 10. Error Amplifier Source Current vs. Junction Temperature

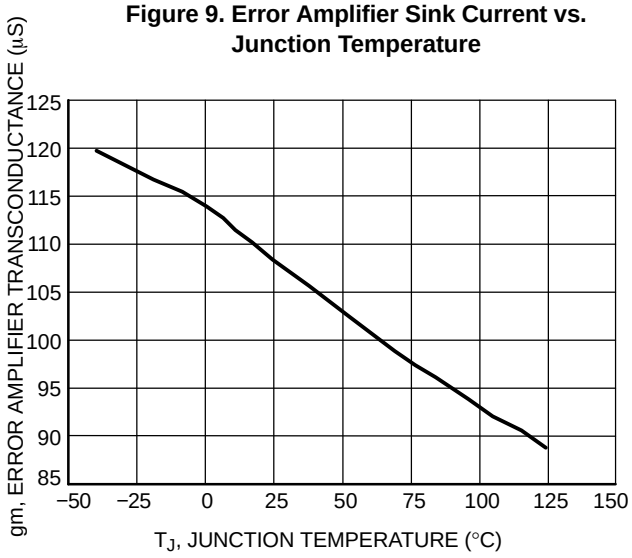


Figure 11. Error Amplifier Transconductance vs. Junction Temperature

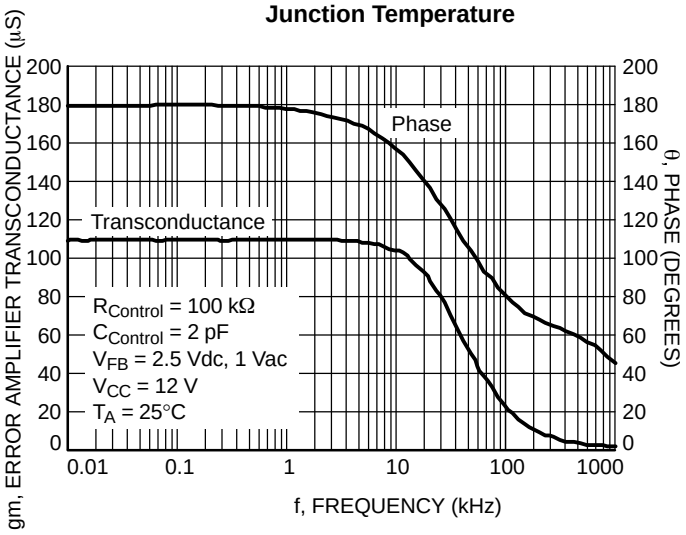


Figure 12. Error Amplifier Transconductance and Phase vs. Frequency

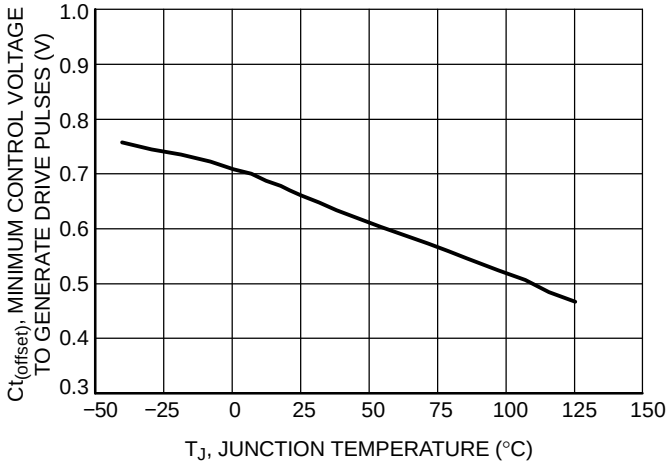


Figure 13. Minimum Control Voltage to Generate Drive Pulses vs. Junction Temperature

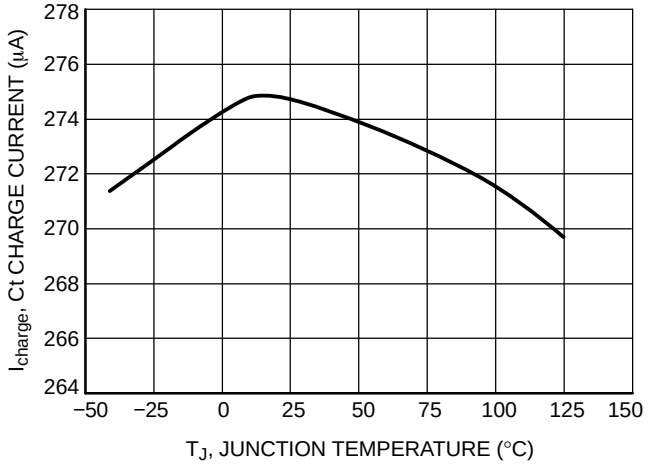


Figure 14. On Time Capacitor Charge Current vs. Junction Temperature

TYPICAL CHARACTERISTICS

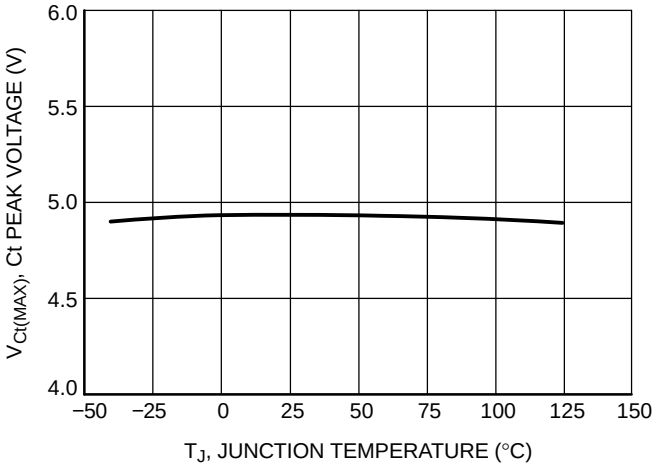


Figure 15. Ct Peak Voltage vs. Junction Temperature

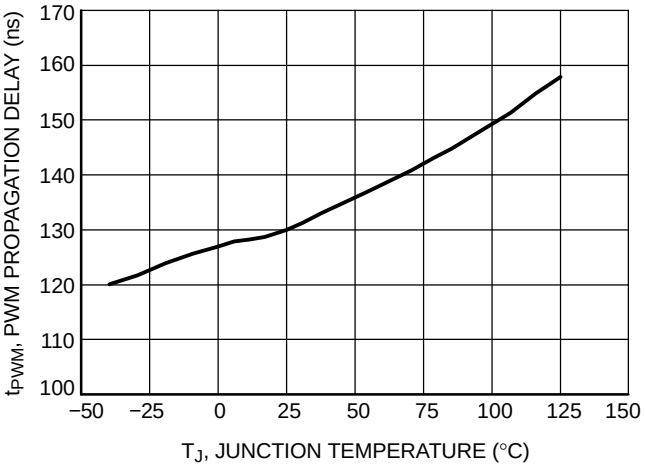


Figure 16. PWM Propagation Delay vs. Junction Temperature

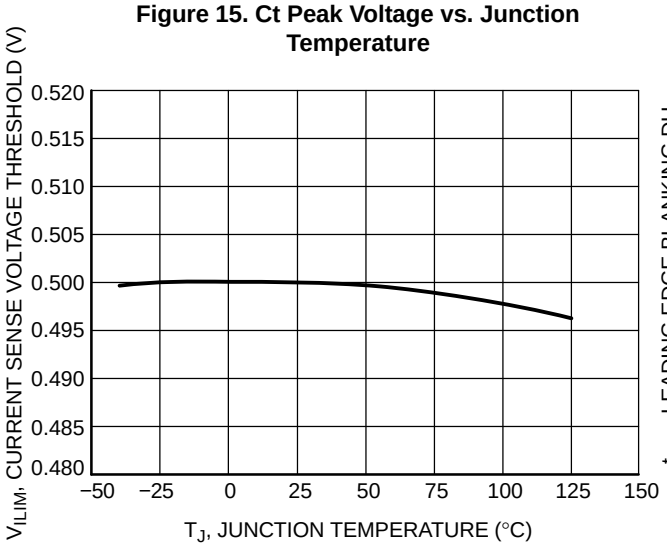


Figure 17. Current Sense Voltage Threshold vs. Junction Temperature

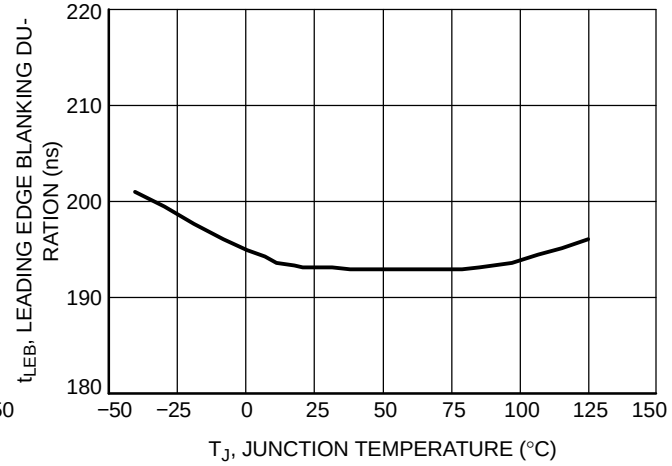


Figure 18. Leading Edge Blanking Duration vs. Junction Temperature

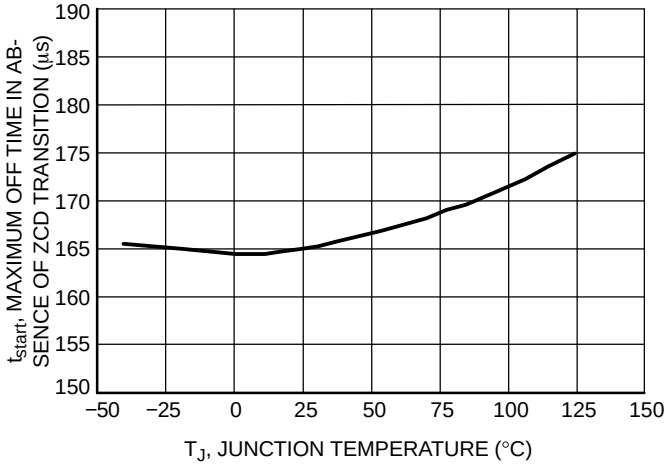


Figure 19. Maximum Off Time in Absence of ZCD Transition vs. Junction Temperature

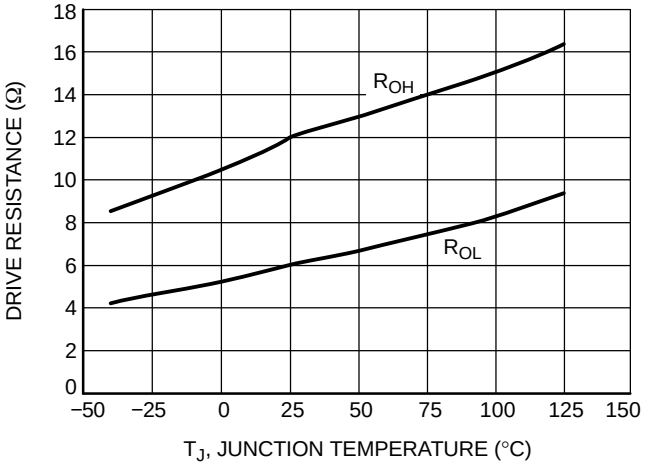


Figure 20. Drive Resistance vs. Junction Temperature

TYPICAL CHARACTERISTICS

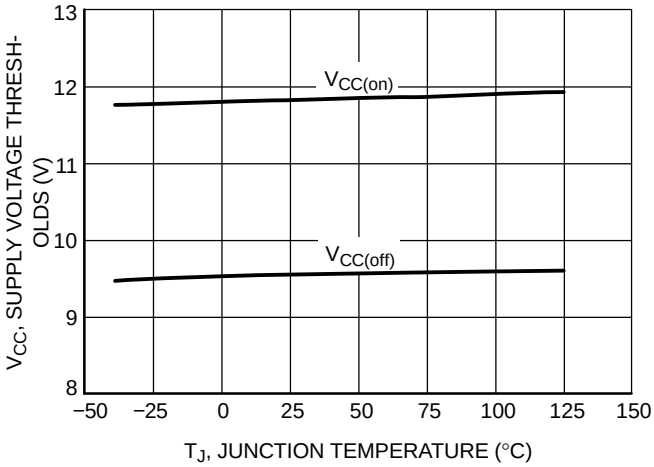


Figure 21. Supply Voltage Thresholds vs. Junction Temperature

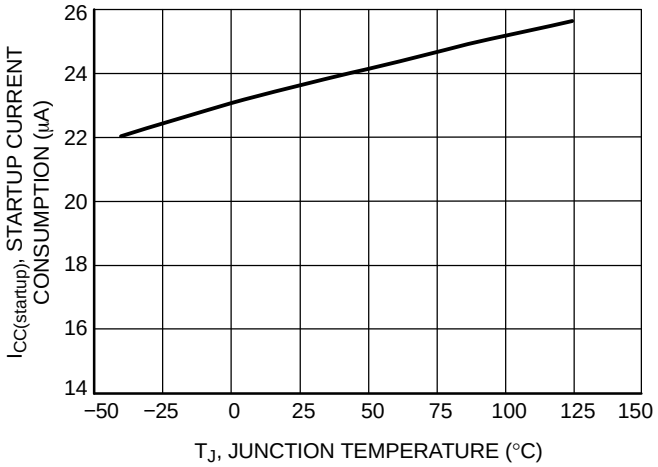


Figure 22. Startup Current Consumption vs. Junction Temperature

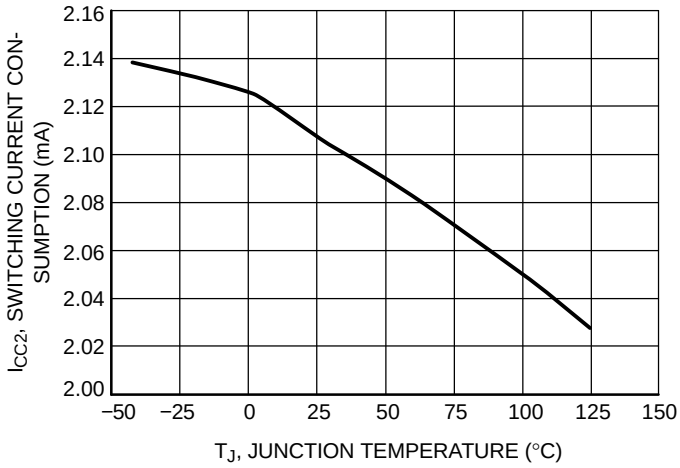


Figure 23. Switching Current Consumption vs. Junction Temperature

Introduction

The NCP1608 is a voltage mode, power factor correction (PFC) controller designed to drive cost−effective pre-converters to comply with line current harmonic regulations. This controller operates in critical conduction mode (CrM) suitable for applications up to 350 W. Its voltage mode scheme enables it to obtain near unity power factor without the need for a line-sensing network. A high precision transconductance error amplifier regulates the output voltage. The controller implements comprehensive safety features for robust designs.

The key features of the NCP1608 are:

- Constant On Time (Voltage Mode) CrM Operation. A high power factor is achieved without the need for input voltage sensing. This enables low standby power consumption.
- Accurate and Programmable On Time Limitation. The NCP1608 uses an accurate current source and an external capacitor to generate the on time.
- Wide Control Range. In high power applications (> 150 W), inadvertent skipping can occur at high input voltage and high output power if noise immunity is not provided. The noise immunity provided by the NCP1608 prevents inadvertent skipping.
- High Precision Voltage Reference. The error amplifier reference voltage is guaranteed at 2.5 V ±1.6% over process and temperature. This results in accurate output voltages.
- Low Startup Current Consumption. The current consumption is reduced to a minimum (< 35 μA) during startup, enabling fast, low loss charging of V_{CC}. The NCP1608 includes undervoltage lockout and provides sufficient V_{CC} hysteresis during startup to reduce the value of the V_{CC} capacitor.
- Powerful Output Driver. A Source 500 mA/Sink 800 mA totem pole gate driver enables rapid turn on and turn off times. This enables improved efficiencies and the ability to drive higher power MOSFETs. A combination of active and passive circuits ensures that the driver output voltage does not float high if V_{CC} does not exceed $V_{CC(on)}$.
- Accurate Fixed Overvoltage Protection (OVP). The OVP feature protects the PFC stage against excessive output overshoots that may damage the system. Overshoots typically occur during startup or transient loads.
- Undervoltage Protection (UVP). The UVP feature protects the system if there is a disconnection in the power path to C_{bulk} (i.e. C_{bulk} is unable to charge).
- Protection Against Open Feedback Loop. The OVP and UVP features protect against the disconnection of the output divider network to the FB pin. An internal resistor (R_{FB}) protects the system when the FB pin is floating (Floating Pin Protection, FPP).
- Overcurrent Protection (OCP). The inductor peak current is accurately limited on a cycle-by-cycle basis. The maximum inductor peak current is adjustable by modifying the current sense resistor. An integrated LEB filter reduces the probability of noise inadvertently triggering the overcurrent limit.
- Shutdown Feature. The PFC pre-converter is shutdown by forcing the FB pin voltage to less than V_{UVP}. In shutdown mode, the I_{CC} current consumption is reduced and the error amplifier is disabled.

Application Information

Most electronic ballasts and switching power supplies use a diode bridge rectifier and a bulk storage capacitor to produce a dc voltage from the utility ac line (Figure 24). This DC voltage is then processed by additional circuitry to drive the desired output.

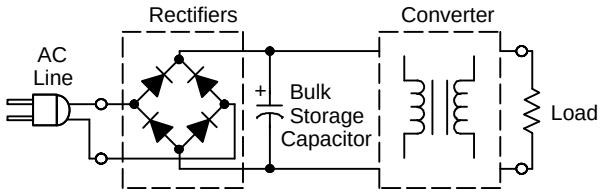


Figure 24. Typical Circuit without PFC

This rectifying circuit consumes current from the line when the instantaneous ac voltage exceeds the capacitor voltage. This occurs near the line voltage peak and the resulting current is non-sinusoidal with a large harmonic content. This results in a reduced power factor (typically < 0.6). Consequently, the apparent input power is higher than the real power delivered to the load. If multiple devices are connected to the same input line, the effect increases and a “line sag” is produced (Figure 25).

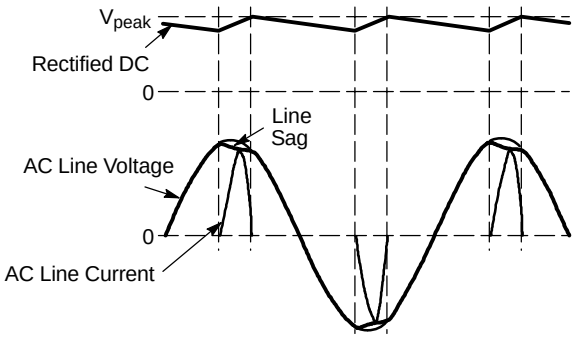


Figure 25. Typical Line Waveforms without PFC

Government regulations and utilities require reduced line current harmonic content. Power factor correction is implemented with either a passive or an active circuit to comply with regulations. Passive circuits contain a combination of large capacitors, inductors, and rectifiers that operate at the ac line frequency. Active circuits use a

high frequency switching converter to regulate the input current harmonics. Active circuits operate at a higher frequency, which enables them to be physically smaller, weigh less, and operate more efficiently than a passive circuit. With proper control of an active PFC stage, almost any complex load emulates a linear resistance, which significantly reduces the harmonic current content. Active PFC circuits are the most popular way to meet harmonic content requirements because of the aforementioned benefits. Generally, active PFC circuits consist of inserting a PFC pre−converter between the rectifier bridge and the bulk capacitor (Figure 26).

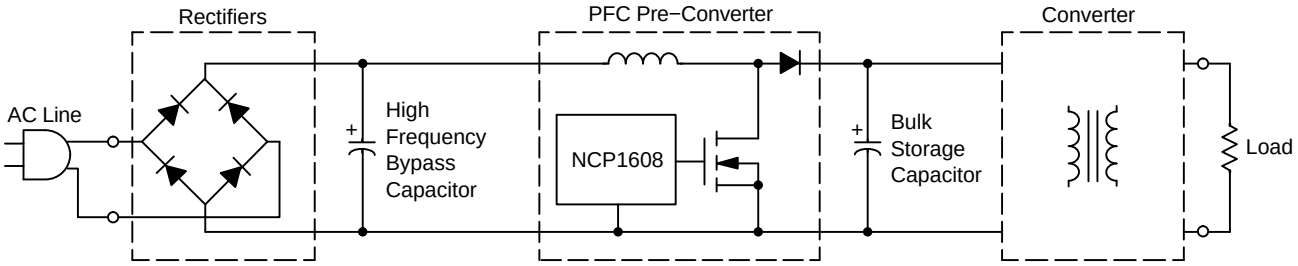


Figure 26. Active PFC Pre−Converter with the NCP1608

The boost (or step up) converter is the most popular topology for active power factor correction. With the proper control, it produces a constant voltage while consuming a sinusoidal current from the line. For medium power (< 350 W) applications, CrM is the preferred control method. CrM occurs at the boundary between discontinuous conduction mode (DCM) and continuous conduction mode (CCM). In CrM, the driver on time begins when the boost inductor current reaches zero. CrM operation is an ideal choice for medium power PFC boost stages because it combines the reduced peak currents of CCM operation with the zero current switching of DCM operation. The operation and waveforms in a PFC boost converter are illustrated in Figure 27.

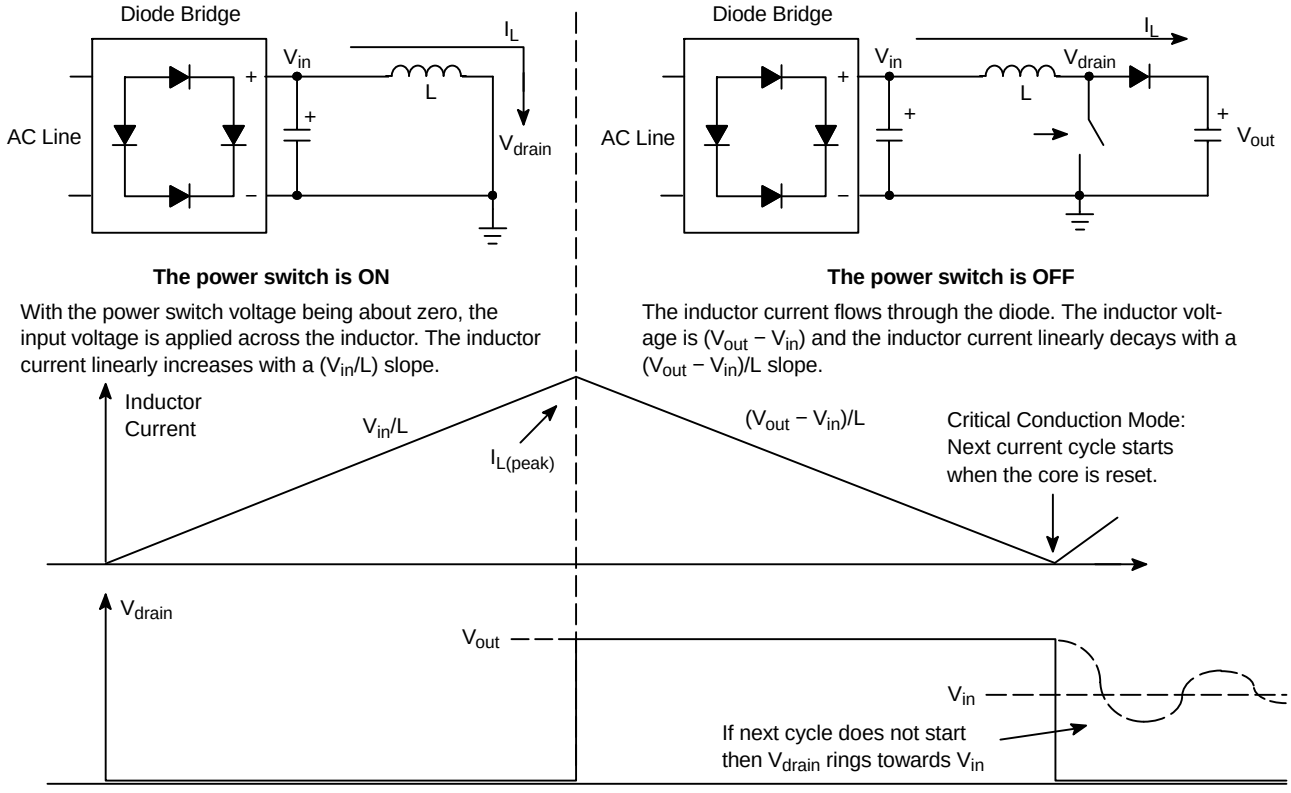


Figure 27. Schematic and Waveforms of an Ideal CrM Boost Converter

When the switch is closed, the inductor current increases linearly to the peak value. When the switch opens, the inductor current linearly decreases to zero. When the inductor current decreases to zero, the drain voltage of the switch (V_{drain}) is floating and begins to decrease. If the next switching cycle does not begin, then V_{drain} rings towards V_{in}. A derivation of equations found in AND8123 leads to the result that high power factor in CrM operation is achieved when the on time (t_{on}) of the switch is constant during an ac cycle and is calculated using Equation 1.

$$t_{on} = \frac{2 \cdot P_{out} \cdot L}{\eta \cdot Vac^2} \qquad \text{(eq. 1)}$$

Where P_{out} is the output power, L is the inductor value, η is the efficiency, and Vac is the rms input voltage.

A description of the switching over an ac line cycle is illustrated in Figure 28. The on time is constant, but the off time varies and is dependent on the instantaneous line voltage. The constant on time causes the peak inductor current ($I_{L(peak)}$) to scale with the ac line voltage. The NCP1608 represents an ideal method to implement a constant on time CrM control in a cost−effective and robust solution by incorporating an accurate regulation circuit, a low current consumption startup circuit, and advanced protection features.

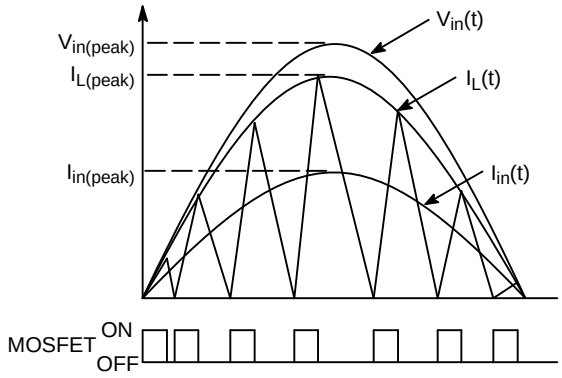


Figure 28. Inductor Waveform During CrM Operation

Error Amplifier Regulation

The NCP1608 regulates the boost output voltage using an internal error amplifier (EA). The negative terminal of the EA is pinned out to FB, the positive terminal is connected to a 2.5 V ± 1.6% reference (V_{REF}), and the EA output is pinned out to Control (Figure 29).

A feature of using a transconductance error amplifier is that the FB pin voltage is only determined by the resistor divider network connected to the output voltage, not the operation of the amplifier. This enables the FB pin to be used for sensing overvoltage or undervoltage conditions independently of the error amplifier.

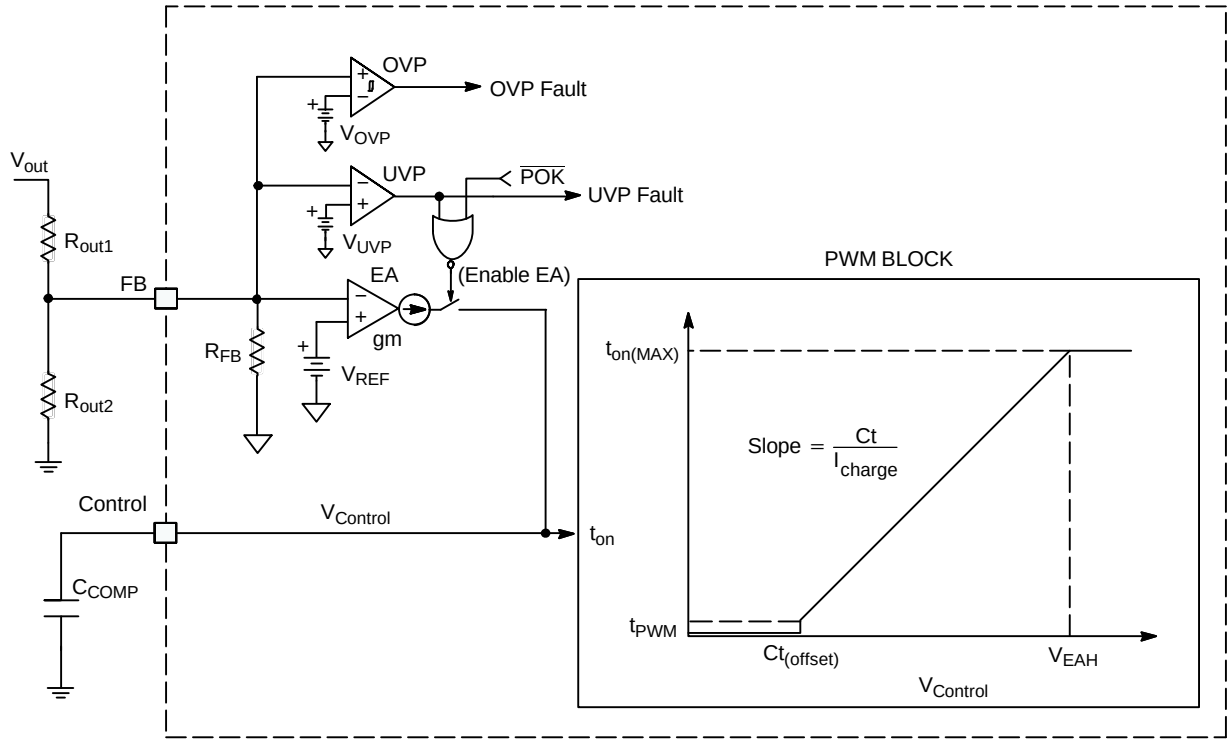


Figure 29. Error Amplifier and On Time Regulation Circuits

A resistor divider (R_{out1} and R_{out2}) scales down the boost output voltage (V_{out}) and is connected to the FB pin. If the output voltage is less than the target output voltage, then V_{FB} is less than V_{REF} and the EA increases the control voltage ($V_{Control}$). This increases the on time of the driver, which increases the power delivered to the output. The increase in delivered power causes V_{out} to increase until the target output voltage is achieved. Alternatively, if V_{out} is greater than the target output voltage, then $V_{Control}$ decreases to cause the on time to decrease until V_{out} decreases to the target output voltage. This cause and effect regulates V_{out} so that the scaled down V_{out} that is applied to FB through R_{out1} and R_{out2} is equal to V_{REF}. The presence of R_{FB} (4.6 MΩ typical value) for FPP is included in the divider network calculation.

The output voltage is set using Equation 2:

$$V_{out} = V_{REF} \cdot \left(R_{out1} \cdot \frac{R_{out2} + R_{FB}}{R_{out2} \cdot R_{FB}} + 1 \right) \quad \text{(eq. 2)}$$

The divider network bias current is selected to optimize the tradeoff of noise immunity and power dissipation. R_{out1} is calculated using the bias current and output voltage using Equation 3:

$$R_{out1} = \frac{V_{out}}{I_{bias(out)}} \quad \text{(eq. 3)}$$

Where $I_{bias(out)}$ is the output divider network bias current. R_{out2} is dependent on V_{out}, R_{out1}, and R_{FB}.

R_{out2} is calculated using Equation 4:

$$R_{out2} = \frac{R_{out1} \cdot R_{FB}}{R_{FB} \cdot \left(\frac{V_{out}}{V_{REF}} - 1 \right) - R_{out1}} \quad \text{(eq. 4)}$$

The PFC stage consumes a sinusoidal current from a sinusoidal line voltage. The converter provides the load with a power that matches the average demand only. The output capacitor (C_{bulk}) compensates for the difference between the delivered power and the power consumed by the load. When the power delivered to the load is less than the power consumed by the load, C_{bulk} discharges. When the delivered power is greater than the power consumed by the load, C_{bulk} charges to store the excess energy. The situation is depicted in Figure 30.

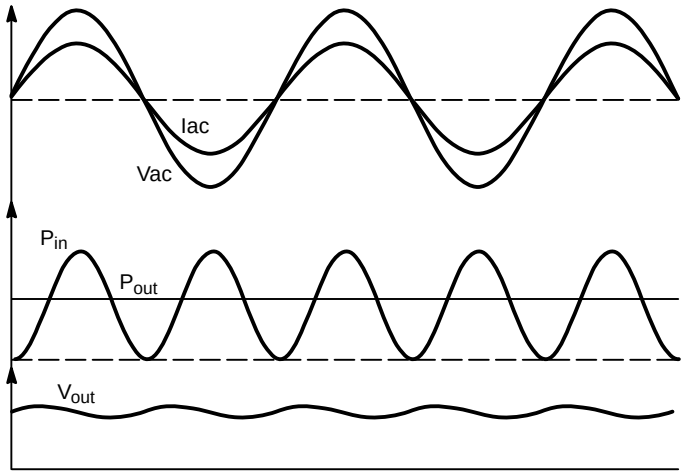


Figure 30. Output Voltage Ripple for a Constant Output Power

Due to the charging/discharging of C_{bulk}, V_{out} contains a ripple at a frequency of either 100 Hz (for a 50 Hz line frequency in Europe) or 120 Hz (for a 60 Hz line frequency in the USA). The V_{out} ripple is attenuated by the regulation loop to ensure $V_{Control}$ is constant during the ac line cycle for the proper shaping of the line current. To ensure $V_{Control}$ is constant during the ac line cycle, the loop bandwidth is typically set below 20 Hz. A type 1 compensation network consists of a capacitor (C_{COMP}) connected between the Control and ground pins (see Figure 1). The capacitor value that sets the loop bandwidth is calculated using Equation 5:

$$C_{COMP} = \frac{gm}{2 \cdot \pi \cdot f_{CROSS}} \quad \text{(eq. 5)}$$

Where f_{CROSS} is the crossover frequency and gm is the error amplifier transconductance. The crossover frequency is set below 20 Hz.

On Time Sequence

The switching pattern consists of constant on times and variable off times for a given rms input voltage and output load. The NCP1608 controls the on time with the capacitor connected to the Ct pin. A current source charges the Ct capacitor to a voltage derived from the Control pin voltage ($V_{Ct(off)}$). $V_{Ct(off)}$ is calculated using Equation 6:

$$V_{Ct(off)} = V_{Control} - Ct_{(offset)} = \frac{2 \cdot P_{out} \cdot L \cdot I_{charge}}{\eta \cdot Vac^2 \cdot Ct} \quad \text{(eq. 6)}$$

When $V_{Ct(off)}$ is reached, the drive turns off (Figure 31).

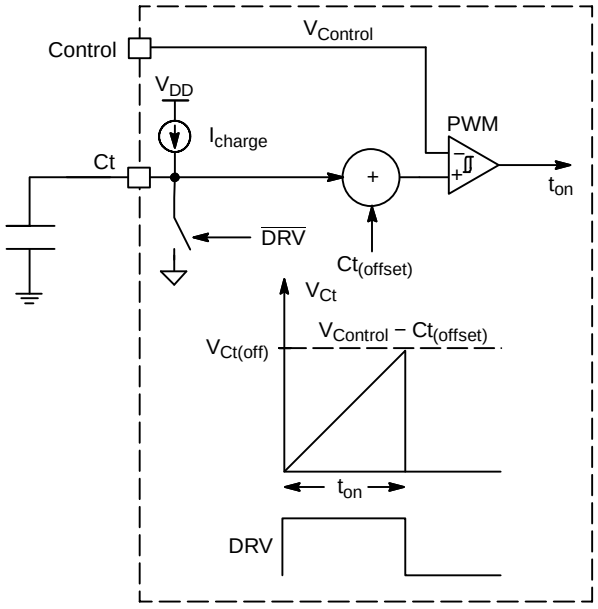


Figure 31. On Time Generation

$V_{Control}$ varies with the rms input voltage and output load, which naturally satisfies Equation 1. The on time is constant during the ac line cycle if the values of compensation components are sufficient to filter out the V_{out} ripple. The maximum on time of the controller occurs when $V_{Control}$ is at the maximum. The Ct capacitor is sized to ensure that the required on time is reached at maximum output power and the minimum input voltage condition. The on time is calculated using Equation 7:

$$t_{on} = \frac{Ct \cdot V_{Ct(MAX)}}{I_{charge}} \qquad \text{(eq. 7)}$$

Combining Equation 7 with Equation 1, results in Equation 8:

$$Ct \geq \frac{2 \cdot P_{out} \cdot L_{MAX} \cdot I_{charge}}{\eta \cdot Vac_{LL}^{2} \cdot V_{Ct(MAX)}} \qquad \text{(eq. 8)}$$

To calculate the minimum Ct value:

$V_{Ct(MAX)}$ = 4.775 V (minimum value),

I_{charge} = 297 μA (maximum value), Vac_{LL} is the minimum rms input voltage, and L_{MAX} is the maximum inductor value.

Off Time Sequence

In CrM operation, the on time is constant during the ac line cycle and the off time varies with the instantaneous input voltage. When the inductor current reaches zero, the drain voltage (V_{drain} in Figure 27) resonates towards V_{in}. Measuring V_{drain} is a way to determine when the inductor current reaches zero. To measure the high voltage V_{drain} directly is generally not economical or practical. Instead, a winding is added to the boost inductor. This winding, called the Zero Current Detection (ZCD) winding, provides a scaled representation of the inductor voltage that is sensed by the controller. Figure 32 shows waveforms of ideal CrM operation using a ZCD winding.

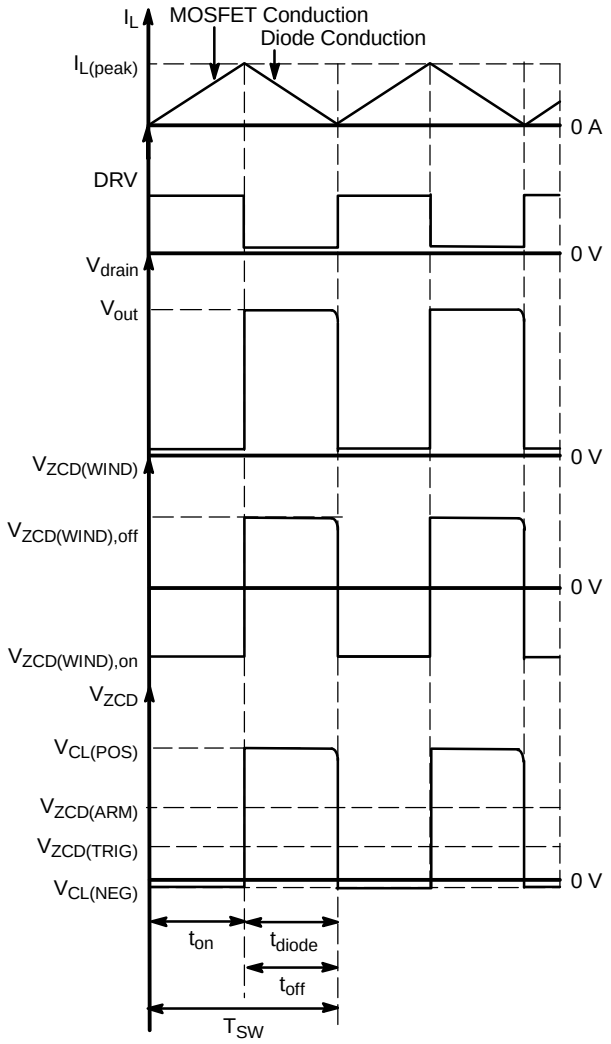


Figure 32. Ideal CrM Waveforms Using a ZCD Winding

The voltage induced on the ZCD winding during the switch on time ($V_{ZCD(WIND),on}$) is calculated using Equation 9:

$$V_{ZCD(WIND),on} = \frac{-V_{in}}{N_B : N_{ZCD}} \qquad \text{(eq. 9)}$$

Where V_{in} is the instantaneous input voltage and N_B:N_{ZCD} is the turns ratio of the boost winding to the ZCD winding.

The voltage induced on the ZCD winding during the switch off time ($V_{ZCD(WIND),off}$) is calculated using Equation 10:

$$V_{ZCD(WIND),off} = \frac{V_{out} - V_{in}}{N_B : N_{ZCD}} \qquad \text{(eq. 10)}$$

When the inductor current reaches zero, the ZCD pin voltage (V_{ZCD}) follows the ZCD winding voltage ($V_{ZCD(WIND)}$) and begins to decrease and ring towards zero volts. The NCP1608 detects the falling edge of V_{ZCD} and turns the driver on. To ensure that a ZCD event is not inadvertently detected, the NCP1608 logic verifies that V_{ZCD} exceeds $V_{ZCD(ARM)}$ and then senses that V_{ZCD} decreases to less than $V_{ZCD(TRIG)}$ (Figure 33).

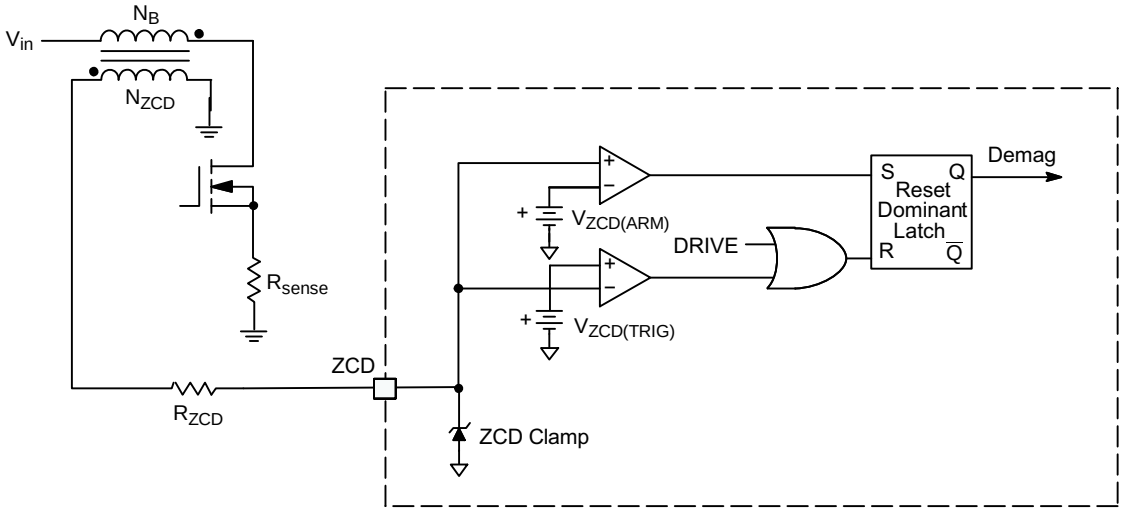


Figure 33. Implementation of the ZCD Block

This sequence achieves CrM operation. The maximum $V_{ZCD(ARM)}$ sets the maximum turns ratio and is calculated using Equation 11:

$$N_B : N_{ZCD} \leq \frac{V_{out} - \left(\sqrt{2} \cdot Vac_{HL}\right)}{V_{ZCD(ARM)}} \qquad \text{(eq. 11)}$$

Where Vac_{HL} is the maximum rms input voltage and $V_{ZCD(ARM)}$ = 1.55 V (maximum value).

The NCP1608 prevents excessive voltages on the ZCD pin by clamping V_{ZCD}. When the ZCD winding is negative, the ZCD pin is internally clamped to $V_{CL(NEG)}$. Similarly, when the ZCD winding is positive, the ZCD pin is internally clamped to $V_{CL(POS)}$. A resistor (R_{ZCD} in Figure 33) is necessary to limit the current into the ZCD pin. The maximum ZCD pin current ($I_{ZCD(MAX)}$) is limited to less than 10 mA. R_{ZCD} is calculated using Equation 12:

$$R_{ZCD} \geq \frac{\sqrt{2} \cdot Vac_{HL}}{I_{ZCD(MAX)} \cdot (N_B : N_{ZCD})} \qquad \text{(eq. 12)}$$

The value of R_{ZCD} and the parasitic capacitance of the ZCD pin determine when the ZCD winding signal is detected and the drive turn on begins. A large R_{ZCD} value creates a long delay before detecting the ZCD event. In this case, the controller operates in DCM and the power factor is reduced. If the R_{ZCD} value is too small, the drive turns on when the drain voltage is high and efficiency is reduced. A popular strategy for selecting R_{ZCD} is to use the R_{ZCD} value that achieves minimum drain voltage turn on. This value is found experimentally. Figure 34 shows the realistic waveforms for CrM operation due to R_{ZCD} and the ZCD pin capacitance.

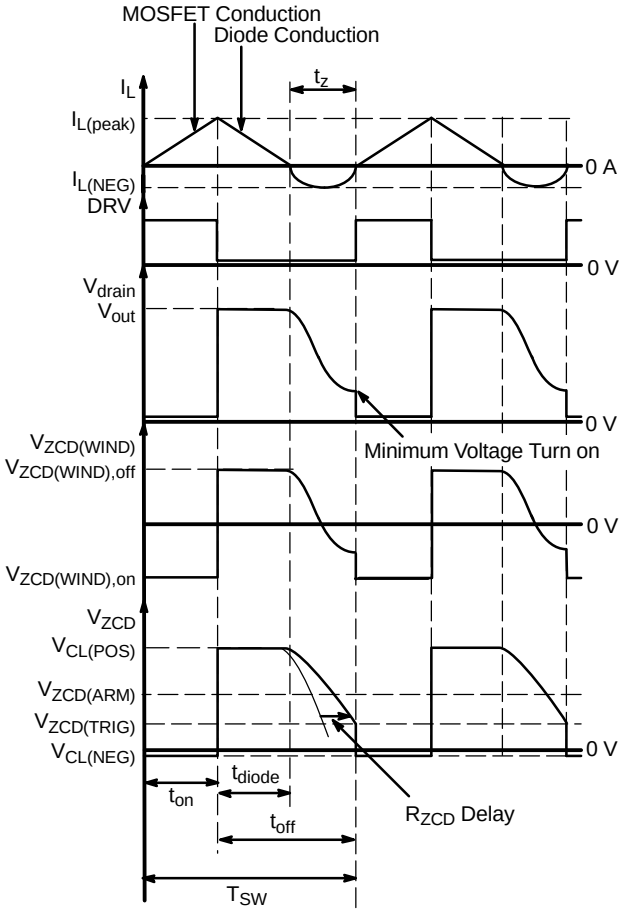


Figure 34. Realistic CrM Waveforms Using a ZCD Winding with R_{ZCD} and the ZCD Pin Capacitance

During the delay caused by R_{ZCD} and the ZCD pin capacitance, the equivalent drain capacitance ($C_{EQ(drain)}$) discharges through the path shown in Figure 35.

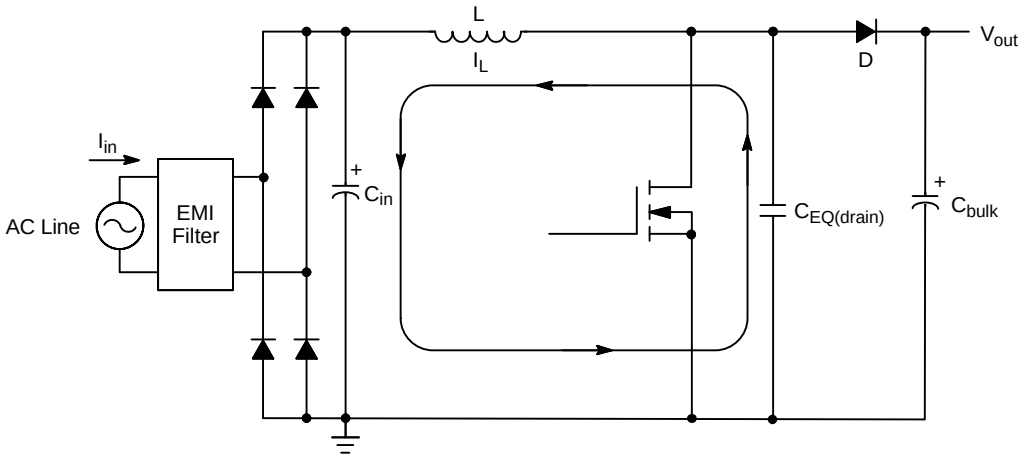


Figure 35. Equivalent Drain Capacitance Discharge Path

$C_{EQ(drain)}$ is the combined parasitic capacitances of the MOSFET, the diode, and the inductor. C_{in} is charged by the energy discharged by $C_{EQ(drain)}$. The charging of C_{in} reverse biases the bridge rectifier and causes the input current (I_{in}) to decrease to zero. The zero input current causes THD to increase. To reduce THD, the ratio (t_z / T_{SW}) is minimized, where t_Z is the period from when I_L = 0 A to when the drive turns on. The ratio (t_z / T_{SW}) is inversely proportional to the square root of L.

During startup, there is no energy in the ZCD winding and no voltage signal to activate the ZCD comparators. This means that the drive never turns on. To enable the PFC stage to start under these conditions, an internal watchdog timer (t_{start}) is integrated into the controller. This timer turns the drive on if the drive has been off for more than 165 μs (typical value). This feature is deactivated during a fault mode (OVP or UVP), and reactivated when the fault is removed.

Wide Control Range

The Ct charging threshold ($V_{Ct(off)}$) decreases as the output power is decreased from the maximum output power to the minimum output power in the application. In high power applications (> 150 W), $V_{Control}$ is reduced to a low voltage at a large output power and $Ct_{(offset)}$ remains constant. The result is that $V_{Ct(off)}$ is reduced to a low voltage at a large output power. The low $V_{Control}$ and $V_{Ct(off)}$ voltages are susceptible to noise. The large output power combined with the low $V_{Control}$ and $V_{Ct(off)}$ increase the probability of noise interfering with the control signals and on time duration (Figures 36 and 37). The noise induces voltage spikes on the Control pin and Ct pin that reduces the drive on time from the on time determined by the feedback loop ($t_{on(loop)}$). The reduced on time causes the energy stored in the inductor (L) to be reduced. The result is that V_{ZCD} does not exceed $V_{ZCD(ARM)}$ and the drive remains off until t_{start} expires. This sequence results in pulse skipping and reduced power factor.

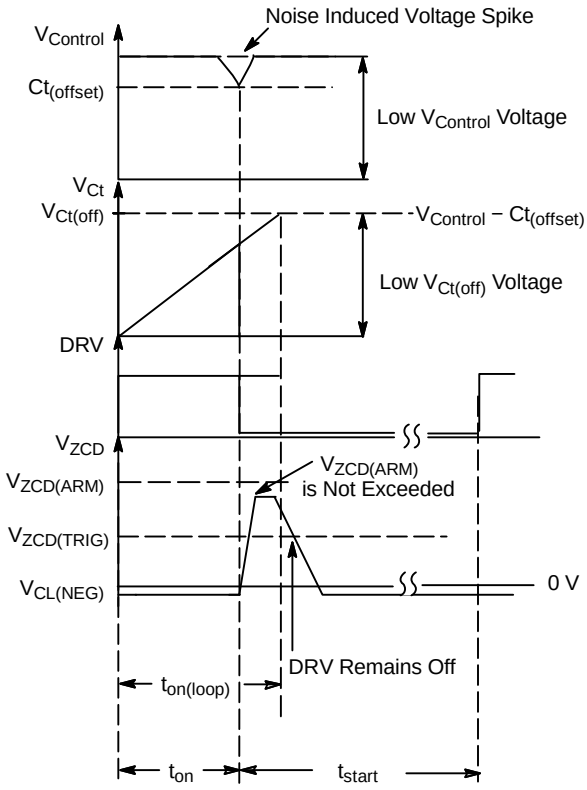


Figure 36. Control Pin Noise Induced On Time Reduction and Pulse Skipping

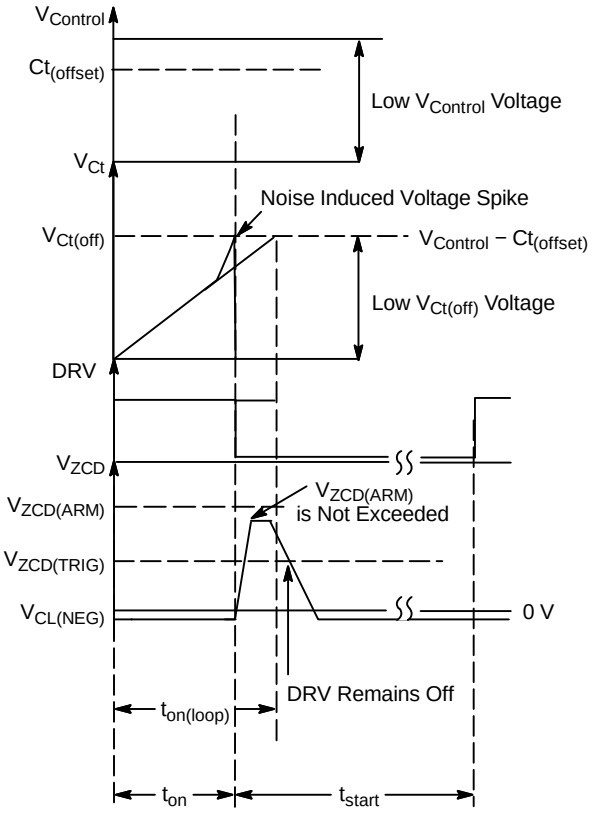


Figure 37. Ct Pin Noise Induced On Time Reduction and Pulse Skipping

The wide control range of the NCP1608 increases $V_{Control}$ and $V_{Ct(off)}$ in comparison to devices with less control range. Figure 38 compares $V_{Ct(off)}$ of the NCP1608 to a device with a 3 V control range for an application with the following parameters:

P_{out} = 250 W

L = 200 μH

η = 92%

Vac_{LL} = 85 Vac

Vac_{HL} = 265 Vac

Figure 38 shows that $V_{Ct(off)}$ of the NCP1608 is 50% larger than the 3 V control range device. The 50% increase enables the NCP1608 to prevent inadvertent skipping at high input voltages and high output power.

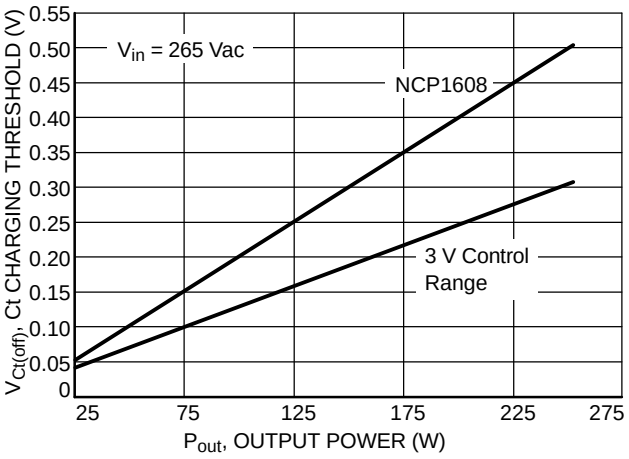


Figure 38. Comparison of Ct Charging Threshold vs. Output Power

Startup

Generally, a resistor connected between the rectified ac line and V_{CC} charges the V_{CC} capacitor to $V_{CC(on)}$. The low startup current consumption (< 35 μA) enables minimized standby power dissipation and reduced startup durations. When V_{CC} exceeds $V_{CC(on)}$, the internal references and logic of the NCP1608 are enabled. The controller includes an undervoltage lockout (UVLO) feature that ensures that the NCP1608 is enabled until V_{CC} decreases to less than $V_{CC(off)}$. This hysteresis ensures sufficient time for the auxiliary winding to supply V_{CC} (Figure 39).

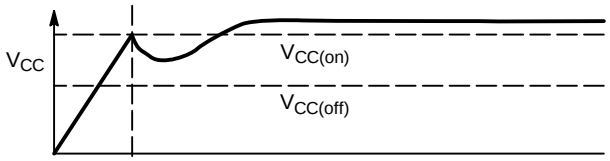


Figure 39. Typical V_{CC} Startup Waveform

When the PFC pre-converter is loaded by a switch−mode power supply (SMPS), it is generally preferable for the SMPS controller to startup first. The SMPS then supplies the NCP1608 V_{CC}. Advanced controllers, such as the NCP1230 or NCP1381, control the enabling of the PFC stage (see Figure 40) and achieve optimal system performance. This sequence eliminates the startup resistors and improves the standby power dissipation of the system.

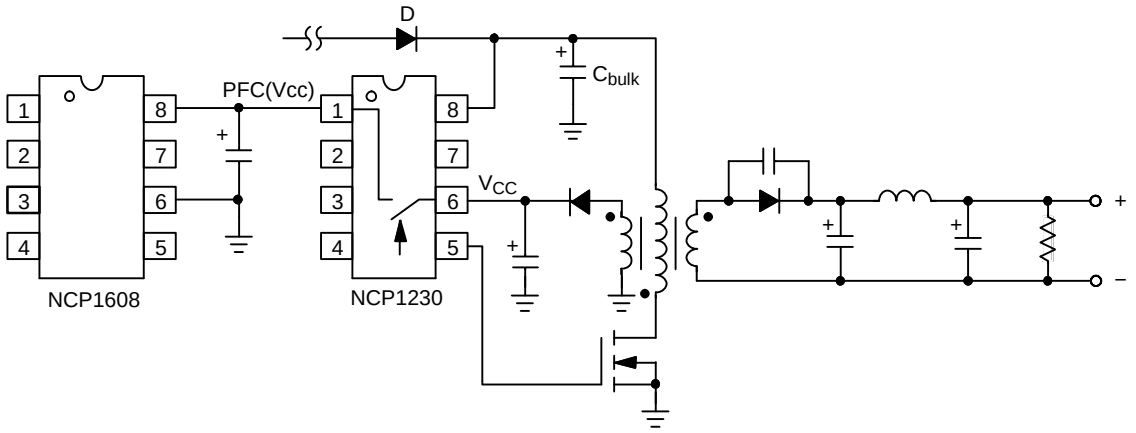


Figure 40. NCP1608 Supplied by a Downstream SMPS Controller (NCP1230)

Soft Start

When V_{CC} exceeds $V_{CC(on)}$, t_{start} begins counting. When t_{start} expires, the error amplifier is enabled and begins charging the compensation network. The drive is enabled when $V_{Control}$ exceeds $Ct_{(offset)}$. The charging of the compensation network slowly increases the drive on time from the minimum time (t_{PWM}) to the steady state on time. This creates a natural soft start mode that reduces the stress of the power components (Figure 41).

Output Driver

The NCP1608 includes a powerful output driver capable of sourcing 500 mA and sinking 800 mA. This enables the controller to drive power MOSFETs efficiently for medium power (≤ 350 W) applications. Additionally, the driver stage provides both passive and active pull−down circuits (Figure 42). The pull−down circuits force the driver output to a voltage less than the turn−on threshold voltage of a power MOSFET when $V_{CC(on)}$ is not reached.

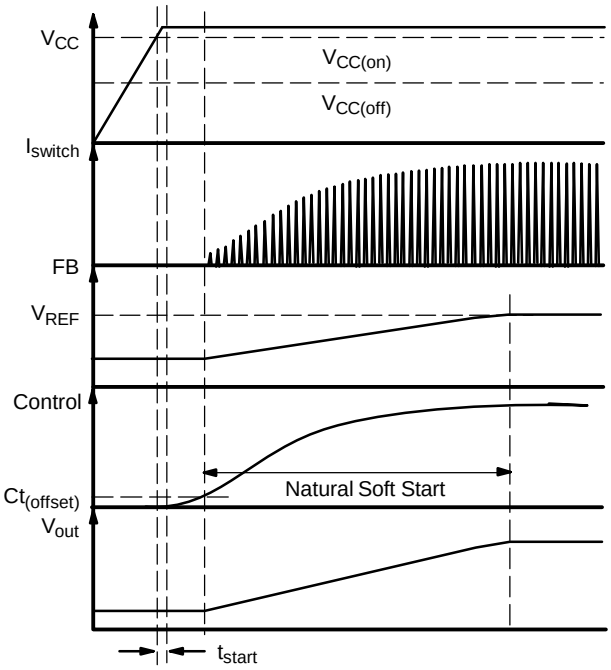


Figure 41. Startup Timing Diagram Showing the Natural Soft Start of the Control Pin

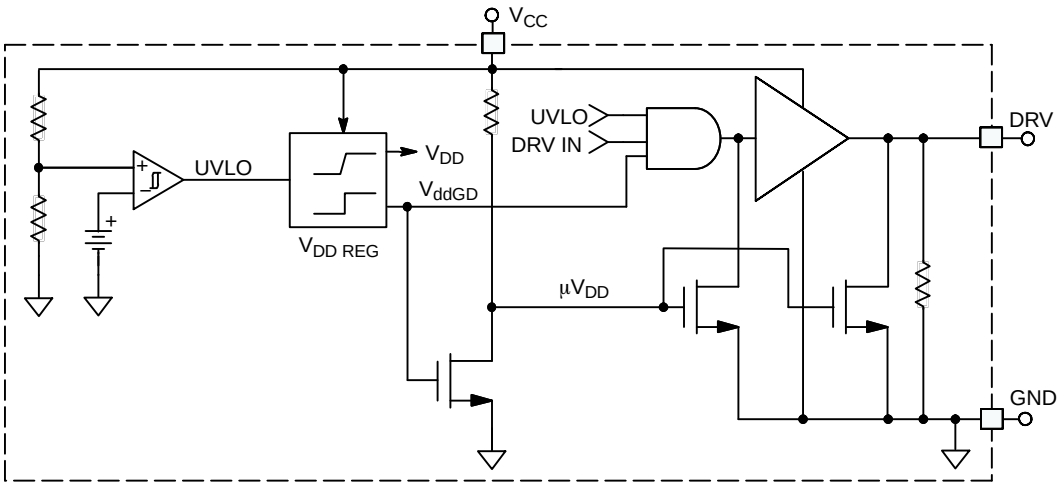


Figure 42. Output Driver Stage and Pull−Down Circuits

Overvoltage Protection (OVP)

The low bandwidth of the feedback network causes active PFC stages to react to changes in output load or input voltages slowly. Consequently, there is a risk of overshoots during startup, load steps, and line steps. For reliable operation, it is critical that overvoltage protection (OVP) prevents the output voltage from exceeding the ratings of the PFC stage components. The NCP1608 detects excessive output voltages and disables the driver until V_{out} decreases to a safe level, which ensures that V_{out} is within the PFC stage component ratings. An internal comparator connected to the FB pin provides the OVP protection. The OVP detection voltage is calculated using Equation 13:

$$V_{out(OVP)} = \frac{V_{OVP}}{V_{REF}} \cdot V_{REF} \cdot \left(R_{out1} \cdot \frac{R_{out2} + R_{FB}}{R_{out2} \cdot R_{FB}} + 1 \right) \quad \text{(eq. 13)}$$

Where V_{OVP}/V_{REF} is the OVP detection threshold.

The value of C_{bulk} is sized to ensure that OVP is not inadvertently triggered by the 100 Hz or 120 Hz ripple of V_{out}. The minimum value of C_{bulk} is calculated using Equation 14:

$$C_{bulk} \geq \frac{P_{out}}{2 \cdot \pi \cdot V_{ripple(peak-peak)} \cdot f_{line} \cdot V_{out}} \quad \text{(eq. 14)}$$

Where $V_{ripple(peak-peak)}$ is the peak−to−peak output voltage ripple and f_{line} is the ac line frequency.

$V_{ripple(peak-peak)}$ is calculated using Equation 15:

$$V_{ripple(peak-peak)} < 2 \cdot \left(V_{out(OVP)} - V_{out} \right) \quad \text{(eq. 15)}$$

The OVP logic includes hysteresis ($V_{OVP(HYS)}$) to ensure that V_{out} has sufficient time to discharge before the NCP1608 attempts to restart and to ensure noise immunity. The output voltage at which the NCP1608 attempts a restart ($V_{out(OVPL)}$) is calculated using Equation 16:

$$V_{out(OVPL)} = \left(\left(\frac{V_{OVP}}{V_{REF}} \cdot V_{REF} \right) - V_{OVP(HYS)} \right) \cdot \left(R_{out1} \cdot \frac{R_{out2} + R_{FB}}{R_{out2} \cdot R_{FB}} + 1 \right) \quad \text{(eq. 16)}$$

Figure 43 depicts the operation of the OVP circuitry.

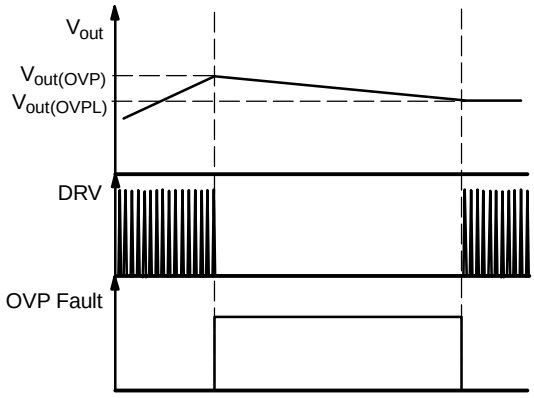


Figure 43. OVP Operation

Undervoltage Protection (UVP)

When the input voltage is applied to the PFC stage, V_{out} is forced to equate to the peak of the line voltage. The NCP1608 detects an undervoltage fault if V_{out} is unusually low, such that V_{FB} is less than V_{UVP} . During an UVP fault, the drive and error amplifier are disabled. The UVP feature protects the system if there is a disconnection in the power path to C_{bulk} (i.e. C_{bulk} is unable to charge) or if R_{out1} is disconnected.

The output voltage that causes an UVP fault is calculated using Equation 17:

$$V_{out(UVP)} = V_{UVP} \cdot \left(R_{out1} \cdot \frac{R_{out2} + R_{FB}}{R_{out2} \cdot R_{FB}} + 1 \right) \quad \text{(eq. 17)}$$

Open Feedback Loop Protection

The NCP1608 features comprehensive protection against open feedback loop conditions by including OVP, UVP, and FPP. Figure 44 illustrates three conditions in which the feedback loop is open. The corresponding number below describes each condition shown in Figure 44.

1. **UVP Protection:** The connection from R_{out1} to the FB pin is open. R_{out2} pulls down the FB pin to ground. The UVP comparator detects an UVP fault and the drive and error amplifier are disabled.
2. **OVP Protection:** The connection from R_{out2} to the FB pin is open. R_{out1} pulls up the FB pin to V_{out}. The ESD diode clamps the FB voltage to 10 V and R_{out1} limits the current into the FB pin. The OVP comparator detects an OVP fault and the drive is disabled.

3. **FPP Protection:** The FB pin is floating. R_{FB} pulls down the FB voltage below V_{UVP}. The UVP comparator detects an UVP fault and the drive and error amplifier are disabled.

UVP and OVP protect the system from low bulk voltages and rapid operating point changes respectively, while FPP protects the system against floating feedback pin conditions. If FPP is not implemented and a manufacturing error causes the FB pin to float, then V_{FB} is dependent on the coupling within the system and the surrounding environment. The coupled V_{FB} may be within the regulation limits (i.e. $V_{UVP} < V_{FB} < V_{REF}$) and cause the controller to deliver excessive power. The result is that V_{out} increases until a component fails due to the voltage stress.

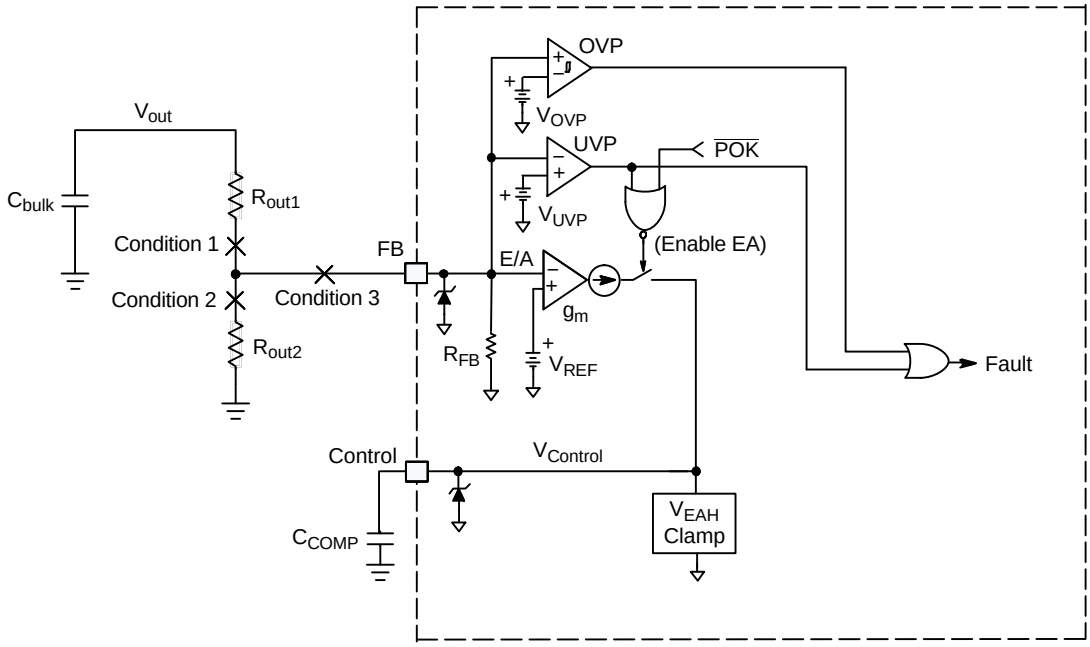


Figure 44. Open Feedback Loop Protection

Overcurrent Protection (OCP)

The dedicated CS pin of the NCP1608 senses the inductor peak current and limits the driver on time if the voltage of the CS pin exceeds V_{ILIM}. The maximum inductor peak current is programmed by adjusting R_{sense}. The inductor peak current is calculated using Equation 18:

$$I_{L(peak)} = \frac{V_{ILIM}}{R_{sense}} \qquad \text{(eq. 18)}$$

An internal LEB filter (Figure 45) reduces the probability of switching noise inadvertently triggering the overcurrent limit. This filter blanks out the CS signal for a duration of t_{LEB}. If additional filtering is necessary, a small RC filter is connected between R_{sense} and the CS pin.

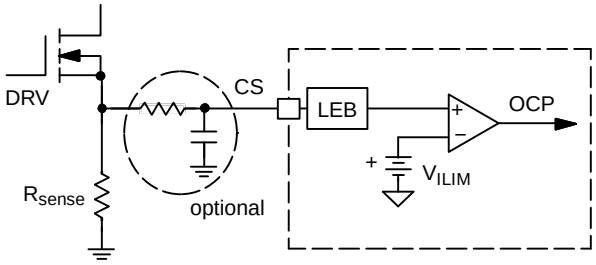


Figure 45. OCP Circuitry with Optional External RC Filter

Shutdown Mode

The NCP1608 enables the user to set the controller in a standby mode of operation. To shutdown the controller, the FB pin is forced to less than V_{UVP}. When using the FB pin for shutdown (Figure 46), the designer must ensure that no significant leakage current exists in the shutdown circuitry. Any leakage current affects the output voltage regulation.

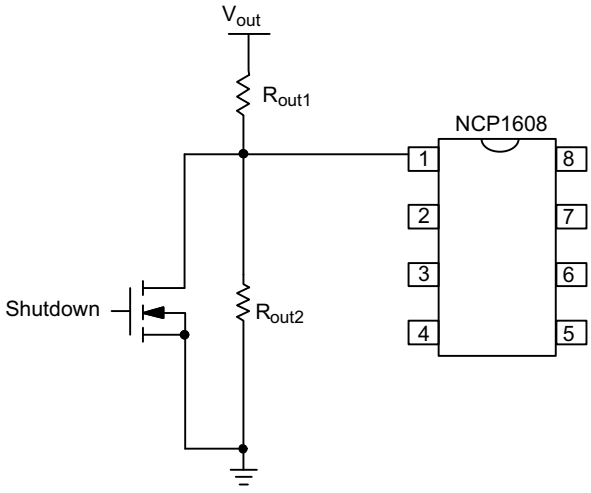


Figure 46. Shutting Down the PFC Stage

Application Information

ON Semiconductor provides an electronic design tool, a demonstration board, and an application note to facilitate the design of the NCP1608 and reduce development cycle time. All the tools can be downloaded or ordered at www.onsemi.com.

The electronic design tool allows the user to easily determine most of the system parameters of a boost pre−converter. The demonstration board is a boost pre−converter that delivers 100 W at 400 V. The circuit schematic is shown in Figure 47. The pre−converter design is described in Application Note AND8396/D.

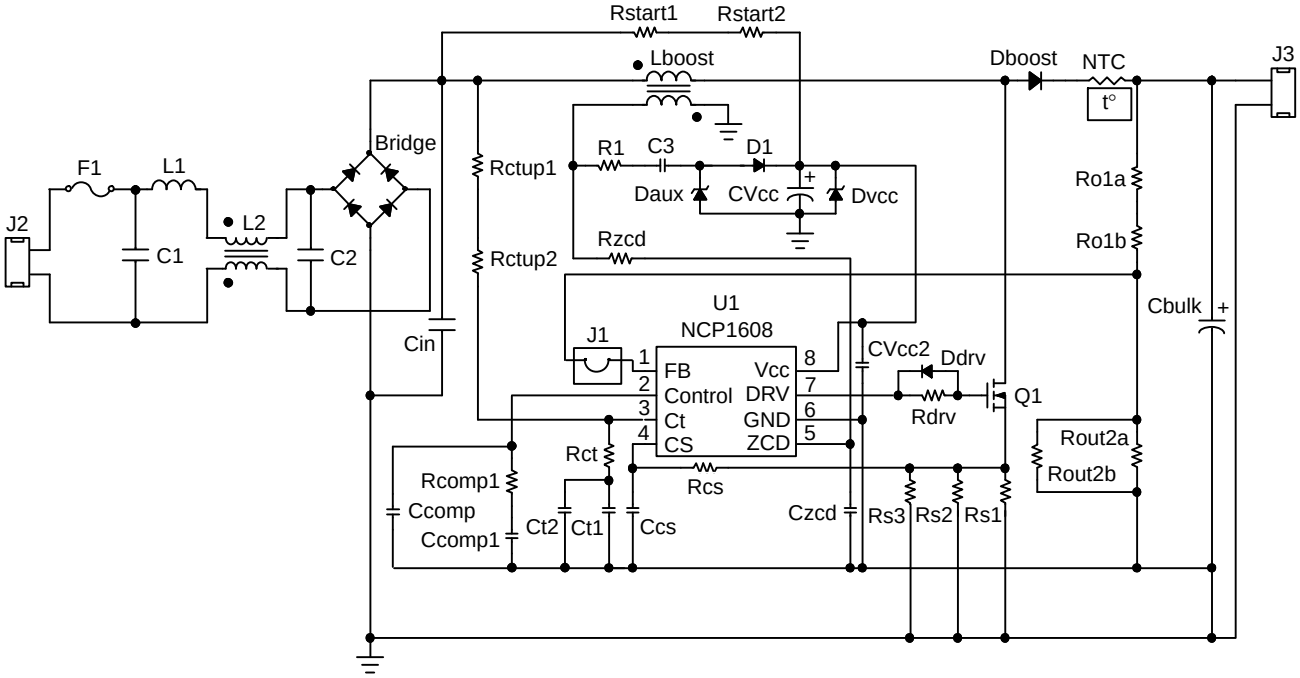


Figure 47. Application Schematic

BOOST DESIGN EQUATIONS Components are identified in Figure 1

Input rms Current	$$Iac = \frac{P_{out}}{\eta \cdot Vac}$$	η (the efficiency of only the PFC stage) is generally in the range of 90 − 95%. Vac is the rms ac line input voltage.
Inductor Peak Current	$$I_{L(peak)} = \frac{\sqrt{2} \cdot 2 \cdot P_{out}}{\eta \cdot Vac}$$	The maximum inductor peak current occurs at the minimum line input voltage and maximum output power.
Inductor Value	$$L \le \frac{Vac^2 \cdot \left(\frac{V_{out}}{\sqrt{2}} - Vac\right) \cdot \eta}{\sqrt{2} \cdot V_{out} \cdot P_{out} \cdot f_{SW(MIN)}}$$	$f_{SW(MIN)}$ is the minimum desired switching frequency. The maximum L is calculated at both the minimum line input voltage and maximum line input voltage.
On Time	$$t_{on} = \frac{2 \cdot L \cdot P_{out}}{\eta \cdot Vac^2}$$	The maximum on time occurs at the minimum line input voltage and maximum output power.
Off Time	$$t_{off} = \frac{t_{on}}{\frac{V_{out}}{Vac \cdot \lvert\sin\theta\rvert \cdot \sqrt{2}} - 1}$$	The off time is a maximum at the peak of the ac line voltage and approaches zero at the ac line zero crossings. Theta (θ) represents the angle of the ac line voltage.
Switching Frequency	$$f_{SW} = \frac{Vac^2 \cdot \eta}{2 \cdot L \cdot P_{out}} \cdot \left(1 - \frac{Vac \cdot \lvert\sin\theta\rvert \cdot \sqrt{2}}{V_{out}}\right)$$	
On Time Capacitor	$$Ct \ge \frac{2 \cdot P_{out} \cdot L_{MAX} \cdot I_{charge}}{\eta \cdot Vac_{LL}^2 \cdot V_{Ct(MAX)}}$$	Where Vac_{LL} is the minimum line input voltage and L_{MAX} is the maximum inductor value. I_{charge} and $V_{Ct(MAX)}$ are shown in the specification table.
Inductor Turns to ZCD Turns Ratio	$$N_B : N_{ZCD} \le \frac{V_{out} - \left(\sqrt{2} \cdot Vac_{HL}\right)}{V_{ZCD(ARM)}}$$	Where Vac_{HL} is the maximum line input voltage. $V_{ZCD(ARM)}$ is shown in the specification table.
Resistor from ZCD Winding to the ZCD pin	$$R_{ZCD} \ge \frac{\sqrt{2} \cdot Vac_{HL}}{I_{ZCD(MAX)} \cdot (N_B : N_{ZCD})}$$	Where $I_{ZCD(MAX)}$ is maximum rated current for the ZCD pin (10 mA).
Output Voltage and Output Divider	$$V_{out} = V_{REF} \cdot \left(R_{out1} \cdot \frac{R_{out2} + R_{FB}}{R_{out2} \cdot R_{FB}} + 1\right)$$ $$R_{out1} = \frac{V_{out}}{I_{bias(out)}}$$ $$R_{out2} = \frac{R_{out1} \cdot R_{FB}}{R_{FB} \cdot \left(\frac{V_{out}}{V_{REF}} - 1\right) - R_{out1}}$$	Where V_{REF} is the internal reference voltage and R_{FB} is the pull−down resistor used for FPP. V_{REF} and R_{FB} are shown in the specification table. $I_{bias(out)}$ is the bias current of the output voltage divider.
Output Voltage OVP Detection and Recovery	$$V_{out(OVP)} = \frac{V_{OVP}}{V_{REF}} \cdot V_{REF} \cdot \left(R_{out1} \cdot \frac{R_{out2} + R_{FB}}{R_{out2} \cdot R_{FB}} + 1\right)$$ $$V_{out(OVPL)} = \left(\left(\frac{V_{OVP}}{V_{REF}} \cdot V_{REF}\right) - V_{OVP(HYS)}\right) \cdot \left(R_{out1} \cdot \frac{R_{out2} + R_{FB}}{R_{out2} \cdot R_{FB}} + 1\right)$$	V_{OVP}/V_{REF} and $V_{OVP(HYS)}$ are shown in the specification table.
Output Voltage Ripple and Output Capacitor Value	$$V_{ripple(peak-peak)} < 2 \cdot \left(V_{out(OVP)} - V_{out}\right)$$ $$C_{bulk} \ge \frac{P_{out}}{2 \cdot \pi \cdot V_{ripple(peak-peak)} \cdot f_{line} \cdot V_{out}}$$	Where f_{line} is the ac line frequency and $V_{ripple(peak-peak)}$ is the peak-to-peak output voltage ripple. Use f_{line} = 47 Hz for universal input worst case.
Output Capacitor rms Current	$$I_{C(RMS)} = \sqrt{\frac{\sqrt{2} \cdot 32 \cdot P_{out}^2}{9 \cdot \pi \cdot Vac \cdot V_{out} \cdot \eta^2} - I_{load(RMS)}^2}$$	Where $I_{load(RMS)}$ is the rms load current.

BOOST DESIGN EQUATIONS Components are identified in Figure 1 (Continued)

Output Voltage UVP Detection	$V_{out(UVP)} = V_{UVP} \cdot \left(R_{out1} \cdot \frac{R_{out2} + R_{FB}}{R_{out2} \cdot R_{FB}} + 1 \right)$	V_{UVP} is shown in the specification table.
Inductor rms Current	$I_{L(RMS)} = \frac{2 \cdot P_{out}}{\sqrt{3} \cdot Vac \cdot \eta}$	
Output Diode rms Current	$I_{D(RMS)} = \frac{4}{3} \cdot \sqrt{\frac{\sqrt{2} \cdot 2}{\pi}} \cdot \frac{P_{out}}{\eta \cdot \sqrt{Vac \cdot V_{out}}}$	
MOSFET rms Current	$I_{M(RMS)} = \frac{2}{\sqrt{3}} \cdot \left(\frac{P_{out}}{\eta \cdot Vac} \right) \cdot \sqrt{1 - \left(\frac{\sqrt{2} \cdot 8 \cdot Vac}{3 \cdot \pi \cdot V_{out}} \right)}$	
Current Sense Resistor	$R_{sense} = \frac{V_{ILIM}}{I_{L(peak)}}$ $P_{R_{sense}} = I_{M(RMS)}^{2} \cdot R_{sense}$	V_{ILIM} is shown in the specification table.
Type 1 Compensation	$C_{COMP} = \frac{gm}{2 \cdot \pi \cdot f_{CROSS}}$	Where f_{CROSS} is the crossover frequency and is typically less than 20 Hz. gm is shown in the specification table.

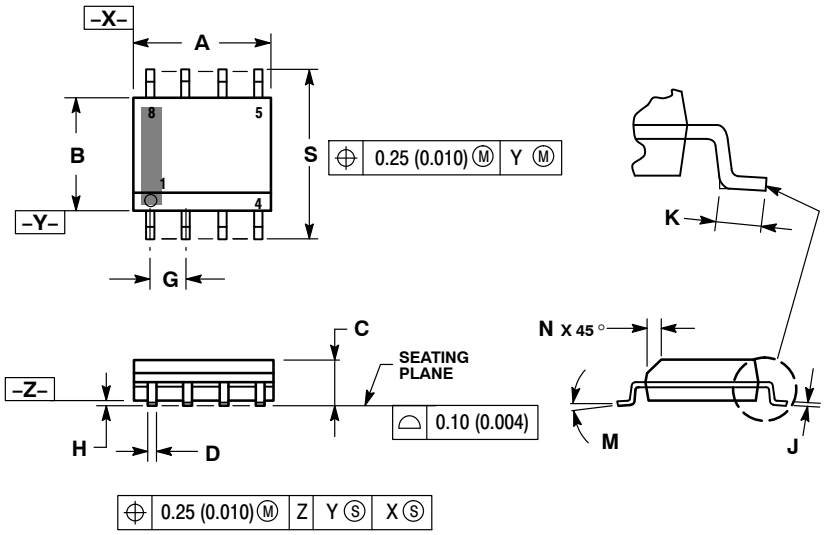
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

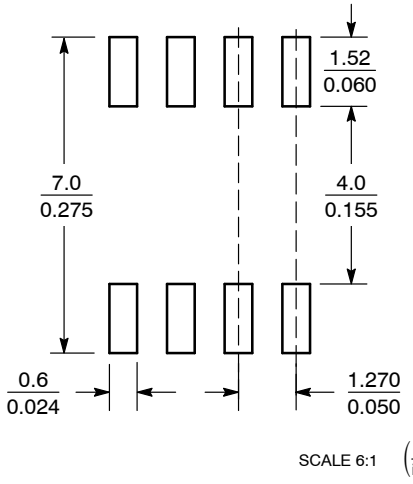
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

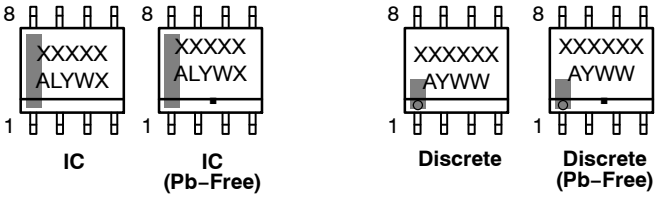
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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DESCRIPTION:	**SOIC−8 NB**		**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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