TEXAS INSTRUMENTS

TPD4E004

SLVS729B –FEBRUARY 2008–REVISED MARCH 2016 2016

TPD4E004 4-Channel ESD-Protection Array For High-Speed Data Interfaces

1 Features

- IEC 61000-4-2 ESD Protection
  - ±8-kV IEC 61000-4-2 Contact Discharge
  - ±12-kV IEC 61000-4-2 Air-Gap Discharge
- ANSI/ESDA/JEDEC JS-001
  - ±15-kV Human Body Model (HBM)
- Low 1.6-pF Input Capacitance
- 0.9-V to 5.5-V Supply Voltage Range
- 4-Channel Device
- Space-Saving SON (DRY) Package

2 Applications

- USB
- Ethernet
- FireWire
- Videos
- Cell Phones
- SVGA Video Connections
- Glucose Meters

3 Description

The TPD4E004 is a low-capacitance transient voltage suppression (TVS) device. TPD4E004 is designed to protect sensitive electronics attached to communication lines from electrostatic discharge (ESD). Each of the four channels consists of a pair of diodes that steer ESD current pulses to V_{CC} or GND. The TPD4E004 protects against ESD pulses up to ±15-kV Human-Body Model (HBM) and, as specified in IEC 61000-4-2, ±8-kV contact discharge and ±12-kV air-gap Discharge. This device has 1.6-pF of capacitance per channel, making it ideal for use in high-speed data IO interfaces.

The TPD4E004 is a quad-ESD structure designed for USB, ethernet, and other high-speed applications.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPD4E004	SON (6)	1.45 mm × 1.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Application Schematic

Table of Contents

4   Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (February 2008) to Revision B   **Page**

5   Pin Configuration and Functions

DRY Package
6-Pin SON
Top View

```
        ┌─────────────┐
IO1  │ [1]     [6] │  V_CC
IO2  │ [2]     [5] │  IO4
GND  │ [3]     [4] │  IO3
        └─────────────┘
```
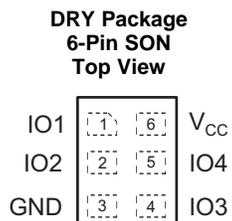
Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	IO1	IO	ESD-protected channel
2	IO2	IO	ESD-protected channel
3	GND	GND	Ground
4	IO3	IO	ESD-protected channel
5	IO4	IO	ESD-protected channel
6	V_{CC}	PWR	Power-supply input

Product Folder Links: *TPD4E004*

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) [1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.3	5.5	V
V_{IO}	Input/output voltage		–0.3	V_{CC} + 0.3	V
	Bump temperature (soldering)	Infrared (15 s)		220	°C
		Vapor phase (60 s)		215	
	Lead temperature (soldering, 10 s)			300	°C
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001		±15000	V
		IEC 61000-4-2	Contact Discharge	±8000	
			Air-Gap Discharge	±12000	

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
T_A	Operating free-air temperature	–40	85	°C
V_{CC}	Operating voltage for pin V_{CC}	0.9	5.5	V
V_{IO}	Operating voltage for pins IO1, IO2, IO3, and IO4	0	Minimum of: (5.8, V_{CC})	V

6.4 Thermal Information

THERMAL METRIC[1]		TPD4E004	UNIT
		DRY (SON)	
		6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	414.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	258.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	251.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	70.6	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	248.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

Product Folder Links: *TPD4E004*

6.5 Electrical Characteristics

V_{CC} = 0.9 V to 5.5 V, T_A = T_{MIN} to T_{MAX} (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP[(1)]	MAX	UNIT
V_{CC}	Supply voltage		0.9		5.5	V
I_{CC}	Supply current				500	nA
V_F	Diode forward voltage	I_F = 1 mA		0.8		V
I_I	Channel leakage current			±1		nA
V_{BR}	Break-down voltage	I_I = 10 µA	6		8	V
$C_{I/O}$	Channel input capacitance	V_{CC} = 5 V, Bias of V_{CC}/2, f = 10 MHz		1.6	2	pF

(1)   Typical values are at V_{CC} = 5 V and T_A = 25°C.

6.6 Typical Characteristics
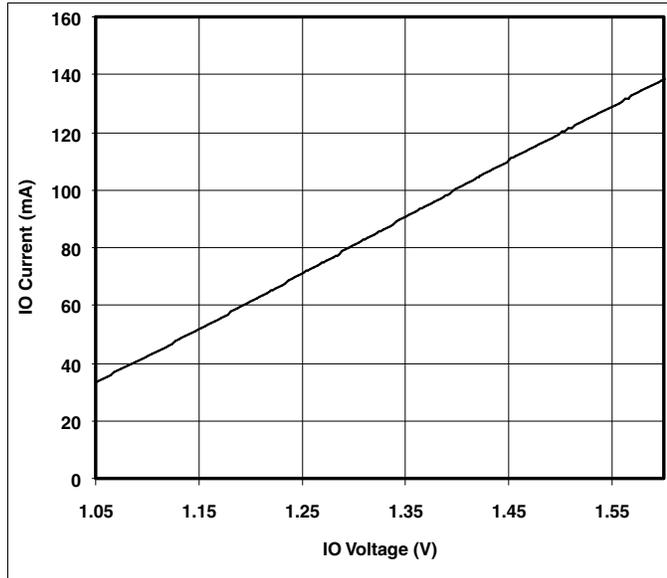
Figure 1. Forward Diode Voltage (Upper Clamp Diode)
(V_{CC} = 0 V, DC Sweep Across the IO Pin)
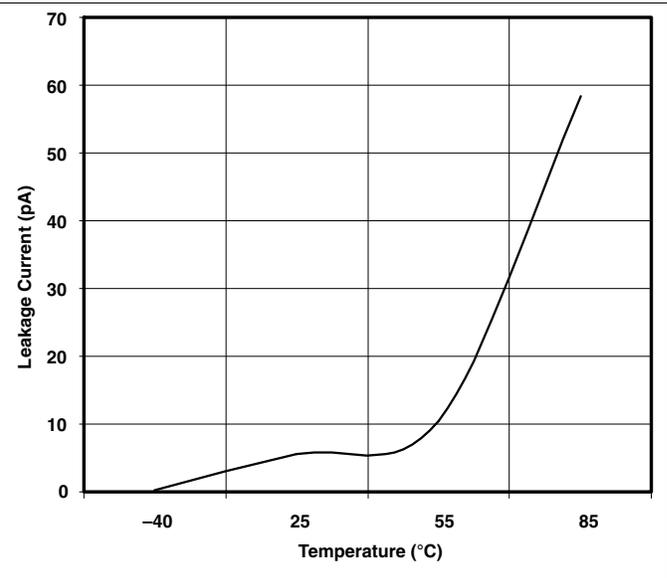
Figure 2. Leakage Current vs Temperature (V_{IO} = 2.5 V)
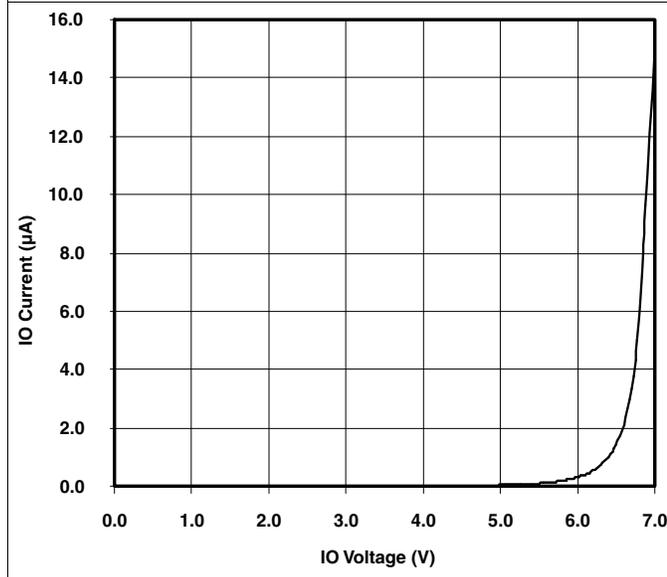
Figure 3. Reverse Diode Curve Current IO to Gnd
(V_{CC} = Open)
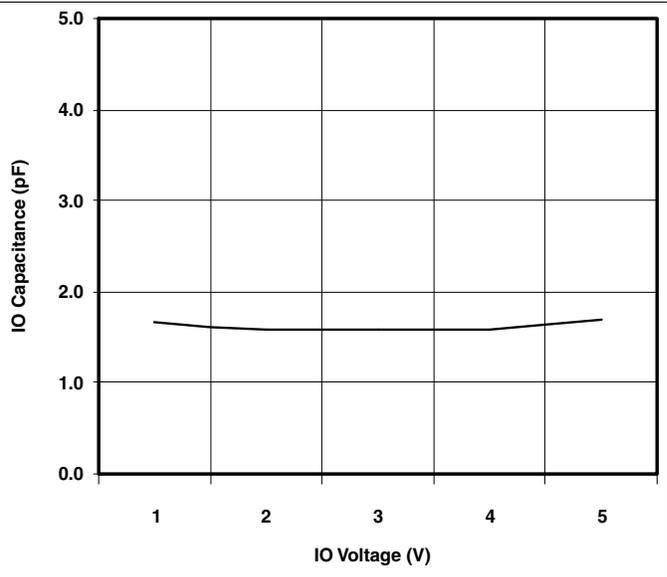
Figure 4. IO Capacitance vs Input Voltage
(V_{CC} = 5 V)

Product Folder Links: *TPD4E004*

7 Detailed Description

7.1 Overview

The TPD4E004 is a four-channel TVS protection diode array. The TPD4E004 is rated to dissipate contact ESD strikes of ±8-kV contact and ±12-kV air-gap, meeting Level 4 as specified in the IEC 61000-4-2 international standard. This device has a 1.6-pF IO capacitance per channel, making it ideal for use in high-speed data IO interfaces.

7.2 Functional Block Diagram
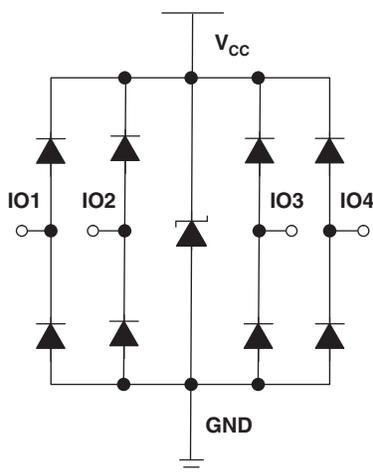
7.3 Feature Description

TPD4E004 is a TVS which provides ESD protection for up to four channels, withstanding up to ±8-kV contact and ±12-kV air-gap ESD per IEC 61000-4-2. The monolithic technology yields exceptionally small variations in capacitance between any IO pin of TPD4E004. The small footprint is ideal for applications where space-saving designs are important.

7.4 Device Functional Modes

The TPD4E004 device is a passive integrated circuit that triggers when voltages are above V_{BR} or below the diodes V_F of approximately –0.3 V. During ESD events, voltages as high as ±8-kV contact and ±12-kV air-gap ESD can be directed to ground via the internal diodes. Once the voltages on the protected line fall below the trigger levels of TPD4E004 (usually within 10's of nano-seconds) the device reverts back to its high-impedance state.

Product Folder Links: *TPD4E004*

8 Application and Implementation

> **NOTE**
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

TPD4E004 is a diode array type TVS which is typically used to provide a path to ground for dissipating ESD events on hi-speed signal lines between a human interface connector and a system. As the current from ESD passes through the TVS, only a small voltage drop is present across the diode. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage, V_{CLAMP}, to a tolerable level for the protected IC.

8.2 Typical Application
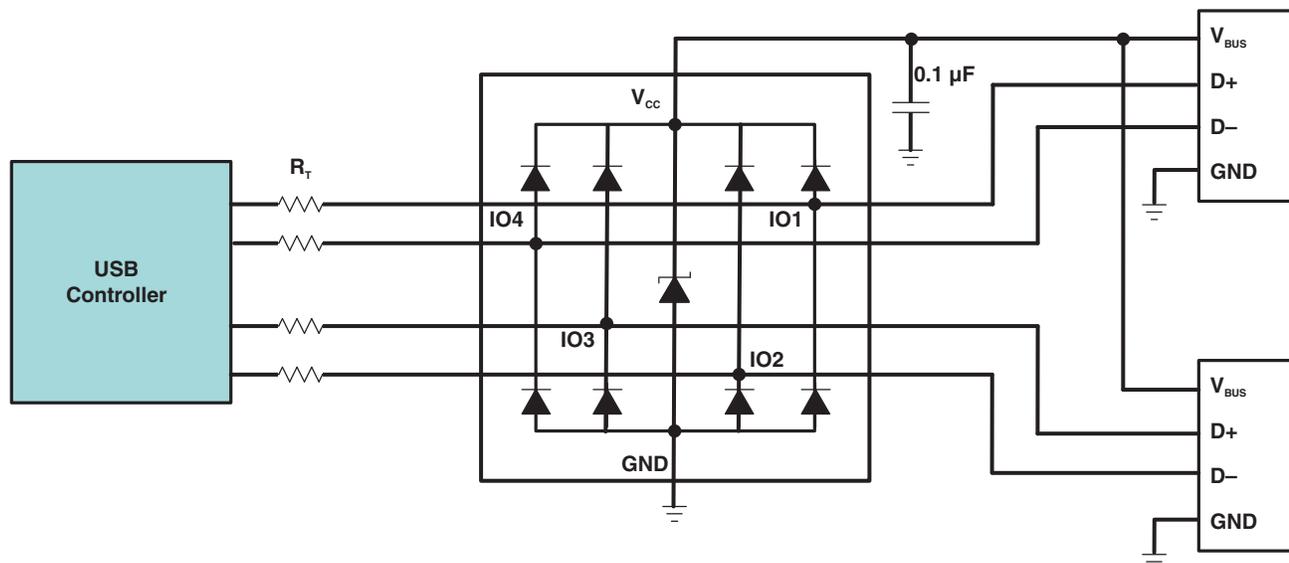
Figure 5. Application Schematic

8.2.1 Design Requirements

For this design example, a single TPD4E004 is used to protect all the pins of two USB2.0 connectors. Table 1 lists the design parameters for the USB application.

Table 1. Design Parameters

DESIGN PARAMETER	VALUE
Signal range on IO1, IO2, IO3, and IO4	0 V to 3.6 V
Signal voltage range on V_{CC}	0 V to 5.5 V
Operating Frequency	240 MHz

8.2.2 Detailed Design Procedure

When placed near the USB connectors, the TPD4E004 ESD solution offers little or no signal distortion during normal operation due to low IO capacitance and ultra-low leakage current specifications. The TPD4E004 ensures that the core circuitry is protected and the system is functioning properly in the event of an ESD strike. For proper operation, see the the following layout and design guidelines should be followed:

 1. Place the TPD4E004 solution close to the connectors. This allows the TPD4E004 to take away the energy

Product Folder Links: *TPD4E004*

associated with ESD strike before it reaches the internal circuitry of the system board.

2. Place a 0.1-µF capacitor very close to the V_{CC} pin. This limits any momentary voltage surge at the IO pin during the ESD strike event.

3. Ensure that there is enough metallization for the V_{CC} and GND loop. During normal operation, the TPD4E004 consumes nA leakage current. But during the ESD event, V_{CC} and GND may see 15-A to 30-A of current, depending on the ESD level. Sufficient current path enables safe discharge of all the energy associated with the ESD strike.

4. Leave the unused IO pins floating. In this example of protecting two USB ports, none of the IO pins will be left unused.

5. The V_{CC} pin can be connected in two different ways:

   (a) If the V_{CC} pin is connected to the system power supply, the TPD4E004 works as a transient suppressor for any signal swing above V_{CC} + V_F. A 0.1-µF capacitor on the device V_{CC} pin is recommended for ESD bypass.

   (b) If the V_{CC} pin is not connected to the system power supply, the TPD4E004 can tolerate higher signal swing in the range up to 5.8 V. Please note that a 0.1-µF capacitor is still recommended at the V_{CC} pin for ESD bypass.

8.2.3 Application Curves

Figure 6 is a capture of the voltage clamping waveform of TPD4E004 during an +8kV Contact IEC 61000-4-2 ESD strike.
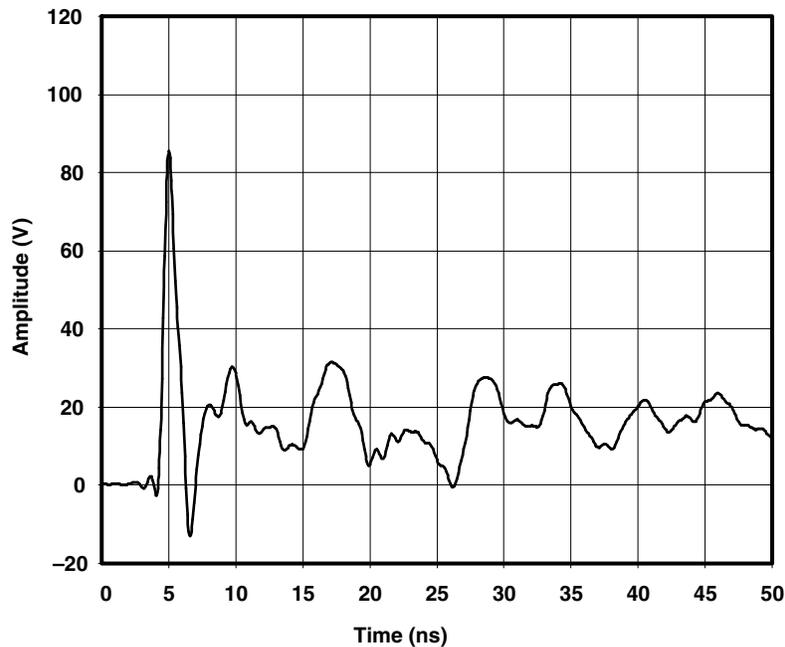
Figure 6. IEC ESD Clamping Waveforms +8-KV Contact

9 Power Supply Recommendations

This device is a passive ESD protection device so there is no need to power it. Make sure that the maximum voltage specifications for each pin are not violated.

10 Layout

10.1 Layout Guidelines

- The optimum placement is as close to the connector as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer needs to minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the connector.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.

10.2 Layout Example
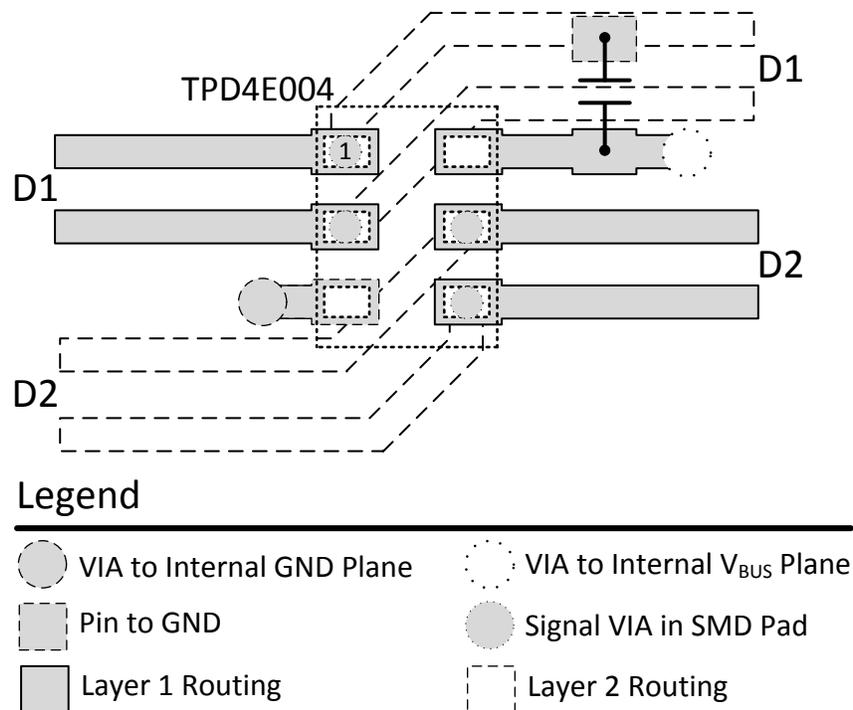
Figure 7. TPD4E004 Layout Example

Product Folder Links: *TPD4E004*

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *Reading and Understanding an ESD Protection Datasheet*, SLLA305
- *ESD Protection Layout Guide*, SLVA680

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
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11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPD4E004DRYR	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2P	Samples
TPD4E004DRYRG4	ACTIVE	SON	DRY	6	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2P	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers
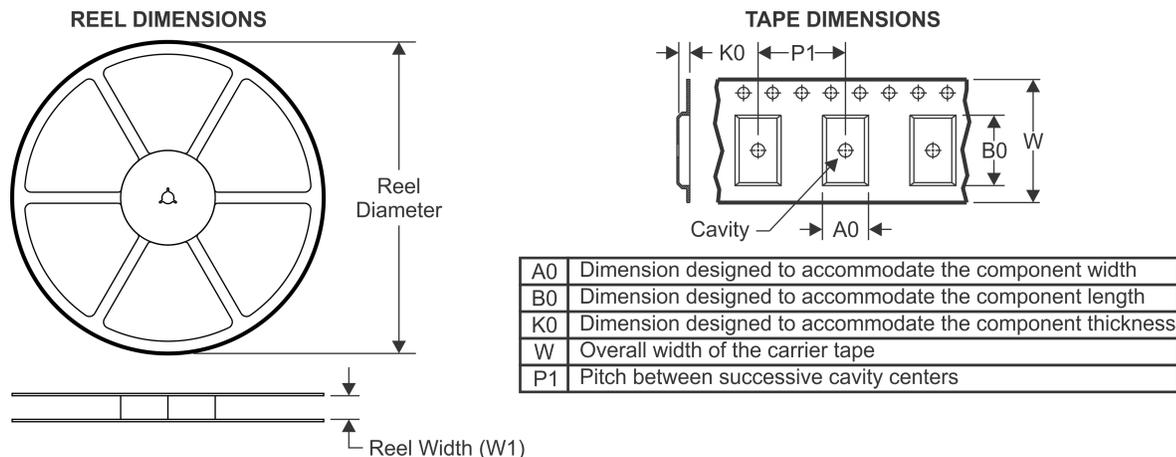
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE
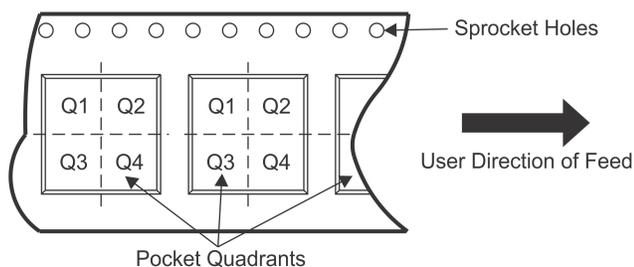
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD4E004DRYR	SON	DRY	6	5000	180.0	9.5	1.2	1.65	0.7	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS
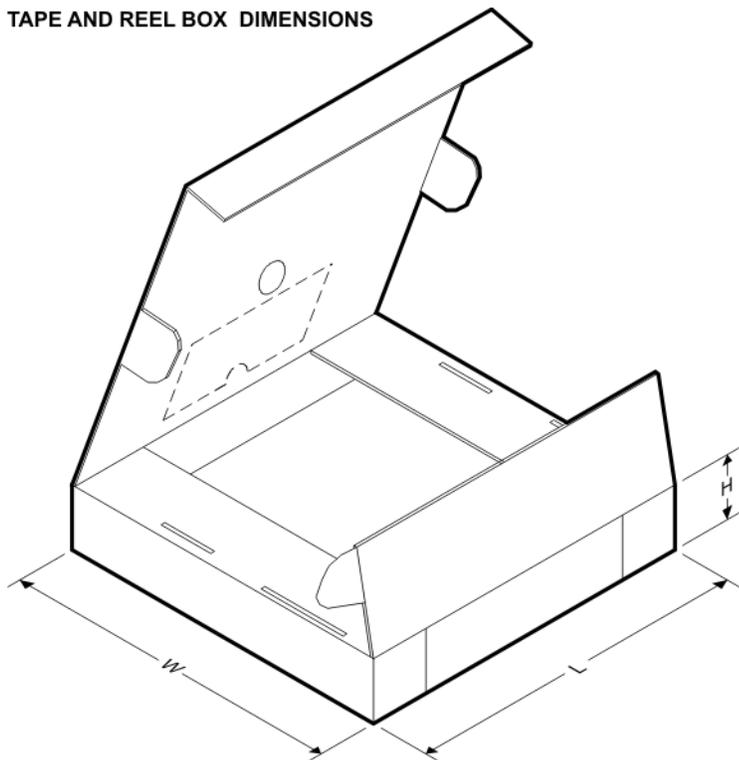
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD4E004DRYR	SON	DRY	6	5000	189.0	185.0	36.0

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4207181/G

TEXAS
INSTRUMENTS

B | 1.05 / 0.95 | A

PIN 1 INDEX AREA

1.5 / 1.4

0.6 MAX

C

0.05 / 0.00

SEATING PLANE

0.08 C

3X 0.6

SYMM

(0.05) TYP

(0.127) TYP

3 | | 4

4X 0.5

2X 1

SYMM

1 | | 6

0.4 / 0.3

6X 0.25 / 0.15

0.1 (M) C A B
0.05 (M) C

PIN 1 ID (OPTIONAL)

5X 0.35 / 0.25

4222894/A 01/2018
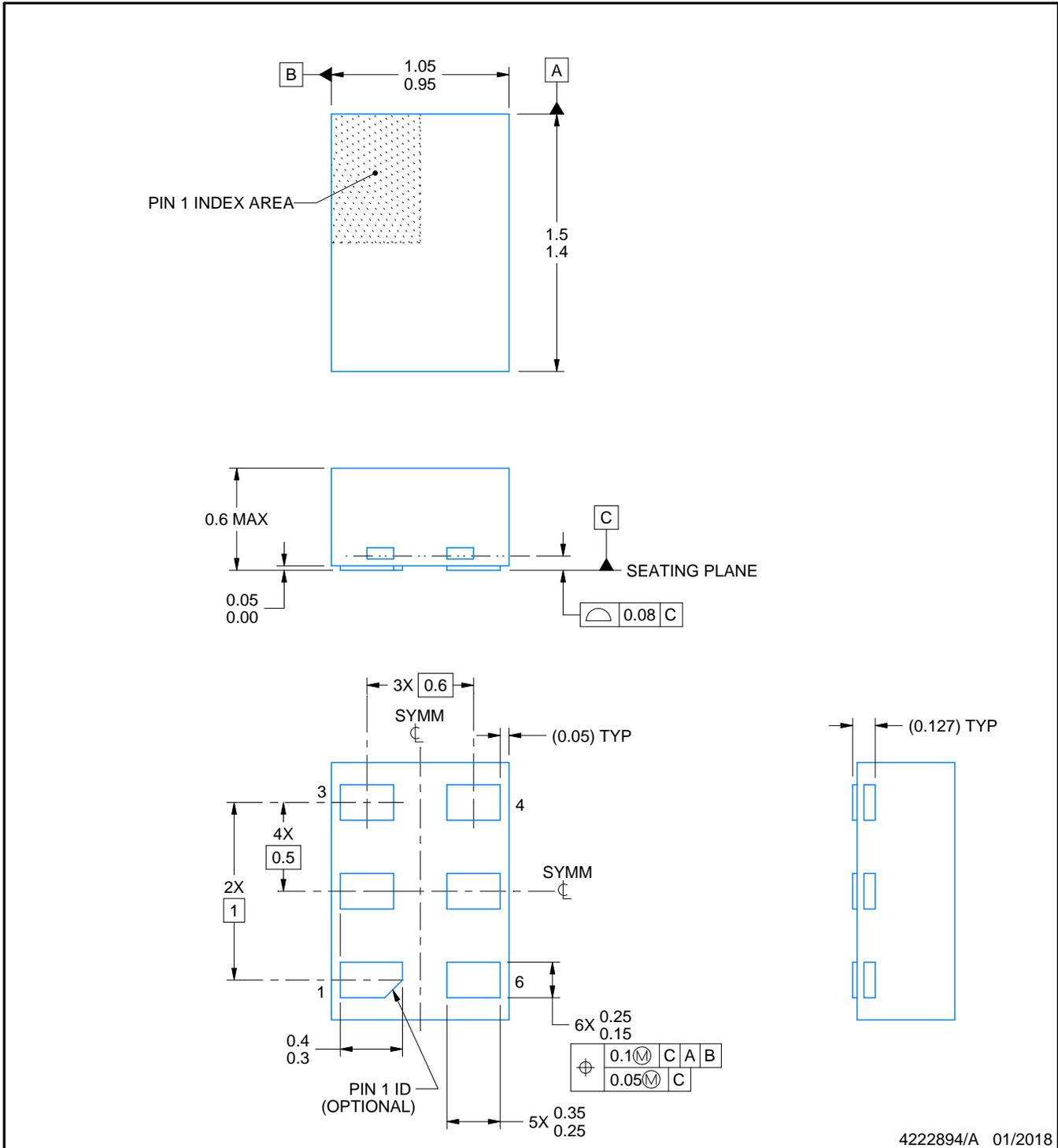
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

SYMM

(0.35)

5X (0.3)

1

6

6X (0.2)

SYMM

4X (0.5)

3

4

(R0.05) TYP

(0.6)
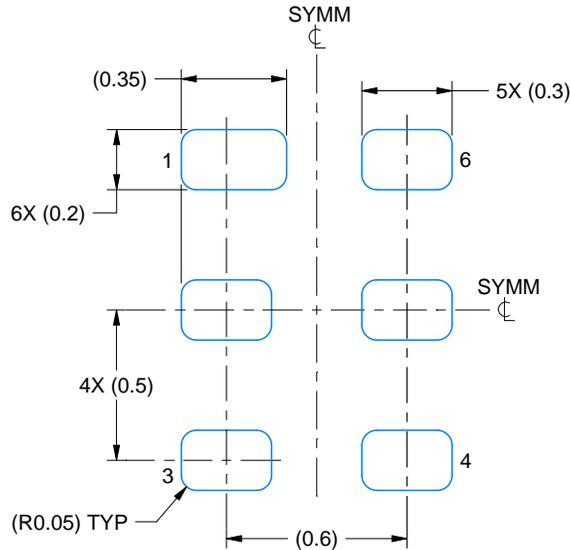
LAND PATTERN EXAMPLE
1:1 RATIO WITH PKG SOLDER PADS
EXPOSED METAL SHOWN
SCALE:40X

0.05 MAX
ALL AROUND

0.05 MIN
ALL AROUND

EXPOSED
METAL

EXPOSED
METAL

SOLDER MASK
OPENING

METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

**NON SOLDER MASK
DEFINED**

**SOLDER MASK
DEFINED
(PREFERRED)**
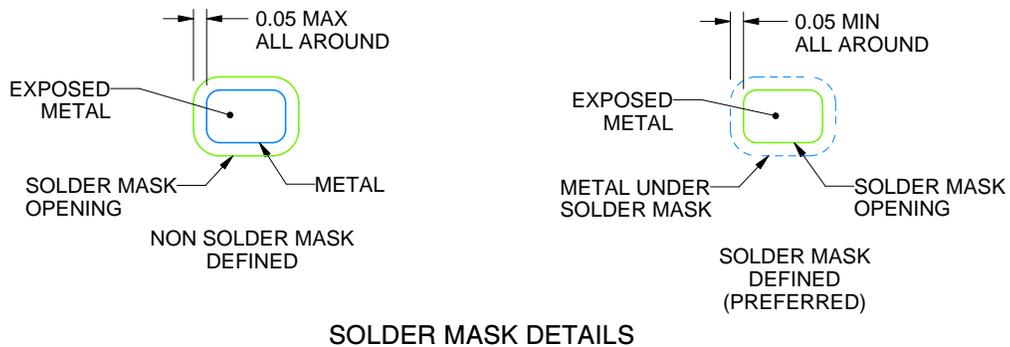
SOLDER MASK DETAILS

4222894/A   01/2018

NOTES: (continued)

3. For more information, see QFN/SON PCB application report in literature No. SLUA271 (www.ti.com/lit/slua271).

SYMM

(0.35)

5X (0.3)

1

6

6X (0.2)

SYMM

4X (0.5)

3

4

(R0.05) TYP

(0.6)
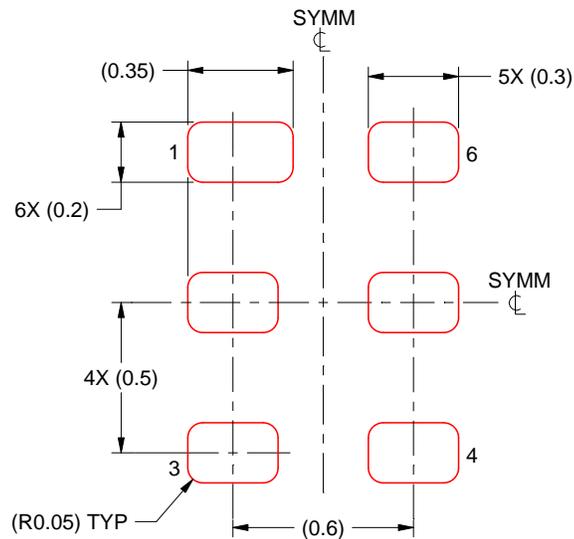
SOLDER PASTE EXAMPLE
BASED ON 0.075 - 0.1 mm THICK STENCIL
SCALE:40X

4222894/A   01/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
   design recommendations.

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