

Hex Level Shifter for TTL to CMOS or CMOS to CMOS

MC14504B

The MC14504B is a hex non-inverting level shifter using CMOS technology. The level shifter will shift a TTL signal to CMOS logic levels for any CMOS supply voltage between 5 and 15 volts. A control input also allows interface from CMOS to CMOS at one logic level to another logic level: Either up or down level translating is accomplished by selection of power supply levels V_{DD} and V_{CC} . The V_{CC} level sets the input signal levels while V_{DD} selects the output voltage levels.

Features

- UP Translates from a Low to a High Voltage or DOWN Translates from a High to a Low Voltage
- Input Threshold Can Be Shifted for TTL Compatibility
- No Sequencing Required on Power Supplies or Inputs for Power Up or Power Down
- 3 to 18 Vdc Operation for V_{DD} and V_{CC}
- Diode Protected Inputs to V_{SS}
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

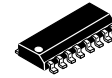
Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage Range	-0.5 to +18.0	V
V_{DD}	DC Supply Voltage Range	-0.5 to +18.0	V
V_{in}	Input Voltage Range (DC or Transient)	-0.5 to +18.0	V
V_{out}	Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 1)	500	mW
T_A	Ambient Temperature Range	-55 to +125	°C
T_{stg}	Storage Temperature Range	-65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

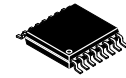
1. Temperature Derating: "D/DW" Packages: -7.0 mW/°C From 65°C To 125°C.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

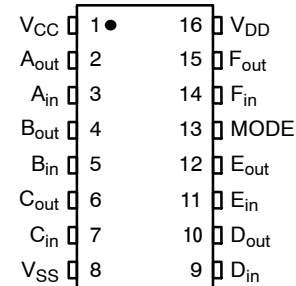


SOIC-16
D SUFFIX
CASE 751B

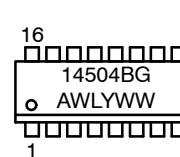


TSSOP-16
DT SUFFIX
CASE 948F

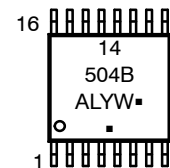
PIN ASSIGNMENT



MARKING DIAGRAMS



SOIC-16



TSSOP-16

- A = Assembly Location
- WL, L = Wafer Lot
- Y = Year
- WW, W = Work Week
- G or ■ = Pb-Free Indicator

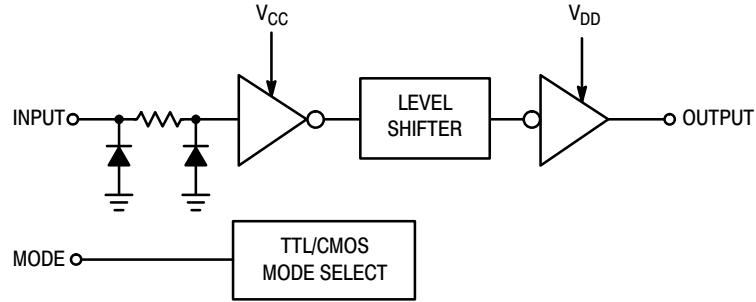
(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

MC14504B

LOGIC DIAGRAM



Mode Select	Input Logic Levels	Output Logic Levels
1 (V_{CC})	TTL	CMOS
0 (V_{SS})	CMOS	CMOS

1/6 of package shown.

ORDERING INFORMATION

Device	Package	Shipping [†]
MC14504BDG	SOIC-16 (Pb-Free)	48 Units / Rail
MC14504BDR2G	SOIC-16 (Pb-Free)	2500 Units / Tape & Reel
NLV14504BDR2G*		
MC14504BDTG	TSSOP-16 (Pb-Free)	96 Units / Rail
MC14504BDTR2G	TSSOP-16 (Pb-Free)	2500 Units / Tape & Reel
NLV14504BDTR2G*		

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

MC14504B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{CC} Vdc	V _{DD} Vdc	- 55°C		25°C			125°C		Unit
				Min	Max	Min	Typ (Note 2)	Max	Min	Max	
Output Voltage V _{in} = 0 V V _{in} = V _{CC}	"0" Level V _{OL}	-	5.0	-	0.05	-	0	0.05	-	0.05	Vdc
		-	10	-	0.05	-	0	0.05	-	0.05	
		-	15	-	0.05	-	0	0.05	-	0.05	
	"1" Level V _{OH}	-	5.0	4.95	-	4.95	5.0	-	4.95	-	Vdc
		-	10	9.95	-	9.95	10	-	9.95	-	
		-	15	14.95	-	14.95	15	-	14.95	-	
Input Voltage (V _{OL} = 1.0 Vdc) TTL-CMOS (V _{OL} = 1.5 Vdc) TTL-CMOS (V _{OL} = 1.0 Vdc) CMOS-CMOS (V _{OL} = 1.5 Vdc) CMOS-CMOS (V _{OL} = 1.5 Vdc) CMOS-CMOS	"0" Level V _{IL}	5.0	10	-	0.8	-	1.3	0.8	-	0.8	Vdc
		5.0	15	-	0.8	-	1.3	0.8	-	0.8	
		5.0	10	-	1.5	-	2.25	1.5	-	1.4	
		5.0	15	-	1.5	-	2.25	1.5	-	1.5	
		10	15	-	3.0	-	4.5	3.0	-	2.9	
		10	15	-	3.0	-	4.5	3.0	-	2.9	
Input Voltage (V _{OH} = 9.0 Vdc) TTL-CMOS (V _{OH} = 13.5 Vdc) TTL-CMOS (V _{OH} = 9.0 Vdc) CMOS-CMOS (V _{OH} = 13.5 Vdc) CMOS-CMOS (V _{OH} = 13.5 Vdc) CMOS-CMOS	"1" Level V _{IH}	5.0	10	2.0	-	2.0	1.5	-	2.0	-	Vdc
		5.0	15	2.0	-	2.0	1.5	-	2.0	-	
		5.0	10	3.6	-	3.5	2.75	-	3.5	-	
		5.0	15	3.6	-	3.5	2.75	-	3.5	-	
		10	15	7.1	-	7.0	5.5	-	7.0	-	
		10	15	7.1	-	7.0	5.5	-	7.0	-	
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	Source I _{OH}	-	5.0	-3.0	-	-2.4	-4.2	-	-1.7	-	mAdc
		-	5.0	-0.64	-	-0.51	-0.88	-	-0.36	-	
		-	10	-1.6	-	-1.3	-2.25	-	-0.9	-	
		-	15	-4.2	-	-3.4	-8.8	-	-2.4	-	
	Sink I _{OL}	-	5.0	0.64	-	0.51	0.88	-	0.36	-	mAdc
		-	10	1.6	-	1.3	2.25	-	0.9	-	
Output Current	I _{in}	-	15	-	±0.1	-	±0.00001	±0.1	-	±1.0	μAdc
Input Capacitance (V _{in} = 0)	C _{in}	-	-	-	-	-	5.0	7.5	-	-	pF
Quiescent Current (Per Package) CMOS-CMOS Mode	I _{DD} or I _{CC}	-	5.0	-	0.05	-	0.0005	0.05	-	1.5	μAdc
		-	10	-	0.10	-	0.0010	0.10	-	3.0	
		-	15	-	0.20	-	0.0015	0.20	-	6.0	
Quiescent Current (Per Package) TTL-CMOS Mode	I _{DD}	5.0	5.0	-	0.5	-	0.0005	0.5	-	3.8	μAdc
		5.0	10	-	1.0	-	0.0010	1.0	-	7.5	
		5.0	15	-	2.0	-	0.0015	2.0	-	15	
Quiescent Current (Per Package) TTL-CMOS Mode	I _{CC}	5.0	5.0	-	5.0	-	2.5	5.0	-	6.0	mAdc
		5.0	10	-	5.0	-	2.5	5.0	-	6.0	
		5.0	15	-	5.0	-	2.5	5.0	-	6.0	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

MC14504B

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	Shifting Mode	V _{CC} Vdc	V _{DD} Vdc	Limits			Unit
					Min	Typ (Note 3)	Max	
Propagation Delay, High to Low	t _{PHL}	TTL – CMOS V _{DD} > V _{CC}	5.0	10	–	140	280	ns
			5.0	15	–	140	280	
		CMOS – CMOS V _{DD} > V _{CC}	5.0	10	–	120	240	
			5.0	15	–	120	240	
		CMOS – CMOS V _{CC} > V _{DD}	10	5.0	–	185	370	
			15	5.0	–	185	370	
CMOS – CMOS V _{CC} > V _{DD}	15	10	–	175	350			
	15	10	–	175	350			
Propagation Delay, Low to High	t _{PLH}	TTL – CMOS V _{DD} > V _{CC}	5.0	10	–	170	340	ns
			5.0	15	–	160	320	
		CMOS – CMOS V _{DD} > V _{CC}	5.0	10	–	170	340	
			5.0	15	–	170	340	
		CMOS – CMOS V _{CC} > V _{DD}	10	5.0	–	100	200	
			15	5.0	–	100	200	
CMOS – CMOS V _{CC} > V _{DD}	15	5.0	–	275	550			
	15	5.0	–	275	550			
CMOS – CMOS V _{CC} > V _{DD}	15	10	–	145	290			
	15	10	–	145	290			
Output Rise and Fall Time	t _{TLH} , t _{THL}	ALL	–	5.0	–	100	200	ns
			–	10	–	50	100	
			–	15	–	40	80	

3. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

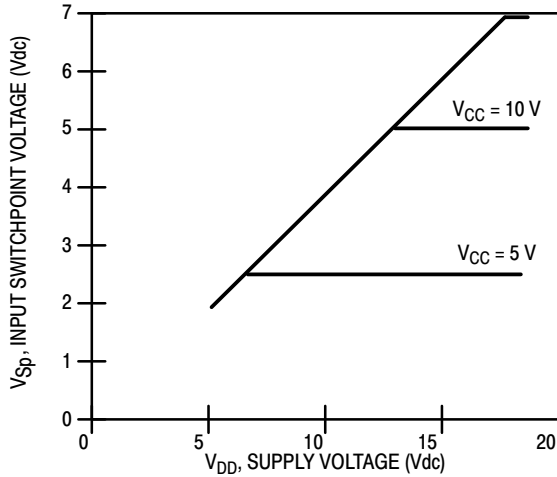


Figure 1. Input Switchpoint CMOS to CMOS Mode

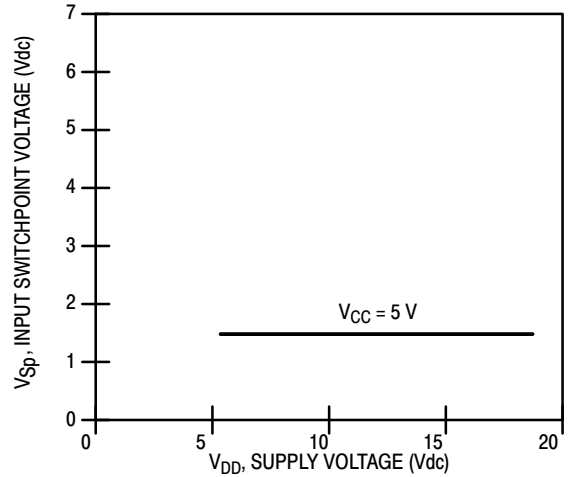


Figure 2. Input Switchpoint TTL to CMOS Mode

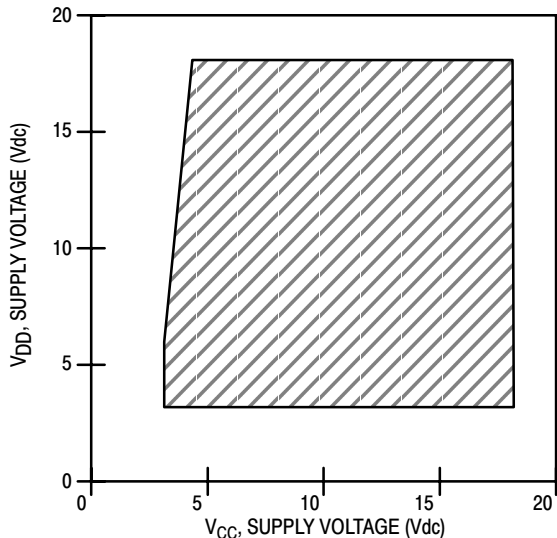


Figure 3. Operating Boundary CMOS to CMOS Mode

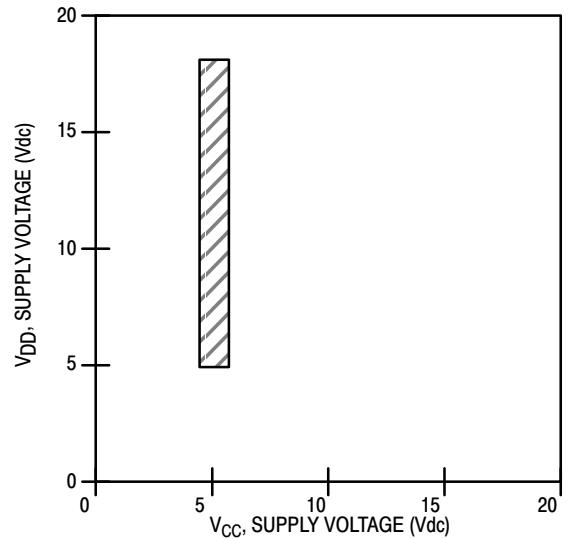


Figure 4. Operating Boundary TTL to CMOS Mode

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 1:1

SOIC-16 CASE 751B-05 ISSUE K

DATE 29 DEC 2006



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

- | | | | |
|--|--|--|--|
| <p>STYLE 1:</p> <p>PIN 1. COLLECTOR</p> <p>2. BASE</p> <p>3. EMITTER</p> <p>4. NO CONNECTION</p> <p>5. EMITTER</p> <p>6. BASE</p> <p>7. COLLECTOR</p> <p>8. COLLECTOR</p> <p>9. BASE</p> <p>10. EMITTER</p> <p>11. NO CONNECTION</p> <p>12. EMITTER</p> <p>13. BASE</p> <p>14. COLLECTOR</p> <p>15. EMITTER</p> <p>16. COLLECTOR</p> | <p>STYLE 2:</p> <p>PIN 1. CATHODE</p> <p>2. ANODE</p> <p>3. NO CONNECTION</p> <p>4. CATHODE</p> <p>5. CATHODE</p> <p>6. NO CONNECTION</p> <p>7. ANODE</p> <p>8. CATHODE</p> <p>9. CATHODE</p> <p>10. ANODE</p> <p>11. NO CONNECTION</p> <p>12. CATHODE</p> <p>13. CATHODE</p> <p>14. NO CONNECTION</p> <p>15. ANODE</p> <p>16. CATHODE</p> | <p>STYLE 3:</p> <p>PIN 1. COLLECTOR, DYE #1</p> <p>2. BASE, #1</p> <p>3. EMITTER, #1</p> <p>4. COLLECTOR, #1</p> <p>5. COLLECTOR, #2</p> <p>6. BASE, #2</p> <p>7. EMITTER, #2</p> <p>8. COLLECTOR, #2</p> <p>9. COLLECTOR, #3</p> <p>10. BASE, #3</p> <p>11. EMITTER, #3</p> <p>12. COLLECTOR, #3</p> <p>13. COLLECTOR, #4</p> <p>14. BASE, #4</p> <p>15. EMITTER, #4</p> <p>16. COLLECTOR, #4</p> | <p>STYLE 4:</p> <p>PIN 1. COLLECTOR, DYE #1</p> <p>2. COLLECTOR, #1</p> <p>3. COLLECTOR, #2</p> <p>4. COLLECTOR, #2</p> <p>5. COLLECTOR, #3</p> <p>6. COLLECTOR, #3</p> <p>7. COLLECTOR, #4</p> <p>8. COLLECTOR, #4</p> <p>9. BASE, #4</p> <p>10. EMITTER, #4</p> <p>11. BASE, #3</p> <p>12. EMITTER, #3</p> <p>13. BASE, #2</p> <p>14. EMITTER, #2</p> <p>15. BASE, #1</p> <p>16. EMITTER, #1</p> |
| <p>STYLE 5:</p> <p>PIN 1. DRAIN, DYE #1</p> <p>2. DRAIN, #1</p> <p>3. DRAIN, #2</p> <p>4. DRAIN, #2</p> <p>5. DRAIN, #3</p> <p>6. DRAIN, #3</p> <p>7. DRAIN, #4</p> <p>8. DRAIN, #4</p> <p>9. GATE, #4</p> <p>10. SOURCE, #4</p> <p>11. GATE, #3</p> <p>12. SOURCE, #3</p> <p>13. GATE, #2</p> <p>14. SOURCE, #2</p> <p>15. GATE, #1</p> <p>16. SOURCE, #1</p> | <p>STYLE 6:</p> <p>PIN 1. CATHODE</p> <p>2. CATHODE</p> <p>3. CATHODE</p> <p>4. CATHODE</p> <p>5. CATHODE</p> <p>6. CATHODE</p> <p>7. CATHODE</p> <p>8. CATHODE</p> <p>9. ANODE</p> <p>10. ANODE</p> <p>11. ANODE</p> <p>12. ANODE</p> <p>13. ANODE</p> <p>14. ANODE</p> <p>15. ANODE</p> <p>16. ANODE</p> | <p>STYLE 7:</p> <p>PIN 1. SOURCE N-CH</p> <p>2. COMMON DRAIN (OUTPUT)</p> <p>3. COMMON DRAIN (OUTPUT)</p> <p>4. GATE P-CH</p> <p>5. COMMON DRAIN (OUTPUT)</p> <p>6. COMMON DRAIN (OUTPUT)</p> <p>7. COMMON DRAIN (OUTPUT)</p> <p>8. SOURCE P-CH</p> <p>9. SOURCE P-CH</p> <p>10. COMMON DRAIN (OUTPUT)</p> <p>11. COMMON DRAIN (OUTPUT)</p> <p>12. COMMON DRAIN (OUTPUT)</p> <p>13. GATE N-CH</p> <p>14. COMMON DRAIN (OUTPUT)</p> <p>15. COMMON DRAIN (OUTPUT)</p> <p>16. SOURCE N-CH</p> | |

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

DOCUMENT NUMBER:	98ASB42566B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC-16	PAGE 1 OF 1

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®



TSSOP-16
CASE 948F-01
ISSUE B

DATE 19 OCT 2006



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

SOLDERING FOOTPRINT



GENERIC MARKING DIAGRAM*



- XXXX = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- G or ■ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present.

DOCUMENT NUMBER:	98ASH70247A	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	TSSOP-16	PAGE 1 OF 1

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Email Requests to: orderlit@onsemi.com

onsemi Website: www.onsemi.com

TECHNICAL SUPPORT

North American Technical Support:

Voice Mail: 1 800-282-9855 Toll Free USA/Canada

Phone: 011 421 33 790 2910

Europe, Middle East and Africa Technical Support:

Phone: 00421 33 790 2910

For additional information, please contact your local Sales Representative