

MJE13005G

SWITCHMODE™ Series NPN Silicon Power Transistors

These devices are designed for high-voltage, high-speed power switching inductive circuits where fall time is critical. They are particularly suited for 115 and 220 V SWITCHMODE applications such as Switching Regulator's, Inverters, Motor Controls, Solenoid/Relay drivers and Deflection circuits.

Features

- $V_{CEO(sus)}$ 400 V
- Reverse Bias SOA with Inductive Loads @ $T_C = 100^\circ\text{C}$
- Inductive Switching Matrix 2 to 4 A, 25 and 100°C t_c @ 3A, 100°C is 180 ns (Typ)
- 700 V Blocking Capability
- SOA and Switching Applications Information
- These Devices are Pb-Free and are RoHS Compliant*

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO(sus)}$	400	Vdc
Collector-Emitter Voltage	V_{CEV}	700	Vdc
Emitter-Base Voltage	V_{EBO}	9	Vdc
Collector Current – Continuous – Peak (Note 1)	I_C I_{CM}	4 8	Adc
Base Current – Continuous – Peak (Note 1)	I_B I_{BM}	2 4	Adc
Emitter Current – Continuous – Peak (Note 1)	I_E I_{EM}	6 12	Adc
Total Device Dissipation @ $T_A = 25^\circ\text{C}$ Derate above 25°C	P_D	2 0.016	W W/ $^\circ\text{C}$
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	75 0.6	W W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	-65 to +150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.67	$^\circ\text{C}/\text{W}$
Maximum Lead Temperature for Soldering Purposes 1/8" from Case for 5 Seconds	T_L	275	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Pulse Test: Pulse Width = 5 ms, Duty Cycle \leq 10%.

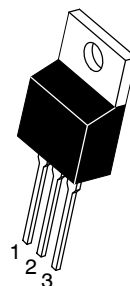
*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



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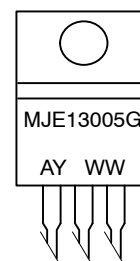
<http://onsemi.com>

**4 AMPERE
NPN SILICON
POWER TRANSISTOR
400 VOLTS – 75 WATTS**



TO-220AB
CASE 221A-09
STYLE 1

MARKING DIAGRAM



A = Assembly Location
Y = Year
WW = Work Week
G = Pb-Free Package

ORDERING INFORMATION

Device	Package	Shipping
MJE13005G	TO-220 (Pb-Free)	50 Units / Rail

MJE13005G

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS (Note 2)					
Collector–Emitter Sustaining Voltage ($I_C = 10\text{ mA}$, $I_B = 0$)	$V_{CEO(sus)}$	400	–	–	Vdc
Collector Cutoff Current ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$) ($V_{CEV} = \text{Rated Value}$, $V_{BE(off)} = 1.5\text{ Vdc}$, $T_C = 100^\circ\text{C}$)	I_{CEV}	–	–	1 5	mAdc
Emitter Cutoff Current ($V_{EB} = 9\text{ Vdc}$, $I_C = 0$)	I_{EBO}	–	–	1	mAdc

SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased	$I_{S/b}$	–	See Figure 11		
Clamped Inductive SOA with Base Reverse Biased	RBSOA	–	See Figure 12		

ON CHARACTERISTICS

 (Note 2)

DC Current Gain ($I_C = 1\text{ Adc}$, $V_{CE} = 5\text{ Vdc}$) ($I_C = 2\text{ Adc}$, $V_{CE} = 5\text{ Vdc}$)	h_{FE}	10 8	– –	60 40	–
Collector–Emitter Saturation Voltage ($I_C = 1\text{ Adc}$, $I_B = 0.2\text{ Adc}$) ($I_C = 2\text{ Adc}$, $I_B = 0.5\text{ Adc}$) ($I_C = 4\text{ Adc}$, $I_B = 1\text{ Adc}$) ($I_C = 2\text{ Adc}$, $I_B = 0.5\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{CE(sat)}$	– – – –	– – – –	0.5 0.6 1 1	Vdc
Base–Emitter Saturation Voltage ($I_C = 1\text{ Adc}$, $I_B = 0.2\text{ Adc}$) ($I_C = 2\text{ Adc}$, $I_B = 0.5\text{ Adc}$) ($I_C = 2\text{ Adc}$, $I_B = 0.5\text{ Adc}$, $T_C = 100^\circ\text{C}$)	$V_{BE(sat)}$	– – –	– – –	1.2 1.6 1.5	Vdc

DYNAMIC CHARACTERISTICS

Current–Gain – Bandwidth Product ($I_C = 500\text{ mAdc}$, $V_{CE} = 10\text{ Vdc}$, $f = 1\text{ MHz}$)	f_T	4	–	–	MHz
Output Capacitance ($V_{CB} = 10\text{ Vdc}$, $I_E = 0$, $f = 0.1\text{ MHz}$)	C_{ob}	–	65	–	pF

SWITCHING CHARACTERISTICS

Resistive Load (Table 2)					
Delay Time	$(V_{CC} = 125\text{ Vdc}$, $I_C = 2\text{ A}$, $I_{B1} = I_{B2} = 0.4\text{ A}$, $t_p = 25\text{ }\mu\text{s}$, Duty Cycle $\leq 1\%$)	t_d	–	0.025	0.1 μs
Rise Time		t_r	–	0.3	0.7 μs
Storage Time		t_s	–	1.7	4 μs
Fall Time		t_f	–	0.4	0.9 μs
Inductive Load, Clamped (Table 2, Figure 13)					
Voltage Storage Time	$(I_C = 2\text{ A}$, $V_{clamp} = 300\text{ Vdc}$, $I_{B1} = 0.4\text{ A}$, $V_{BE(off)} = 5\text{ Vdc}$, $T_C = 100^\circ\text{C}$)	t_{sv}	–	0.9	4 μs
Crossover Time		t_c	–	0.32	0.9 μs
Fall Time		t_{fi}	–	0.16	– μs

2. Pulse Test: Pulse Width = 300 μs , Duty Cycle = 2%.

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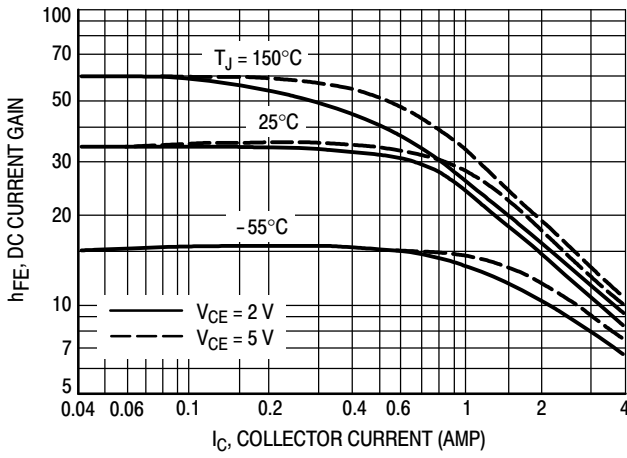


Figure 1. DC Current Gain

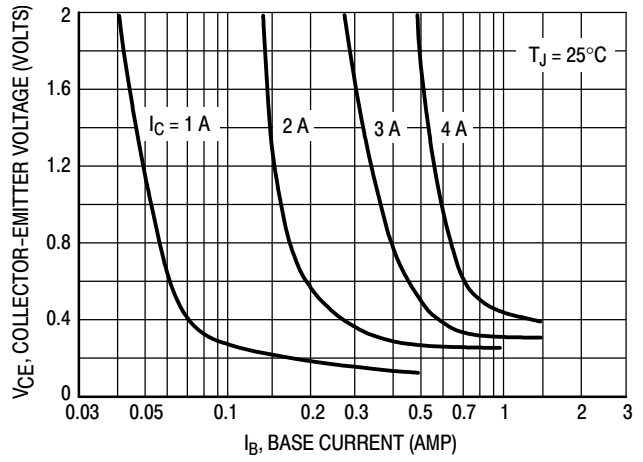


Figure 2. Collector Saturation Region

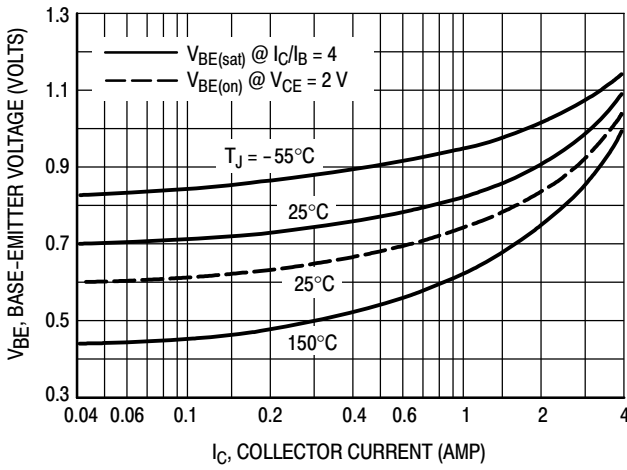


Figure 3. Base-Emitter Voltage

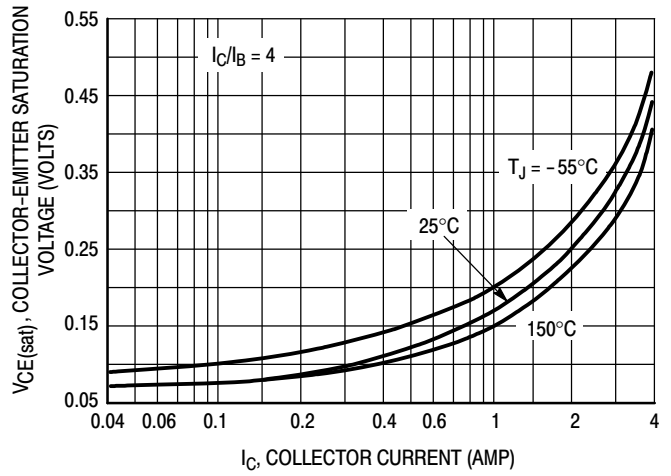


Figure 4. Collector-Emitter Saturation Voltage

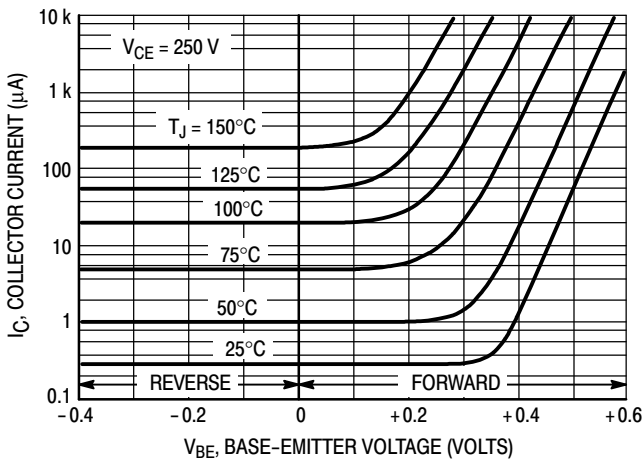


Figure 5. Collector Cutoff Region

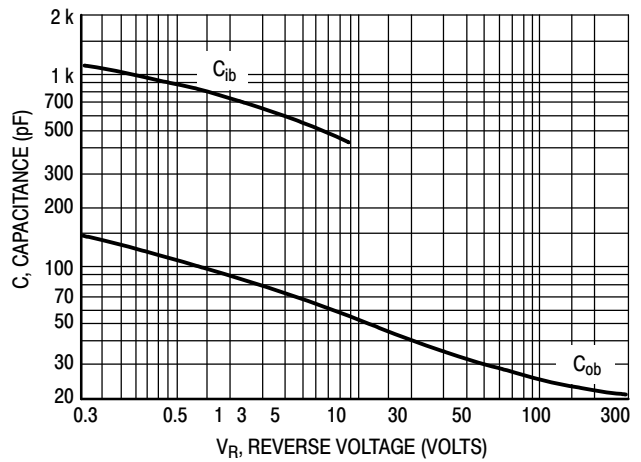


Figure 6. Capacitance

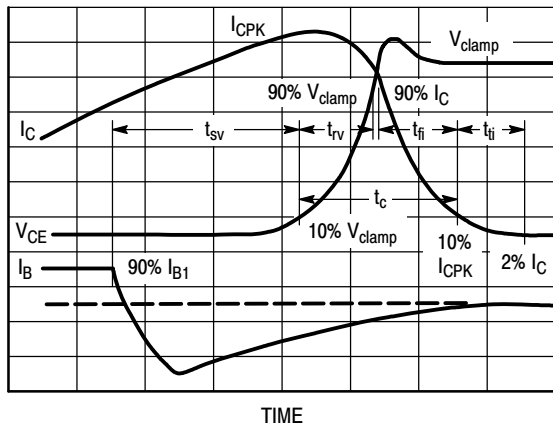


Figure 7. Inductive Switching Measurements

Table 1. Typical Inductive Switching Performance

I _C AMP	T _C °C	t _{sv} ns	t _{rv} ns	t _{fi} ns	t _{ti} ns	t _c ns
2	25	600	70	100	80	180
	100	900	110	240	130	320
3	25	650	60	140	60	200
	100	950	100	330	100	350
4	25	550	70	160	100	220
	100	850	110	350	160	390

NOTE: All Data recorded in the inductive Switching Circuit In Table 2.

SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}

t_{rv} = Voltage Rise Time, 10–90% V_{clamp}

t_{fi} = Current Fall Time, 90–10% I_C

t_{ti} = Current Tail, 10–2% I_C

t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN–222:

$$P_{SWT} = 1/2 V_{CC}I_C(t_c)f$$

In general, t_{rv} + t_{fi} ≈ t_c. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a “SWITCHMODE” transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING PERFORMANCE

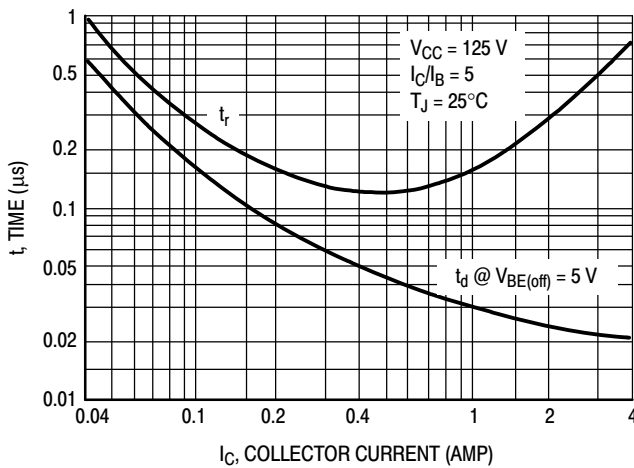


Figure 8. Turn-On Time

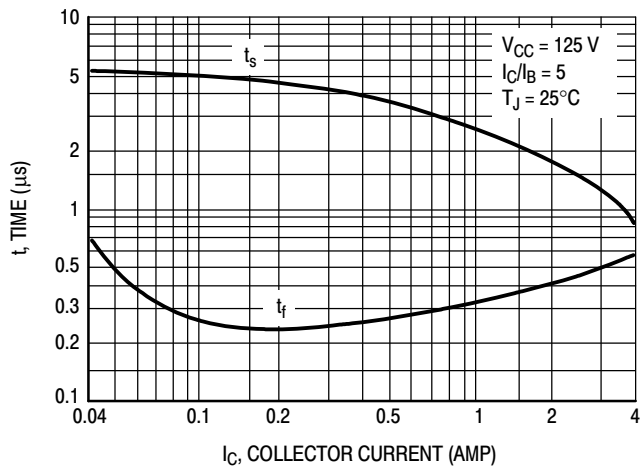


Figure 9. Turn-Off Time

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Table 2. Test Conditions for Dynamic Performance

REVERSE BIAS SAFE OPERATING AREA AND INDUCTIVE SWITCHING		RESISTIVE SWITCHING	
TEST CIRCUITS	<p>DUTY CYCLE $\leq 10\%$ $t_r, t_f \leq 10 \text{ ns}$</p> <p>NOTE PW and V_{CC} Adjusted for Desired I_C R_B Adjusted for Desired I_{B1}</p>		
CIRCUIT VALUES	Coil Data: Ferroxcube Core #6656 Full Bobbin (~16 Turns) #16 GAP for 200 $\mu\text{H}/20 \text{ A}$ $L_{\text{coil}} = 200 \mu\text{H}$	$V_{CC} = 20 \text{ V}$ $V_{\text{clamp}} = 300 \text{ Vdc}$	$V_{CC} = 125 \text{ V}$ $R_C = 62 \Omega$ $D1 = 1\text{N}5820 \text{ or Equiv.}$ $R_B = 22 \Omega$
TEST WAVEFORMS	<p>t_1 ADJUSTED TO OBTAIN I_C</p> $t_1 \approx \frac{L_{\text{coil}} (I_{C(pk)})}{V_{CC}}$ $t_2 \approx \frac{L_{\text{coil}} (I_{C(pk)})}{V_{\text{clamp}}}$ <p>Test Equipment Scope-Tektronics 475 or Equivalent</p>	<p>$t_r, t_f < 10 \text{ ns}$ Duty Cycle = 1.0% R_B and R_C adjusted for desired I_B and I_C</p>	

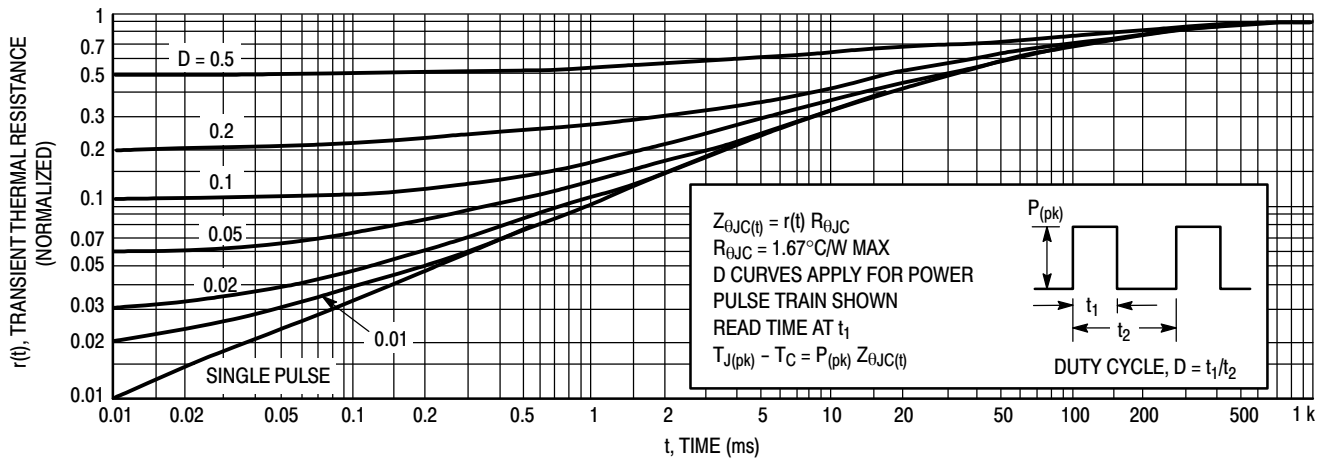


Figure 10. Typical Thermal Response [$Z_{\theta JC}(t)$]

SAFE OPERATING AREA INFORMATION

The Safe Operating Area Figures 11 and 12 are specified ratings for these devices under the test conditions shown.

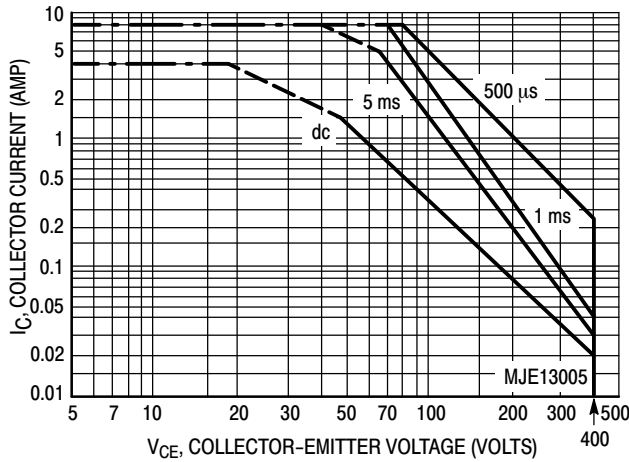


Figure 11. Forward Bias Safe Operating Area

FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 11 is based on $T_C = 25^\circ\text{C}$; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25^\circ\text{C}$. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 11 may be found at any case temperature by using the appropriate curve on Figure 13.

$T_{J(pk)}$ may be calculated from the data in Figure 10. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

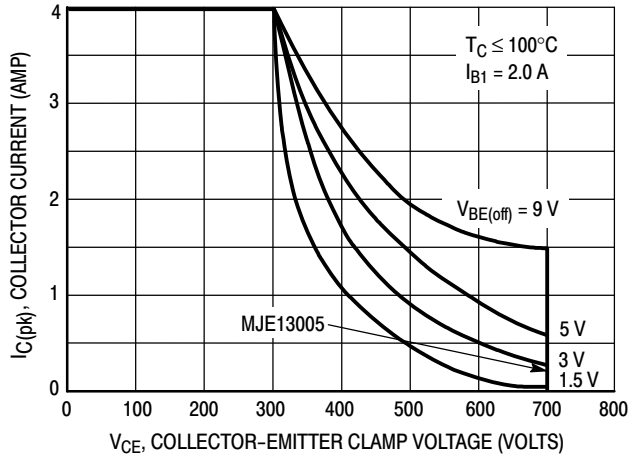


Figure 12. Reverse Bias Switching Safe Operating Area

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current conditions during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 12 gives the complete RBSOA characteristics.

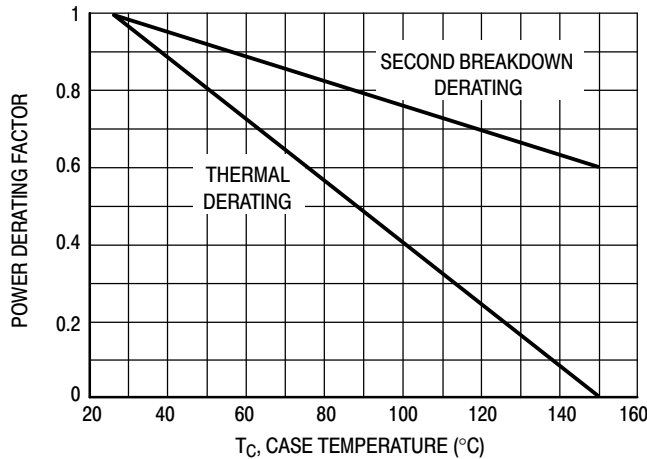


Figure 13. Forward Bias Power Derating

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