STS17NH3LL

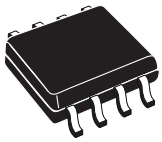
N-channel 30 V - 0.004 Ω - 17 A - SO-8
STripFET™ Power MOSFET for DC-DC conversion

Features

Type	V_{DSS}	$R_{DS(on)}$	I_D
STS17NH3LL	30V	<0.0057Ω	17A(1)

1. This value is rated according to Rthj-pcb

- Optimal $R_{DS(on)}$ x Qg trade-off @ 4.5 V
- Conduction losses reduced
- Improved junction-case thermal resistance
- Low threshold device



SO-8

Applications

- Switching application

Description

This device utilizes the latest advanced design rules of ST's proprietary STripFET™ technology. This process coupled to unique metallization techniques realizes the most advanced low voltage Power MOSFET in SO-8 ever produced.

Figure 1. Internal schematic diagram

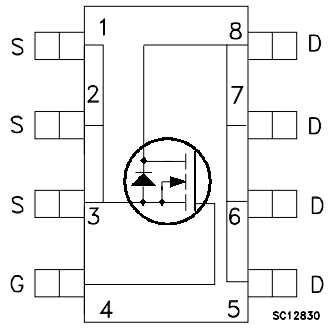


Table 1. Device summary

Order code	Marking	Package	Packaging
STS17NH3LL	17H3LL-	SO-8	Tape & reel

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	30	V
V_{GS}	Gate- source voltage	± 16	V
I_D (1)	Drain current (continuous) at T_C = 25°C	17	A
I_D	Drain current (continuous) at T_C = 100°C	10.6	A
I_{DM} (2)	Drain current (pulsed)	68	A
P_{tot} (1)	Total dissipation at T_C = 25°C	2.7	W
T_{stg}	Storage temperature	-55 to 150	°C
Tj	Operating junction temperature		

1. This value is rated according to Rthj-pcb
2. Pulse width limited by safe operating area

Table 3. Thermal resistance

Symbol	Parameter	Value	Unit
Rthj-pcb(1)	Thermal resistance junction-ambient max	47	°C/W

1. When mounted on 1inch² FR-4 board, 2oz of Cu and t< 10sec

Table 4. Avalanche data

Symbol	Parameter	Value	Unit
I_{AV}	Not-repetitive avalanche current	7.5	A
E_{AS}	Single pulse avalanche energy (starting Tj=25°C, Id=I_{AV})	150	mJ

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250 µA, V_{GS} = 0	30			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating V_{DS} = Max rating @125°C			1 10	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 16 V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	1			V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D = 8.5 A V_{GS} = 4.5 V, I_D = 8.5 A		0.004 0.005	0.0057 0.0075	Ω Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS}=25 V, f=1 MHz V_{GS} = 0		1810 565 41		pF pF pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD}=15 V, I_D=17 A V_{GS}=4.5 V *(see Figure 14)*		18 4.8 5.3	24	nC nC nC
R_G	Gate input resistance	f=1 MHz Gate DC Bias = 0 Test signal level = 20 mV open drain	0.5	1.5	3	Ω

Table 7. Switching times

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	V_{DD} = 15 V, I_D = 8.5 A R_G = 4.7 Ω, V_{GS} = 10 V *(see Figure 16)*		8 65		ns ns
$t_{d(off)}$ t_f	Turn-off delay time Fall time	V_{DD} = 15 V, I_D = 8.5 A R_G = 4.7 Ω, V_{GS} = 10 V *(see Figure 16)*		38 20		ns ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
I_{SD} I_{SDM}	Source-drain current Source-drain current (pulsed)				17 68	A A
V_{SD} (1)	Forward on voltage	I_{SD} = 17 A, V_{GS} = 0			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 17 A, di/dt = 100 A/µs V_{DD} = 15 V, T_j = 25°C *(see Figure 15)*		22 32 1.9		ns nC A

1. Pulsed: pulse duration=300µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

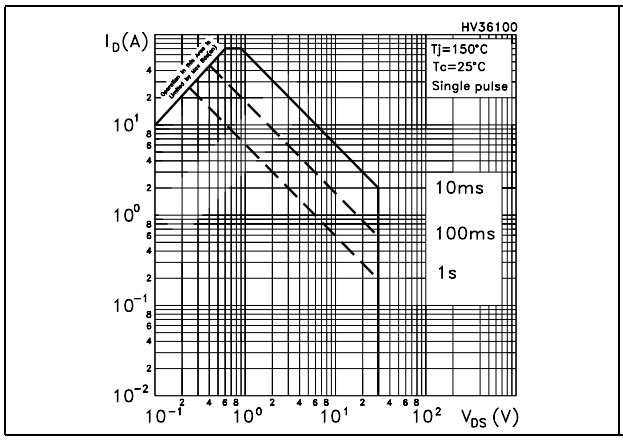


Figure 3. Thermal impedance

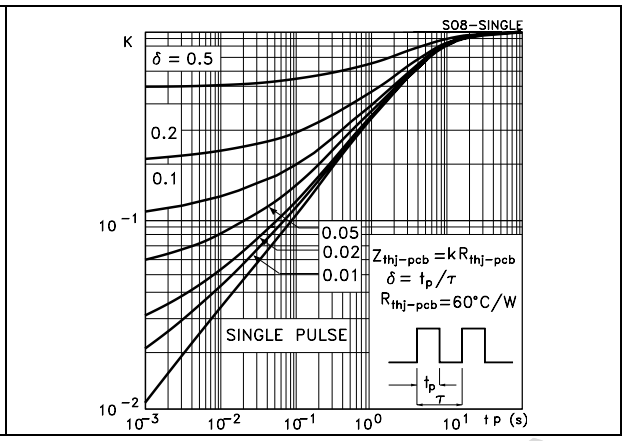


Figure 4. Output characteristics

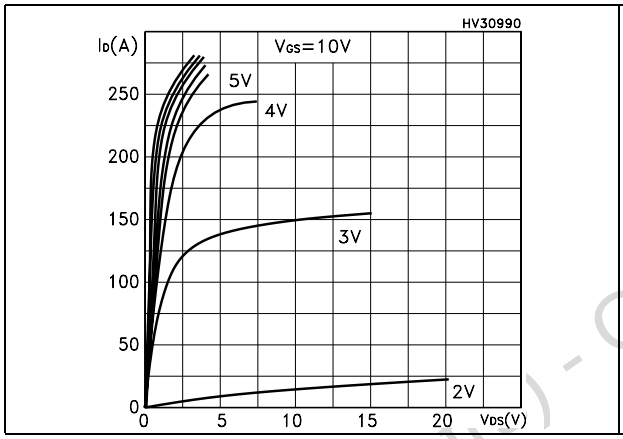


Figure 5. Transfer characteristics

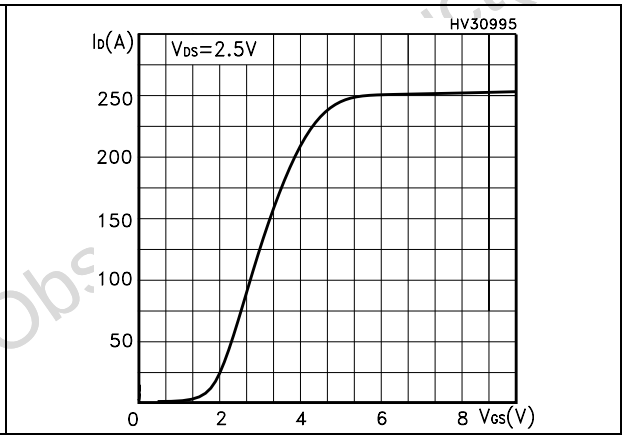


Figure 6. Normalized B_{VDSS} vs temperature

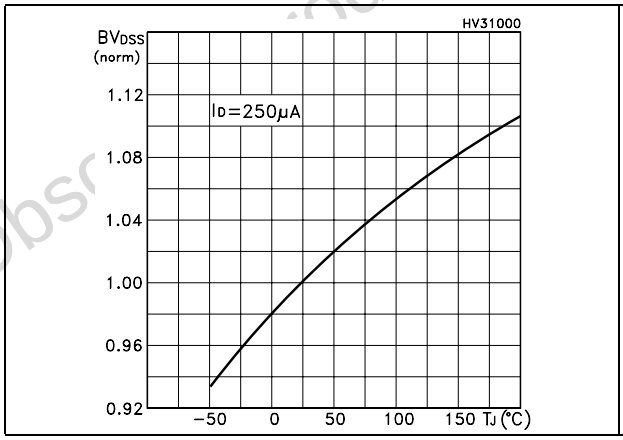


Figure 7. Static drain-source on resistance

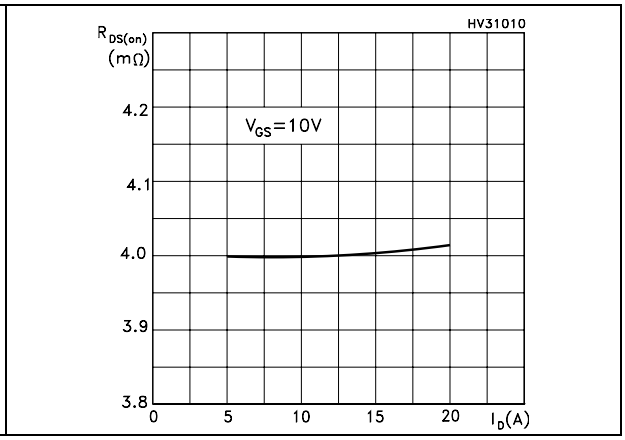


Figure 8. Gate charge vs gate-source voltage

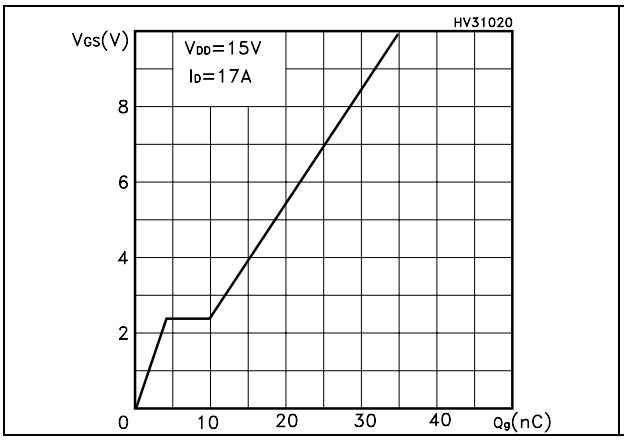


Figure 9. Capacitance variations

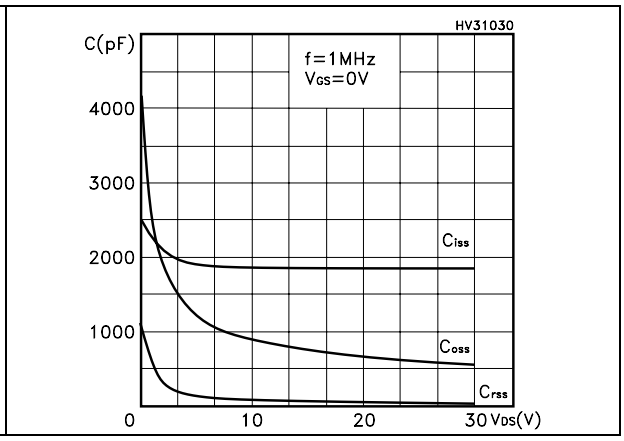


Figure 10. Normalized gate threshold voltage vs temperature

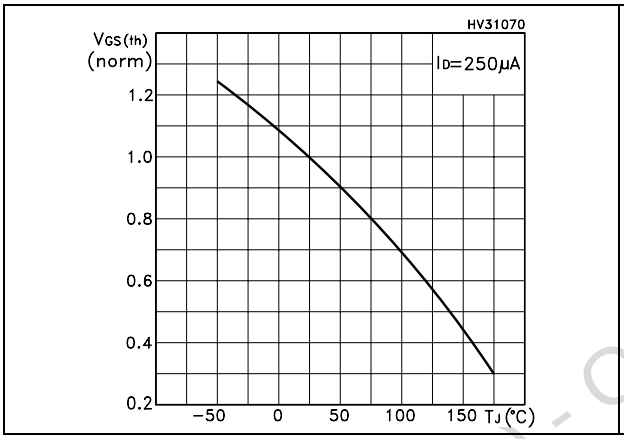


Figure 11. Normalized on resistance vs temperature

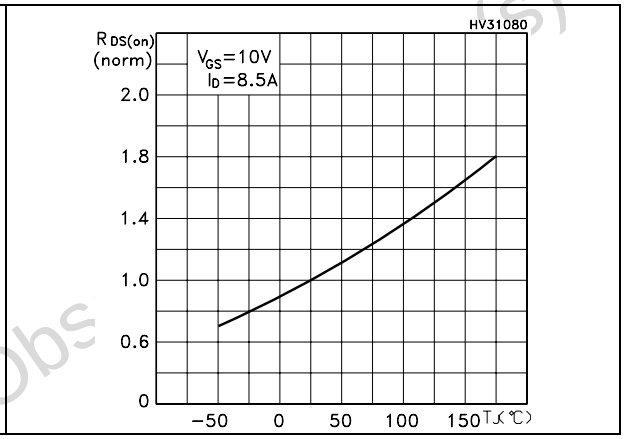
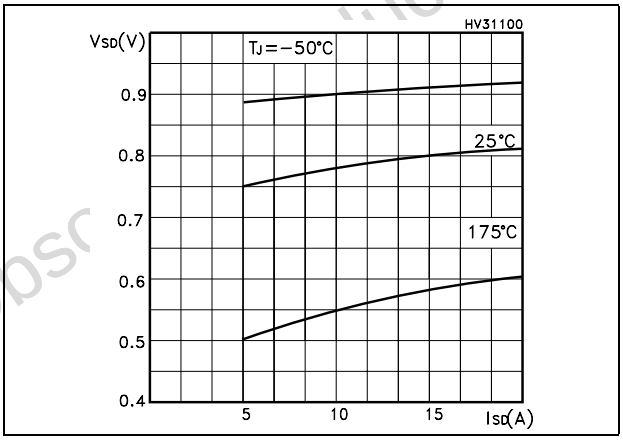


Figure 12. Source-drain diode forward characteristics



3 Test circuit

Figure 13. Switching times test circuit for resistive load

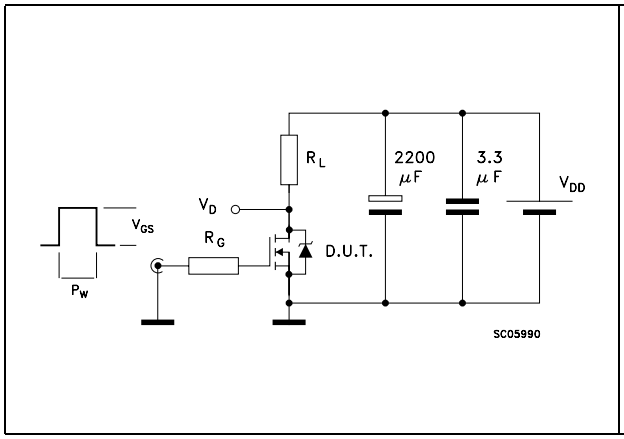


Figure 14. Gate charge test circuit

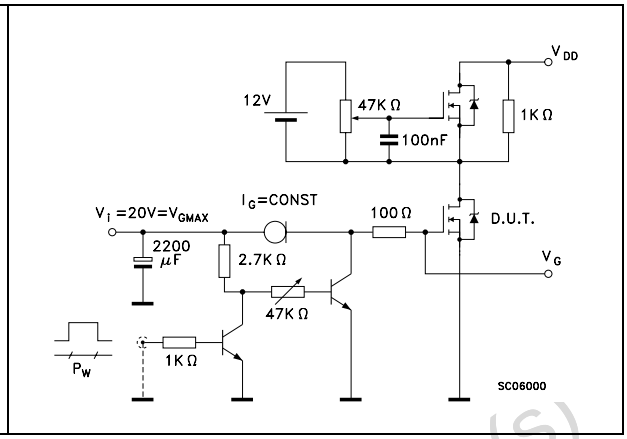


Figure 15. Test circuit for inductive load switching and diode recovery times

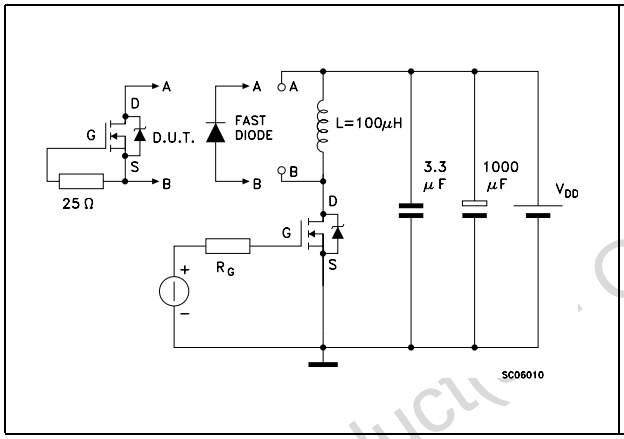


Figure 16. Unclamped inductive load test circuit

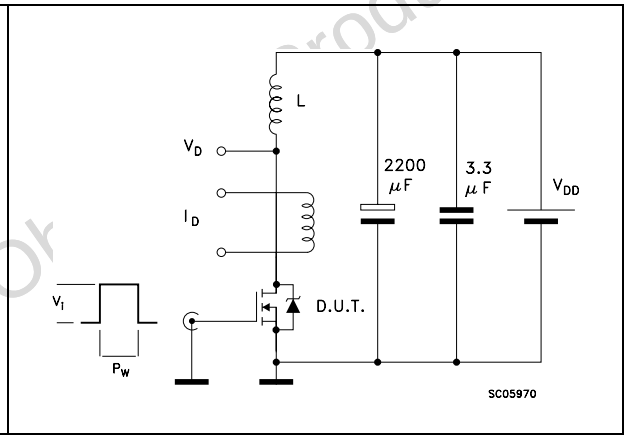


Figure 17. Unclamped inductive waveform

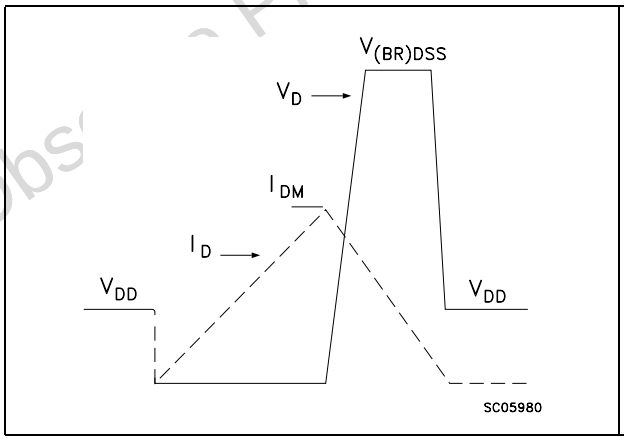
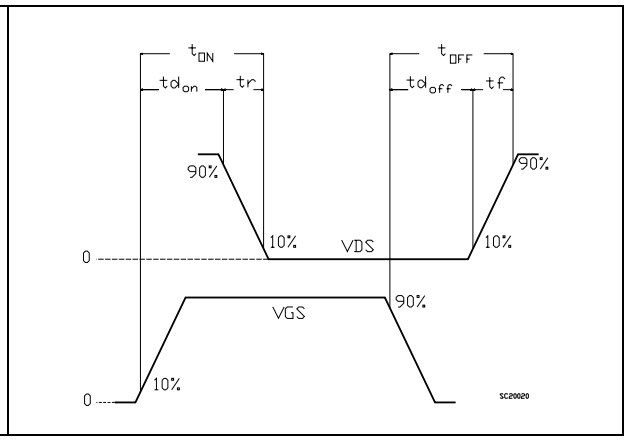


Figure 18. Switching time waveform

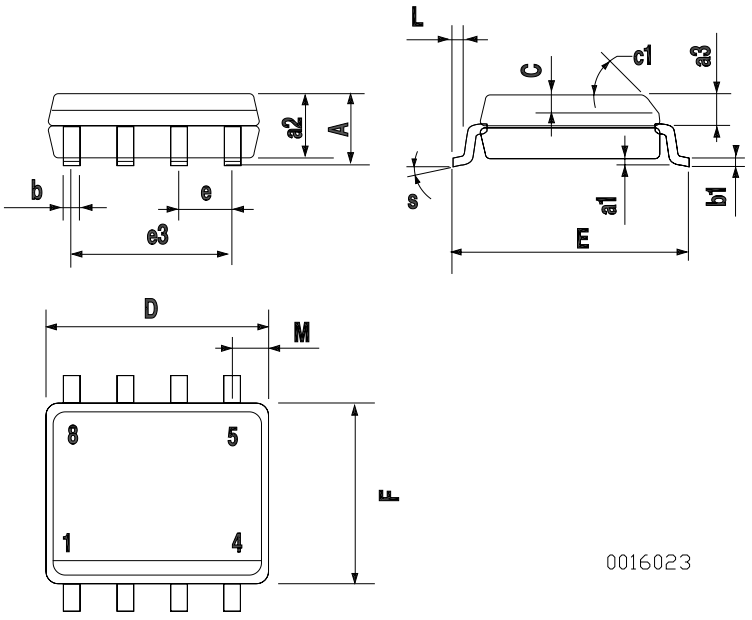


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: *www.st.com*

SO-8 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					



5 Revision history

Table 9. Document revision history

Date	Revision	Changes
01-Aug-2006	1	First release
09-Jan-2007	2	Complete version
12-Dec-2007	3	Inserted new *Table 4: Avalanche data*

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