PCN Number:		202	20221215005.2						PCN Date:		December 16, 2022	
Title	e:	Qualifica	ation	of TI	Malaysia a	as an addi	tiona	I Assembly &	Tes	st site	for sel	ect devices
Cus	tom	er Conta	ıct:	PCN /	<u>Manager</u>	Dept:		Quality Servi	ices	5		
Proposed 1 Ship Hater Hipo 16 7173							Sample Requests accepted until:			Jan 1	6, 2023*	
*Sa	*Sample requests received after Jan 16, 2023 will not be supported.											
Change Type:												
\boxtimes	Asse	embly Sit	e			Design				Wafe	r Bump	Site
	Asse	embly Pro	cess			Data She	eet			Wafe	r Bump	Material
\boxtimes	Asse	embly Ma	terial	S		Part nun	nber	change		Wafe	r Bump	Process
	Mec	hanical S	Specif	icatio	n 🛛	Test Site	е			Wafe	r Fab S	Site
	Pacl	king/Ship	ping/	Labeli	ng 🗆	Test Pro	cess			Wafe	r Fab I	Materials
										Wafe	er Fab Process	
						PCN I	Deta	ails				
Des	cript	tion of C	hang	e:								
	Texas Instruments Incorporated is announcing the qualification of TI Malaysia as an additional Assembly & Test site for the devices listed below. Material differences are as follows:											
					TI Taiwa	n	1	I Malaysia				
	Wire	type			0.96mils <i>A</i>		0.96mils Au (Die to die) 1.0mil Cu (Die to LF)					
Tes	Test coverage, insertions, conditions will remain consistent with current testing.											
Reason for Change:												
Supply continuity												
Ant	icipa	ted imp	act o	n For	m, Fit, Fu	ınction, Ç)uali	ty or Reliabil	ity	(posit	ive /	negative):
Non	None											
Impact on Environmental Ratings												
Checked boxes indicate the status of environmental ratings following implementation of this change. If below boxes are checked, there are no changes to the associated environmental ratings.												
		RoHS			REAC	ЭН		Green Statu		IEC 62474		
					No Change ■ No Change No Change			No Change	Change 🔲 No Char			nange

Changes to product identification resulting from this PCN:

Assembly Site	Assembly Site Origin (22L)	Assembly Country Code (23L)	Assembly City
TI Taiwan	TAI	TWN	Chung Ho, New Taipei City
TI Malaysia	MLA	MYS	Kuala Lumpur

Sample product shipping label (not actual product label)





(1P) \$N74L\$07N\$R

(Q) 2000 (D) 0336

(31T)LOT: 3959047MLA

(4W) TKY(1T) 7523483S12

(P)

(2P) REV: (V) 0033317

(20L) C\$0: SHE (21L) CCO: U\$A

(22L) A\$0: MLA (23L) ACO: MY\$

Product Affected:										
ISO5451QDWQ1	ISO5452QDWQ1	ISO5851QDWQ1	ISO5852SQDWQ1							
ISO5451QDWRQ1	ISO5452QDWRQ1	ISO5851QDWRQ1	ISO5852SQDWRQ1							

Qualification Report Approve Date 08-Dec-2022

Automotive New Product Qualification Summary (As per AEC-Q100 and JEDEC Guidelines)

Product Attributes

Attributes	Qual Device:	QBS Reference:	QBS Reference:	QBS Reference:	QBS Reference:	QBS Reference:
Attributes	ISO5851QDWRQ1	<u>ISO5851</u> Q <u>DWQ1</u>	<u>ISO5851</u> Q <u>DWQ1</u>	<u>ISO5852S</u> Q <u>DWQ1</u>	<u>ISO6741</u> Q <u>DWQ1</u>	UCC21520AQDWRQ1
Automotiv e Grade Level	Grade 1	Grade 1	Grade 1	Grade 1	Grade 1	Grade 1
Operating Temp Range (C)	-40 to 125	-40 to 125	-40 to 125	-40 to 125	-40 to 125	-40 to 125
Product Function	Interface	Interface	Interface	Interface	Interface	Pow er Management
Wafer Fab Supplier	MH8, DP1DM5, DP1DM5	MH8, DP1 DM5, DP1 DM5	DP1 DM5, DP1 DM5, MH8	DP1DM5, DP1DM5, MH8	MH8, MH8	MH8, MH8, MH8
Assembly Site	MLA	TAI	TAI	TAI	MLA	MLA
Package Group	SOIC	SOIC	SOIC	SOIC	SOIC	SOIC
Package Designator	DW	DW	DW	DW	DW	DW
Pin Count	16	16	16	16	16	16

QBS: Qual By Similarity

Qual Device ISO5851QDWRQ1 is qualified at MSL2 260C

Qualification Results

Data Displayed as: Number of lots / Total sample size / Total failed

Тур	e	#	Test Spec	Min Lot Qty	SS / Lot	Test Name	Condition	Duration	Qual Device: ISO5851QDWRQ1	QBS Reference: ISO5851QDWQ1	QBS Reference: ISO5851QDWQ1	QBS Reference: ISO5852SQDWQ1	QBS Reference: ISO6741QDWQ1	QBS Reference: UCC21520AQDWRQ1
Tes	Test Group A - Accelerated Environment Stress Tests													

PC	A1	JEDEC J- STD-020 JESD22- A113	3	77	Preconditioning	MSL2 260C	1 Step	No Fails	-				
PC	A1	JEDEC J- STD-020 JESD22- A113	3	77	Preconditioning	MSL3 260C	1 Step	-	-	-	-	-	No Fails
HAST	A2	JEDEC JESD22- A110	3	77	Biased HAST	130C/85%RH	96 Hours	-	3/231/0	-	1/77/0	3/231/0	3/231/0
AC/UHAST	А3	JEDEC JESD22- A102/JEDEC JESD22- A118	3	77	Autoclave	121C/15psig	96 Hours	1/77/0	1/77/0	2/154/0	1/77/0	3/231/0	3/231/0
rc	A4	JEDEC JESD22- A104 and Appendix 3	3	77	Temperature Cycle	-65C/150C	500 Cycles	1/77/0	1/77/0	2/154/0	1/77/0	3/231/0	3/231/0
HTSL	A6	JEDEC JESD22- A103	1	45	High Temperature Storage Life	150C	1000 Hours	-	-	-	-	3/135/0	-
HTSL	A6	JEDEC JESD22- A103	1	45	High Temperature Storage Life	175C	500 Hours	-	1/45/0	-	1/45/0	-	3/135/0
Tost Grow	n B - Acc	elerated Lifetir	no Simul	ation To	te								
ve st Grou	P D - ACC		Simul	acion res									
HTOL	B1	JEDEC JESD22- A108	1	77	Life Test	125C	1000 Hours	-	3/231/0	-	1/77/0	3/231/0	1/77/0
ELFR	B2	AEC Q100- 008	1	77	Early Life Failure Rate	125C	48 Hours	-	3/2400/0	-	-	-	-
Test Grou	p C - Pac	kage Assembl	y Integrit	y Tests									
WBS	C1	AEC Q100- 001	1	30	Wire Bond Shear	Minimum of 5 devices, 30 wires Cpk>1.67	Wires	3/90/0	1/30/0	2/60/0	1/30/0	3/90/0	3/90/0
WBP	C2	MIL-STD883 Method 2013		30	Wire Bond Pull	Minimum of 9 devices, 30 wires Cpk>1.67	Wires	3/90/0	1/30/0	2/60/0	1/30/0	3/90/0	3/90/0
SD	СЗ	JEDEC JESD22- B102	1	15	PB Solderability	>95% Lead Coverage	-	-	-	1/15/0	-	1/15/0	1/15/0
SD	СЗ	JEDEC JESD22- B102	1	15	PB-Free Solderability	>95% Lead Coverage	-	-	-	1/15/0	-	1/15/0	1/15/0
PD	C4	JEDEC JESD22- B100 and B108	1	10	Physical Dimensions	Cpk>1.67	-	3/30/0	1/10/0	2/20/0	1/10/0	3/30/0	3/30/0
Test Grou	ıp D - Die	Fabrication Re	liability 1	lests									
ЕМ	D1	JESD61	-	-	Electromigration	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements				
TDDB	D2	JESD35	-	-	Time Dependent Dielectric Breakdown	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements				
нсі	D3	JESD60 & 28	-	-	Hot Carrier Injection	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements				
NBTI	D4	-	-	-	Negative Bias Temperature Instability	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements				
SM	D5	-	-	-	Stress Migration	-	-	Completed Per Process Technology Requirements	Completed Per Process Technology Requirements				
Test Grou	ıp E - Ele	ctrical Verificat	ion Tests										
ESD	E2	AEC Q100- 002	1	3	ESD HBM	-	2000 Volts	-	1/3/0	-	1/3/0	1/3/0	-
ESD	E3	AEC Q100- 011	1	3	ESD CDM	-	500 Volts	1/3/0	1/3/0	-	1/3/0	1/3/0	1/3/0
LU	E4	AEC Q100- 004	1	6	Latch-Up	Per AEC Q100-004	-	-	1/6/0	-	1/6/0	1/6/0	-
ED	E5	AEC Q100- 009	3	30	Electrical Distributions	Cpk>1.67 Room, hot, and cold		1/30/0	1/30/0	2/60/0	3/90/0	3/90/0	3/90/0
				_									

Preconditioning was performed for Autoclave, Unbiased HAST, THB/Biased HAST, Temperature Cycle, Thermal Shock, and HTSL, as applicable

The following are equivalent HTOL options based on an activation energy of 0.7eV: 125C/1k Hours, 140C/480 Hours, 150C/300 Hours, and 155C/240 Hours

The following are equivalent HTSL options based on an activation energy of 0.7eV: 150C/1k Hours, and 170C/420 Hours

The following are equivalent Temp Cycle options per JESD47: -55C/125C/700 Cycles and -65C/150C/500 Cycles **Ambient Operating Temperature by Automotive Grade Level:**

Grade 0 (or E): -40C to +150C Grade 1 (or Q): -40C to +125C Grade 2 (or T): -40C to +105C Grade 3 (or I): -40C to +85C

E1 (TEST): Electrical test temperatures of Qual samples (High temperature according to Grade level):

Room/Hot/Cold: HTOL, ED

Room/Hot: THB/HAST, TC/PTC, HTSL, ELFR, ESD & LU

Room: AC/uHAST

Quality and Environmental data is available at TI's external Web site: http://www.ti.com/

For questions regarding this notice, e-mails can be sent to the contacts shown below or your local Field Sales Representative.

Location	E-Mail					
WW Change Management Team	PCN www admin_team@list.ti.com					

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