

# SN74ACT574 Octal D-Type Edge-Triggered Flip-Flops With 3-State Outputs

## 1 Features

- Operation of 4.5-V to 5.5-V  $V_{CC}$
- Inputs accept voltages to 5.5 V
- Max  $t_{pd}$  of 9 ns at 5 V
- Inputs are TTL-Voltage compatible

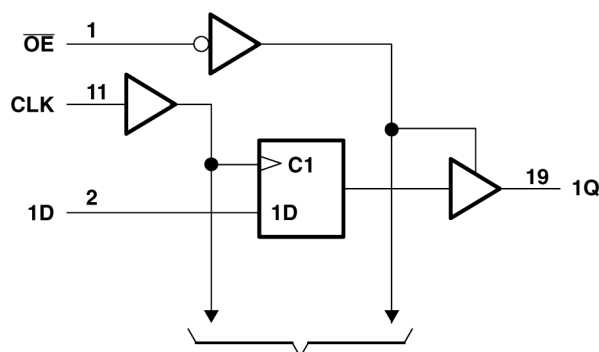
## 2 Description

These 8-bit flip-flops feature 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. The devices are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

### Package Information

PART NUMBER	PACKAGE <sup>1</sup>	BODY SIZE (NOM)
SN74ACT574	DB (SSOP, 20)	7.50 mm × 5.30 mm
	DW (SOIC, 20)	12.80 mm × 7.50 mm
	N (PDIP, 20)	25.40 mm × 6.35 mm
	NS (SOP, 20)	12.6 mm × 5.3 mm
	PW (TSSOP, 20)	6.50 mm × 4.40 mm

1. For all available packages, see the orderable addendum at the end of the data sheet.



To Seven Other Channels

Figure 2-1. Logic Diagram (Positive Logic)



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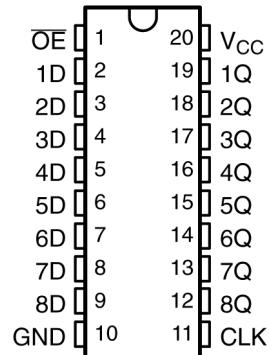
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### 3 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (November 2002) to Revision E (May 2023)	Page
• Added <i>Package Information</i> table, <i>Pin Functions</i> table, and <i>Thermal Information</i> table.....	1

## 4 Pin Configuration and Functions



**Figure 4-1. SN74ACT574 DB, DW, N, NS, or PW Package (Top View)**

**Table 4-1. Pin Functions**

PIN		I/O	DESCRIPTION
NAME	NO.		
OE	1	Input	Output enable for all channels, active low
D1	2	Input	Input for channel 1
D2	3	Input	Input for channel 2
D3	4	Input	Input for channel 3
D4	5	Input	Input for channel 4
D5	6	Input	Input for channel 5
D6	7	Input	Input for channel 6
D7	8	Input	Input for channel 7
D8	9	Input	Input for channel 8
GND	10	—	Ground
CLK	11	Input	Clock input for all channels, rising edge triggered
Q8	12	Output	Output for channel 8
Q7	13	Output	Output for channel 7
Q6	14	Output	Output for channel 6
Q5	15	Output	Output for channel 5
Q4	16	Output	Output for channel 4
Q3	17	Output	Output for channel 3
Q2	18	Output	Output for channel 2
Q1	19	Output	Output for channel 1
V <sub>CC</sub>	20	—	Positive supply

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range	-0.5	7	V
V <sub>I</sub> <sup>2</sup>	Input voltage range	-0.5	V <sub>CC</sub> + 0.5	V
V <sub>O</sub> <sup>2</sup>	Output voltage range	-0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	(V <sub>I</sub> < 0 or V <sub>I</sub> > V <sub>CC</sub> )		±20 mA
I <sub>OK</sub>	Output clamp current	(V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub> )		±20 mA
I <sub>O</sub>	Continuous output current	(V <sub>O</sub> = 0 to V <sub>CC</sub> )		±50 mA
Continuous current through V <sub>CC</sub> or GND				±200 mA
T <sub>stg</sub>	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

### 5.2 Recommended Operating Conditions

See [Note 1](#)

		SN74ACT574		UNIT
		MIN	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage	2		V
V <sub>IL</sub>	Low-level input voltage		0.8	V
V <sub>I</sub>	Input voltage	0	V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current		-8	mA
I <sub>OL</sub>	Low-level output current		8	mA
Δt/Δv	Input transition rise or fall rate		20	ns/V
T <sub>A</sub>	Operating free-air temperature	-40	85	°C

- (1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

### 5.3 Thermal Information

THERMAL METRIC <sup>(1)</sup>	SN74ACT574					UNIT
	DB	DW	N	NS	PW	
	20 PINS					
R <sub>θJA</sub>	70	58	69	60	83	°C/W

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report ([SPRA953](#)).

## 5.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN74ACT574		UNIT
			MIN	TYP	MAX	MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = -50 μA	4.5 V	4.4	4.49		4.4	V	
		5.5 V	5.4	5.49		5.4		
	I <sub>OH</sub> = -24 mA	4.5 V	3.86			3.76		
		5.5 V	4.86			4.76		
	I <sub>OH</sub> = -50 mA <sup>1</sup>	5.5 V						
I <sub>OH</sub> = -75 mA <sup>1</sup>	5.5 V				3.85			
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	4.5 V			0.1	0.1	V	
		5.5 V			0.1	0.1		
	I <sub>OL</sub> = 24 mA	4.5 V			0.36	0.44		
		5.5 V			0.36	0.44		
	I <sub>OL</sub> = 50 mA <sup>1</sup>	5.5 V						
I <sub>OL</sub> = 75 mA <sup>1</sup>	5.5 V				1.65			
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5.5 V			±0.25	±2.5	μA	
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5 V			±0.1	±1	μA	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			4	40	μA	
ΔI <sub>CC</sub> <sup>2</sup>	One input at 3.4 V, Other inputs at GND or V <sub>CC</sub>	5.5 V		0.6		1.5	mA	
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		4.5			pF	

- (1) Not more than one output should be tested at a time, and the duration of the test should not exceed 2 ms.  
(2) This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or V<sub>CC</sub>.

## 5.5 Timing Requirements

over recommended operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER		$T_A = 25^\circ\text{C}$		SN74ACT574		UNIT
		MIN	MAX	MIN	MAX	
$f_{\text{clock}}$	Clock frequency	100		85		MHz
$t_w$	Pulse duration, CLK high or low	3		4		ns
$t_{\text{su}}$	Setup time, data before CLK $\uparrow$	2.5		2.5		ns
$t_h$	Hold time, data after CLK $\uparrow$	1		1		ns

## 5.6 Switching Characteristics

over recommended operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

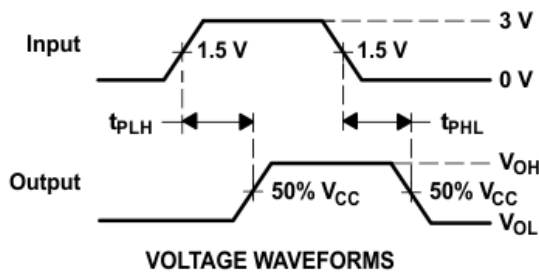
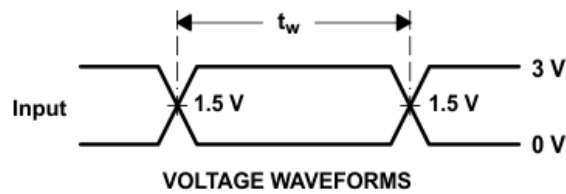
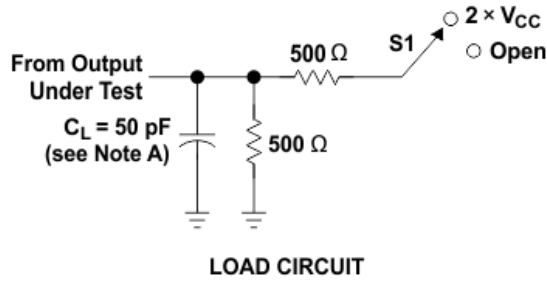
PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			SN74ACT574		UNIT
			MIN	TYP	MAX	MIN	MAX	
$f_{\text{max}}$			100	110		85		MHz
$t_{\text{pd}}$	CLK	Q	2.5	7	11	2	12	ns
			2	6.5	10	1.5	11	
$t_{\text{PHL}}$	$\overline{\text{OE}}$	Q	2	6.4	9.5	1.5	10	ns
			2	6	9	1.5	10	
$t_t$	$\overline{\text{OE}}$	Q	2	7	10.5	1.5	11.5	ns
			2	5.5	8.5	1.5	9	

## 5.7 Operating Characteristics

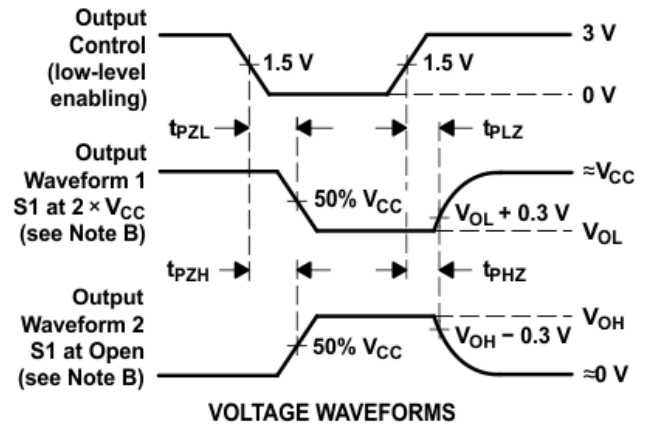
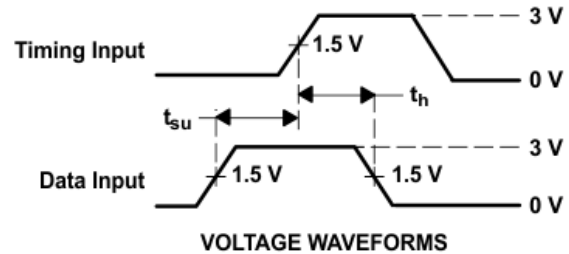
$V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
$C_{\text{pd}}$	Power dissipation capacitance	$C_L = 50\text{ pF}$ , $f = 1\text{ MHz}$	40	pF

## 6 Parameter Measurement Information



TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PLZ}$	$2 \times V_{CC}$
$t_{PHZ}/t_{PHZ}$	Open



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .  
 D. The outputs are measured one at a time with one input transition per measurement.

Figure 6-1. Load Circuit and Voltage Waveforms

## 7 Detailed Description

### 7.1 Overview

The eight flip-flops of the 'ACT574 devices are D-type edge-triggered flip-flops. On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels set up at the data (D) inputs.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines in a bus-organized system without need for interface or pullup components.

$\overline{OE}$  does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

### 7.2 Functional Block Diagram

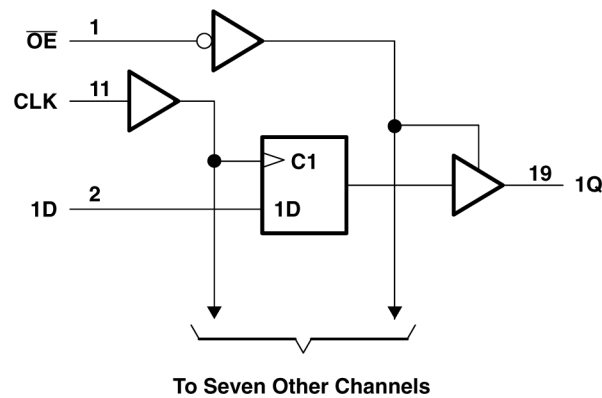


Figure 7-1. Logic Diagram (Positive Logic)

### 7.3 Device Functional Modes

Table 7-1. Function Table (Each Flip-flop)

INPUTS			OUTPUT Q
$\overline{OE}$	CLK	D	
L	↑	H	H
L	↑	L	L
L	H or L	X	$Q_0$
H	X	X	Z



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74ACT574DBR	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AD574	<a href="#">Samples</a>
SN74ACT574DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT574	<a href="#">Samples</a>
SN74ACT574N	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74ACT574N	<a href="#">Samples</a>
SN74ACT574NSR	ACTIVE	SO	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT574	<a href="#">Samples</a>
SN74ACT574PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AD574	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ACT574DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74ACT574DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74ACT574NSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74ACT574PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ACT574DBR	SSOP	DB	20	2000	356.0	356.0	35.0
SN74ACT574DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74ACT574NSR	SO	NS	20	2000	367.0	367.0	45.0
SN74ACT574PWR	TSSOP	PW	20	2000	356.0	356.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74ACT574N	N	PDIP	20	20	506	13.97	11230	4.32

PW0020A



# PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220206/A 02/2017

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

# DB0020A



# PACKAGE OUTLINE

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4214851/B 08/2019

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

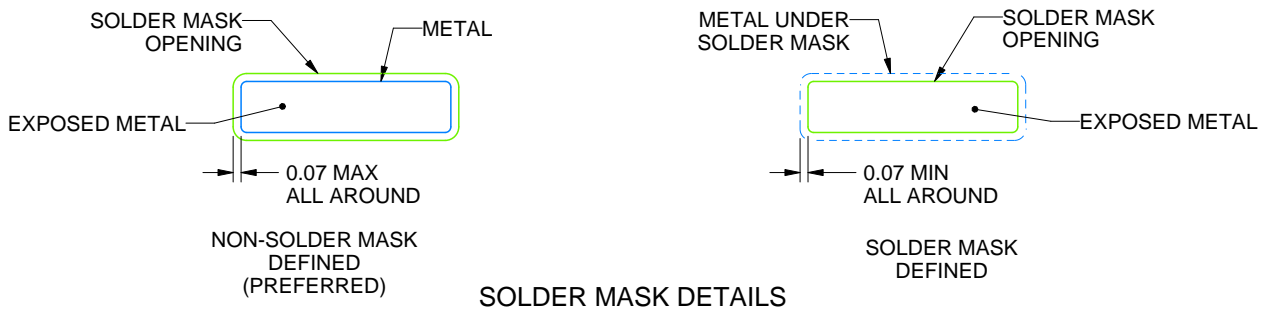
DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4214851/B 08/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

### NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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