PRODUCT CHANGE NOTIFICATION

Linear Technology Corporation
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August 25, 2016

PCN# 082516

Dear Sir/Madam:

Subject: Notification of Change to LTC3882/LTC3882-1 Die and Datasheet

Dear Sir/Madam:

Please be advised that Linear Technology Corporation has made improvements to the LTC3882/LTC3882-1 product die to improve performance in the following areas:

1) Fix errata
2) Reduce power up times
3) Support I^2C PMBus thresholds compatible with bus power supplies as low as 1.8 volts
4) Improve on-chip EEPROM robustness
5) Reduce the ADC update period

The four documented errata in the LTC3882 are eliminated. Refer to the following link for the current LTC3882 errata document http://cds.linear.com/docs/en/spec-notice/er3882fa.pdf.

T_{INIT}, the time required from application of VIN until the part is ready to start sequencing output rails, is reduced from a typical value of 70ms to 30ms. This may allow applications to power up faster after application of VIN. This change is transparent in all applications that require sequencing of multiple power rails using multiple LTC Power System Management (PSM) parts connected in the recommended manner.

I^2C thresholds are reduced in order to support PMBus communication with other ICs using I/O interface supplies as low as 1.8 volts. The VIL and VIH specifications for the SDA, SCL, RUN0, RUN1, GPIO0 and GPIO1 pins are reduced from 1.4V and 2.0V, respectively, to 0.8V and 1.35V. The LTC3882 is fully compliant with PMBus 1.2. For more details, please refer to PMBus 1.2 revisions on the PMBus website http://pmbus.org/Specifications/OlderSpecifications and the SMBus Specification Version 2.0 at http://smbus.org/specs/smbus20.pdf.

Error Correcting Code (ECC) is added to the internal non-volatile memory to enhance its reliability. This change is transparent to the user and requires no modifications to programming files or system firmware. As a consequence of adding ECC, the area in the EEPROM available for fault log is reduced to 4 events. The read length of 147 bytes remains the same but the fifth and sixth

events are a repeat of the fourth event. However, when reading the fault log from RAM, all 6 events of cyclical data remain.

The ADC update period, $T_{CONVERT}$, is reduced from 100ms to 90ms, providing more timely telemetry of all monitored parameters.

The silicon revision can be electronically read via the MFR_SPECIAL_ID PMBus register 420* where * is a value of 8-F for the revised silicon.

The LTC3882 electrical specification changes are shown in the attached red-lined datasheet. No changes were made to the analog sections of the LTC3882, and no PWM characteristics changed. Product specifications are unaffected. The die change was qualified by performing characterization over the full operating junction temperature range and through rigorous engineering evaluation across a broad range of application conditions. In addition, the LTC3882 will have successfully completed the following qualification tests prior to release:

- HTOL stress testing 1000 hours
- HAST testing 192 hours
- Unbiased 150C data retention testing 1000 hours
- Thermal cycles 1000 cycles
- 150C high temperature storage life 1000 hours

Samples of the revised material are available for evaluation. Product built using the improved design is targeted for shipment with an approximate datecode of 1648.

Should you have any further questions, please feel free to contact your local Linear Technology sales person or you may contact me at 408-432-1900 ext. 2374, or by E-mail DJANI@LINEAR.COM. If I do not hear from you by before October 25, 2016, we will consider this change to be approved by your company.

Sincerely,

Daksha Jani
Quality Assurance Engineer

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_J = 25°C (Note 2). V_{CC} = 5V, V_{SENSE0}^+ = V_{SENSE1}^+ = 1.8V, V_{SENSE0}^- = V_{SENSE1}^- = I_{AVG_GND} = GND = 0V, f_{SYNC} = 500kHz (externally driven) unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
IC Supply							
V_{CC}	V_{CC} Voltage Range	V_{DD33} = Internal LDO	●	4.5		13.8	V
V_{DD33_EXT}	V_{DD33} Voltage Range	V_{CC} = V_{DD33} (Note 6)	●	3		3.6	V
V_{UVLO}	Undervoltage Lockout Threshold	V_{DD33} Rising Hysteresis	●		42	3	V mV
I_Q	IC Operating Current				32		mA
t_{INIT}	Controller Initialization Time	Delay from RESTORE_USER_ALL, MFR_RESET or V_{DD33} > V_{UVLO} Until TON_DELAY Can Begin			~~70~~ 30		ms
V_{DD33} Linear Regulator							
V_{DD33}	Internal V_{DD33} Voltage	V_{CC} ≥ 4.5V	●	3.2	3.3	3.4	V
I_{DD33}	V_{DD33} Current Limit	V_{DD33} = 2.8V V_{DD33} = 0V			85 40		mA mA
V_{DD25} Linear Regulator							
V_{DD25}	Internal V_{DD25} Voltage			2.25	2.5	2.75	V
I_{DD25}	V_{DD25} Current Limit				95		mA
PWM Control Loops							
VINSNS	V_{IN} Sense Voltage Range			3		38	V
R_{VINSNS}	VINSNS Input Resistance				278		kΩ
V_{OUT_R0}	Range 0 Maximum V_{OUT} Range 0 Set Point Accuracy (Note 7) Range 0 Resolution Range 0 LSB Step Size	0.6V ≤ V_{OUT} ≤ 5V 0.6V ≤ V_{OUT} ≤ 5V	 ●	 –0.5	5.25 ±0.2 12 1.375	 0.5	V % % Bits mV
V_{OUT_R1}	Range 1 Maximum V_{OUT} Range 1 Set Point Accuracy (Note 7) Range 1 Resolution Range 1 LSB Step Size	0.6V ≤ V_{OUT} ≤ 2.5V 0.6V ≤ V_{OUT} ≤ 2.5V	 ●	 –0.5	2.65 ±0.2 12 0.6875	 0.5	V % % Bits mV
I_{VSENSE}	V_{SENSE} Input Current	V_{SENSE}^+ = 5.5V V_{SENSE}^- = 0V			235 –335		µA µA
$V_{LINEREG}$	V_{CC} Line Regulation, No Output Servo	4.5V ≤ V_{CC} ≤ 13.2V (See Test Circuit)		–0.02		0.02	%/V
AVP	AVP Set Accuracy, ΔV_{OUT} Resolution LSB Step Size	AVP = 10%, VOUT_COMMAND = 1.8V, I_{SENSE} Differential Step 3mV (20%) to 12mV (80%) IOUT_OC_WARN_LIMIT at 15mV	●	–118	 5 0.5	–96	mV Bits %
$A_{V(OL)}$	Error Amplifier Open-Loop Voltage Gain				87		dB
SR	Error Amplifier Slew Rate				9.5		V/µs
f_{0dB}	Error Amplifier Bandwidth				30		MHz
I_{COMP}	Error Amplifier Output Current	Sourcing Sinking			–2.6 34		mA mA
R_{VSFB}	Resistance Between V_{SENSE}^+ and FB	Range 0 Range 1	● ●	52 37	67 49	83 61	kΩ kΩ
V_{ISENSE}	I_{SENSE} Differential Input Range				±70		mV
I_{ISENSE}	$I_{SENSE}^{\pm}$ Input Current	0V ≤ V_{PIN} ≤ 5.5V		–1	±0.1	1	µA
I_{AVG_VOS}	I_{AVG} Current Sense Offset	Referred to I_{SENSE} Inputs	 ●	 –600	±175	 650	µV µV

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{SIOS}	Slave Current Sharing Offset	Referred to I_{SENSE} Inputs			±300		µV
			●	–800		700	µV
f_{SYNC}	SYNC Frequency Accuracy	250kHz ≤ f_{SYNC} ≤ 1.25MHz	●	–10		10	%
Input Voltage Supervisor							
N_{VON}	Input ON/OFF Resolution				8		Bits
	LSB Step Size				143		mV
V_{ON_TOL}	Input ON/OFF Threshold Accuracy	15V ≤ V_{IN_ON} ≤ 35V	●	–2		2	%
Output Voltage Supervisors							
N_{UVOV}	Resolution				9		Bits
V_{UVOV_R0}	Range 0 Maximum Threshold				5.5		V
	Range 0 Accuracy	2V ≤ V_{OUT} ≤ 5V (UV and OV)	●	–1		1	%
	Range 0 LSB Step Size				11		mV
V_{UVOV_R1}	Range 1 Maximum Threshold				2.75		V
	Range 1 Accuracy	1V ≤ V_{OUT} ≤ 2.5V (UV and OV)	●	–1		1	%
	Range 1 LSB Step Size				5.5		mV
Output Current Supervisors							
N_{ILIM}	Resolution				8		Bits
	Step Size	$I_{SENSE}^+ – I_{SENSE}^-$			0.4		mV
V_{ILIM_TOL}	Output Current Limit Accuracy	15mV < $I_{SENSE}^+ – I_{SENSE}^-$ ≤ 30mV	●	–1.7		1.7	mV
		30mV < $I_{SENSE}^+ – I_{SENSE}^-$ ≤ 50mV	●	–2.5		2.5	mV
		50mV < $I_{SENSE}^+ – I_{SENSE}^-$ ≤ 70mV	●	–5.2		5.2	mV
V_{IREV}	I_{REV} Threshold Voltage	$I_{SENSE}^+ – I_{SENSE}^-$			0		mV
ADC Readback Telemetry (Note 8)							
N_{VIN}	VINSNS Readback Resolution	(Note 9)			10		Bits
V_{IN_TUE}	VINSNS Total Unadjusted Readback Error	4.5V ≤ VINSNS ≤ 38V				0.5	%
			●			2	%
N_{DC}	PWM Duty Cycle Resolution	(Note 9)			10		Bits
DC_{TUE}	PWM Duty Cycle Total Unadjusted Readback Error	PWM Duty Cycle = 12.5%		–2		2	%
N_{VOUT}	V_{OUT} Resolution				16		Bits
	LSB Step Size				244		µV
V_{OUT_TUE}	V_{OUT} Total Unadjusted Readback Error	0.6V ≤ V_{OUT} ≤ 5.5V, Constant Load			±0.2		%
			●	–0.5		0.5	%
N_{ISENSE}	I_{OUT} Readback Resolution	(Note 9)			10		Bits
	LSB Step Size (at $I_{SENSE}^{\pm}$)	0mV ≤ $\lvert I_{SENSE}^+ – I_{SENSE}^- \rvert$ < 16mV			15.625		µV
		16mV ≤ $\lvert I_{SENSE}^+ – I_{SENSE}^- \rvert$ < 32mV			31.25		µV
		32mV ≤ $\lvert I_{SENSE}^+ – I_{SENSE}^- \rvert$ < 63.9mV			62.5		µV
		63.9mV ≤ $\lvert I_{SENSE}^+ – I_{SENSE}^- \rvert$ ≤ 70mV			125		µV
I_{SENSE_FS}	I_{OUT} Full Scale Conversion Range				±70		mV
I_{SENSE_TUE}	I_{OUT} Total Unadjusted Readback Error	$\lvert I_{SENSE}^+ – I_{SENSE}^- \rvert$ ≥ 6mV, 0V ≤ V_{OUT} ≤ 5.5V	●	–1		1	%
I_{SENSE_OS}	I_{OUT} Zero-Code Offset Voltage			–32		32	µV
N_{TEMP}	Temperature Resolution				0.25		°C
T_{EXT_TUE}	External Temperature Total Unadjusted Readback Error	TSNS0, TSNS1 ≤ 1.85V (Note 10)					
		MFR_PWM_MODE_LTC3882[6] = 0	●	–3		3	°C
		MFR_PWM_MODE_LTC3882[6] = 1	●	–7		7	°C
T_{INT_TUE}	Internal Temperature Total Unadjusted Readback Error	Internal Diode	●		±1		°C
$t_{CONVERT}$	Update Rate	(Note 11)			~~100~~ 90		ms

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Internal EEPROM (Notes 4, 6)							
Endurance	Number of Write Operations	0°C ≤ T_J ≤ 85°C During All Write Operations	●	10,000			Cycles
Retention	Stored Data Retention	T_J ≤ 125°C	●	10			Years
Mass Write Time	STORE_USER_ALL Execution Duration	0°C ≤ T_J ≤ 85°C During All Write Operations	●		0.2	2	s
Digital Inputs (SCL, SDA, RUN*n*, $\overline{\text{GPIO}n}$, SYNC, SHARE_CLOCK, WP)							
V_{IH}	Input High Voltage	SCL, SDA, RUN0, RUN1, $\overline{\text{GPIO0}}$, $\overline{\text{GPIO1}}$ SYNC, SHARE_CLK, WP	● ●	~~2.0~~ 1.35 1.8			V V
V_{IL}	Input Low Voltage	SCL, SDA, RUN0, RUN1, $\overline{\text{GPIO0}}$, $\overline{\text{GPIO1}}$ SYNC, SHARE_CLK, WP	● ●			~~1.4~~0.8 0.6	V V
V_{HYST}	Input Hysteresis	SCL, SDA			80		mV
I_{PUWP}	Input Pull-Up Current	WP = 0V			10		µA
C_{IN}	Input Capacitance	SCL, SDA, RUN0, RUN1, $\overline{\text{GPIO0}}$, $\overline{\text{GPIO1}}$, SYNC, SHARE_CLK				10	pF
t_{FILT}	Input Digital Filter Delay	$\overline{\text{GPIO0}}$, $\overline{\text{GPIO1}}$ RUN0, RUN1			3 10		µs µs
Digital Outputs (PWM*n*/TG*n*, ENn/BG*n*)							
V_{OL}	Output Low Voltage	I_{SINK} = 2mA	●			300	mV
V_{OH}	Output High Voltage	I_{SOURCE} = 2mA	●	2.7			V
t_{RO}	Output Rise Time	C_{LOAD} = 30pF, 10% to 90%			5		ns
t_{FO}	Output Fall Time	C_{LOAD} = 30pF, 90% to 10%			4		ns
Open Drain and Three State Outputs (SCL, SDA, RUN*n*, $\overline{\text{GPIO}n}$, SYNC, SHARE_CLOCK, $\overline{\text{ALERT}}$, PWM*n*, EN*n*)							
V_{OL}	Output Low Voltage	I_{SINK} = 3mA; SDA, SCL, $\overline{\text{GPIO0}}$, $\overline{\text{GPIO1}}$, $\overline{\text{ALERT}}$, SYNC, RUN0, RUN1, SHARE_CLK	●		0.2	0.4	V
I_{TEST}	PWM Protocol Test Current	EN0, EN1 = 3.3V, MFR_PWM_MODE_LTC3882[2:1] = 0			10		µA
I_{LKG}	Output Leakage Current	0V ≤ PWM0, PWM1 ≤ V_{DD33} 0V ≤ EN0, EN1 ≤ V_{DD33} 0V ≤ $\overline{\text{GPIO0}}$, $\overline{\text{GPIO1}}$ ≤ 3.6V 0V ≤ SYNC, SHARE_CLK ≤ 3.6V 0V ≤ RUN0, RUN1 ≤ 5.5V 0V ≤ SCL, SDA, $\overline{\text{ALERT}}$ ≤ 5.5V	● ● ●	–1 –5 –5		1 5 5	µA µA µA
Serial Bus Timing							
f_{SMB}	Serial Bus Operating Frequency		●	10		400	kHz
t_{BUF}	Bus Free Time Between Stop and Start		●	1.3			µs
$t_{HD,STA}$	Hold Time After (Repeated) Start Condition. After This Period, the First Clock Is Generated		●	0.6			µs
$t_{SU,STA}$	Repeated Start Condition Setup Time		●	0.6			µs
$t_{SU,STO}$	Stop Condition Setup Time		●	0.6			µs
$t_{HD,DAT}$	Data Hold Time: Receiving Data Transmitting Data		 ● ●	 0 0.3		 0.9	 ns µs
$t_{SU,DAT}$	Input Data Setup Time		●	100			ns
$t_{TIMEOUT}$	Clock Low Timeout		●	25		35	ms
t_{LOW}	Serial Clock Low Period		●	1.3		10000	µs
t_{HIGH}	Serial Clock High Period		●	0.6			µs