ESD7321

ESD Protection Diodes

Low Capacitance ESD Protection Diode for High Speed Data Lines

The ESD7321 ESD protection diodes are designed to protect high speed data lines from ESD. Low capacitance and low ESD clamping voltage make this device an ideal solution for protecting voltage sensitive high speed data lines.

Features

- Low Capacitance (0.5 pF Max, I/O to GND)
- Protection for the Following IEC Standards:
  IEC 61000−4−2 (Level 4)
- Low ESD Clamping Voltage
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- USB 3.x
- MHL 2.0
- SATA/SAS
- PCI Express

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Operating Junction Temperature Range	T_J	−55 to +125	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C
Lead Solder Temperature − Maximum (10 Second Duration)	T_L	260	°C
IEC 61000−4−2 Contact (ESD) IEC 61000−4−2 Air (ESD)	ESD ESD	±15 ±15	kV kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

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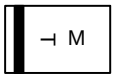
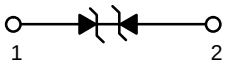
MARKING DIAGRAM

X3DFN2
CASE 152AF



T = Specific Device Code
(Rotated 90° clockwise)
M = Date Code

PIN CONFIGURATION AND SCHEMATIC



ORDERING INFORMATION

Device	Package	Shipping†
ESD7321MUT5G	X3DFN2 (Pb−Free)	10000 / Tape & Reel

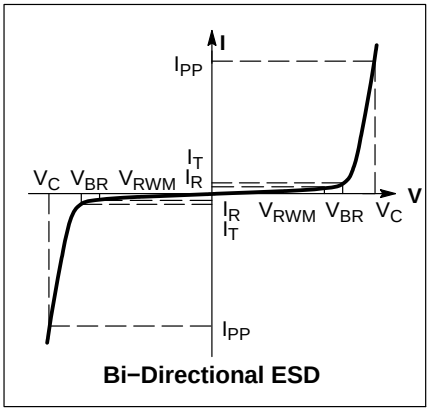
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise noted)

Symbol	Parameter
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Working Peak Reverse Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current

*See Application Note AND8308/D for detailed explanations of datasheet parameters.



Bi−Directional ESD

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Reverse Working Voltage	V_{RWM}				7.0	V
Breakdown Voltage	V_{BR}	I_T = 1 mA (Note 1)	8.0			V
Reverse Leakage Current	I_R	V_{RWM} = 7.0 V, I/O to GND			200	nA
Clamping Voltage	V_C	I_{PP} = 8 A − (IEC61000−4−2 Level 2 Equivalent (±4 kV Contact, ±8 kV Air))		18		V
ESD Clamping Voltage	V_C	Per IEC 61000−4−2	See Figures 1 and 2			
Junction Capacitance	C_J	V_R = 0 V, f = 1 MHz			0.5	pF
Dynamic Resistance	R_{DYN}	TLP Pulse		1		Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Breakdown voltage is tested from pin 1 to 2 and pin 2 to 1.

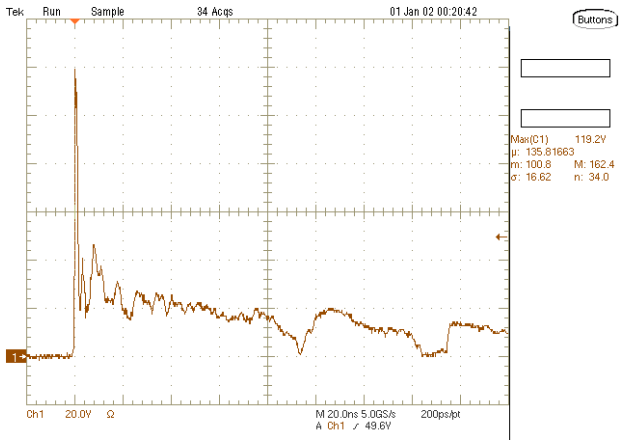


Figure 1. ESD Clamping Voltage Screenshot Positive 8 kV Contact per IEC61000−4−2

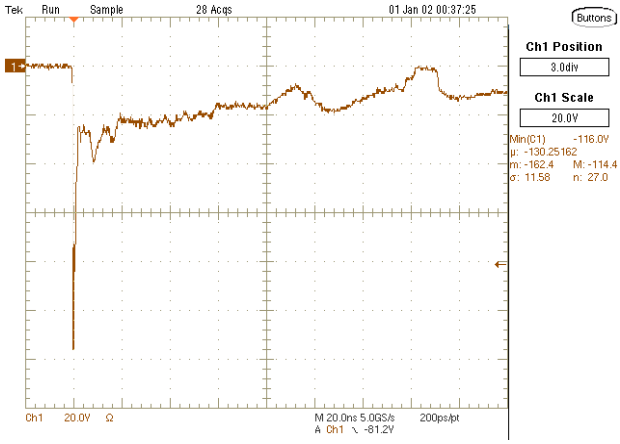


Figure 2. ESD Clamping Voltage Screenshot Negative 8 kV Contact per IEC61000−4−2

TYPICAL CHARACTERISTICS

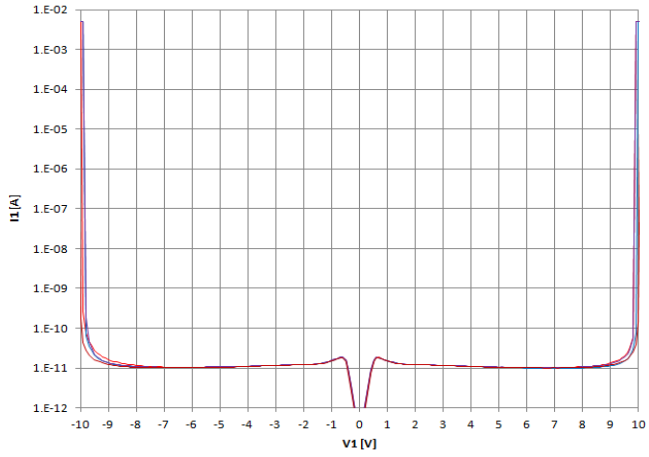


Figure 3. IV Characteristics

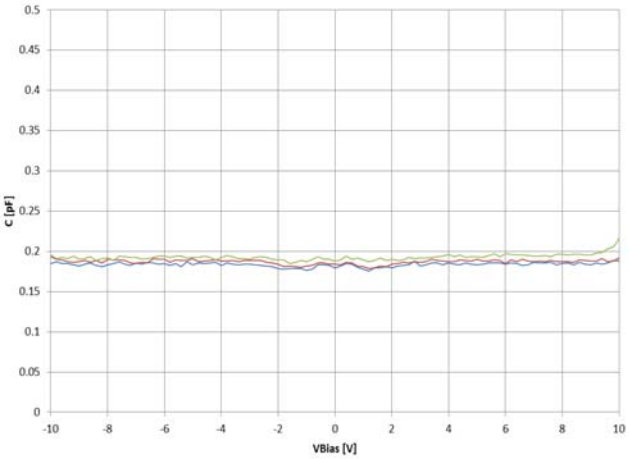


Figure 4. CV Characteristics

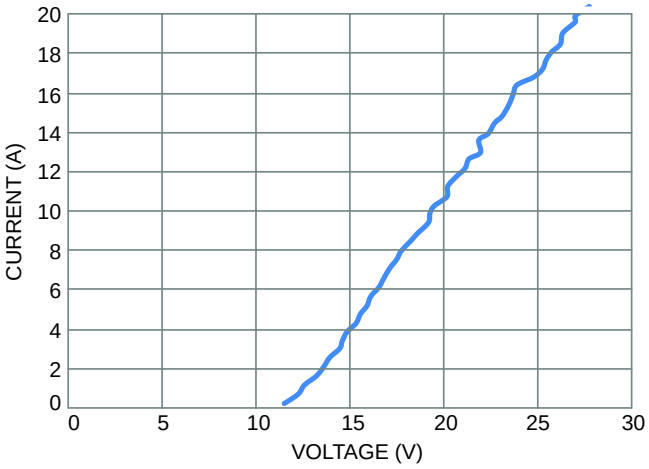


Figure 5. Positive TLP I−V Curve

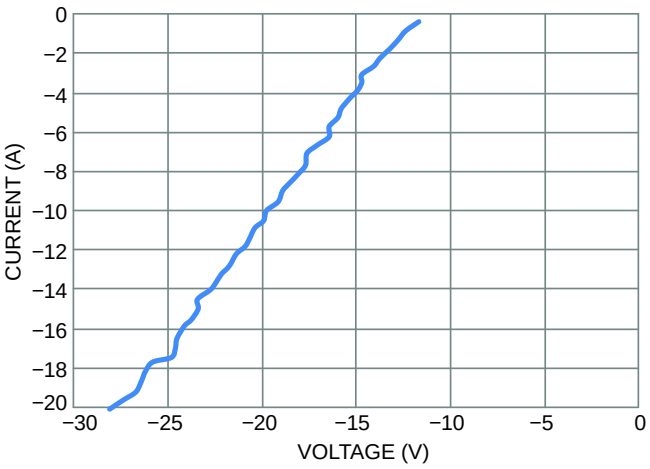


Figure 6. Negative TLP I−V Curve

IEC 61000−4−2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

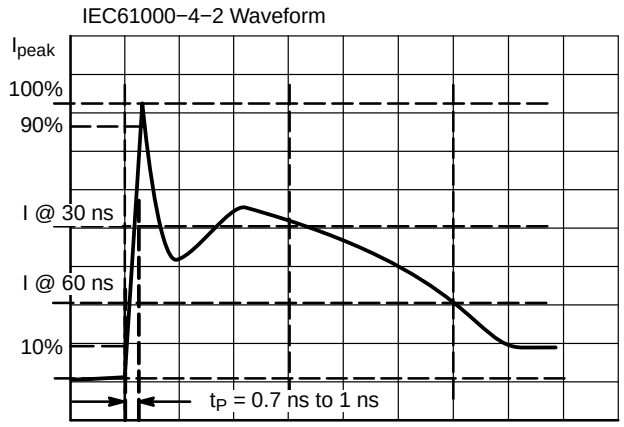


Figure 7. IEC61000−4−2 Spec

Transmission Line Pulse (TLP) Measurement

Transmission Line Pulse (TLP) provides current versus voltage (I−V) curves in which each data point is obtained from a 100 ns long rectangular pulse from a charged transmission line. A simplified schematic of a typical TLP system is shown in Figure 8. TLP I−V curves of ESD protection devices accurately demonstrate the product's ESD capability because the 10s of amps current levels and under 100 ns time scale match those of an ESD event. This is illustrated in Figure 9 where an 8 kV IEC 61000−4−2 current waveform is compared with TLP current pulses at 8 A and 16 A. A TLP I−V curve shows the voltage at which the device turns on as well as how well the device clamps voltage over a range of current levels.

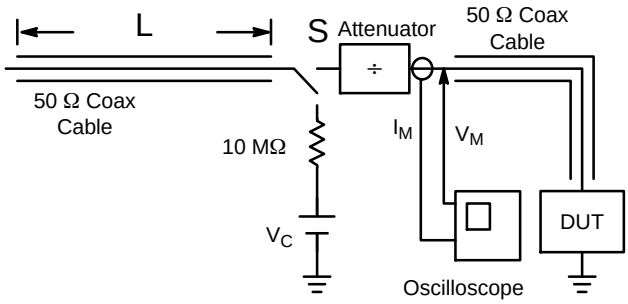


Figure 8. Simplified Schematic of a Typical TLP System

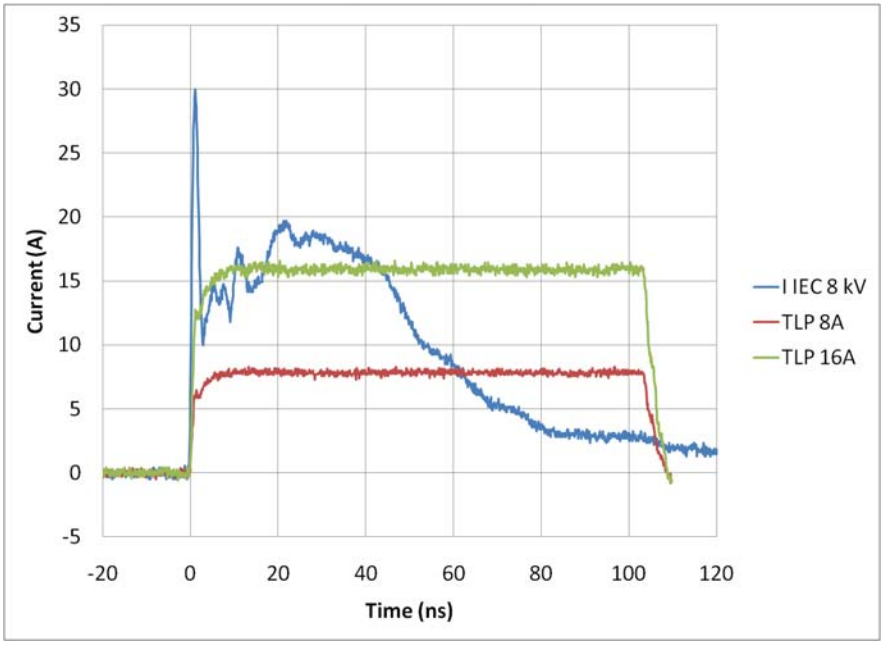
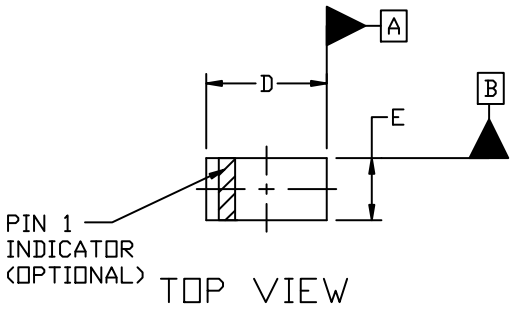


Figure 9. Comparison Between 8 kV IEC 61000−4−2 and 8 A and 16 A TLP Waveforms

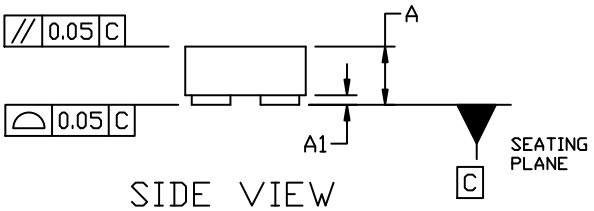
X3DFN2, 0.62x0.32, 0.355P, (0201)
CASE 152AF
ISSUE B

SCALE 8:1

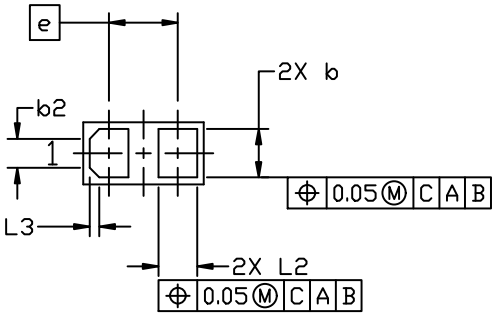
DATE 13 JAN 2023



TOP VIEW



SIDE VIEW

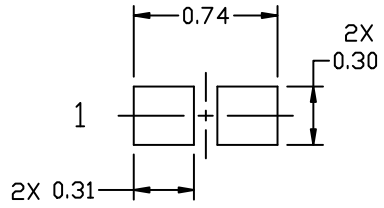


BOTTOM VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS

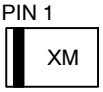
	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	0.25	0.29	0.33
A1	0.00	---	0.05
b	0.22	0.25	0.28
b2	0.150 REF		
D	0.58	0.62	0.66
E	0.28	0.32	0.36
e	0.355 BSC		
L2	0.17	0.20	0.23
L3	0.050 REF		



RECOMMENDED
MOUNTING FOOTPRINT*

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



X = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**X3DFN2, 0.62X0.32, 0.355P, (0201)**	**PAGE 1 OF 1**

PUBLICATION ORDERING INFORMATION

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